

DM74AS646 • DM74AS648

Octal Bus Transceiver and Register

General Description

This device incorporates an octal bus transceiver and an octal D-type register configured to enable multiplexed transmission of data from bus to bus or internal register to bus.

This bus transceiver features totem-pole 3-STATE outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide this device with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. It is particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The registers in the DM74AS646, DM74AS648 are edge-triggered D-type flip-flops. On the positive transition of the clock (CAB or CBA), the input bus data is stored.

The SAB and SBA control pins are provided to select whether real-time data or stored data is transferred. A LOW input level selects real-time data, and a HIGH level selects stored data. The select controls have a "make before break" configuration to eliminate a glitch which would normally occur in a typical multiplexer during the transition between stored and real-time data.

The enable \bar{G} and direction control pins provide four modes of operation; real-time data transfer from bus A to B, real-time data transfer from bus B to A, real-time bus A and/or B data transfer to internal storage, or internal store data transfer to bus A or B.

When the enable \bar{G} pin is LOW, the direction pin selects which bus receives data. When the enable \bar{G} pin is HIGH, both buses become disabled yet their input function is still enabled.

Features

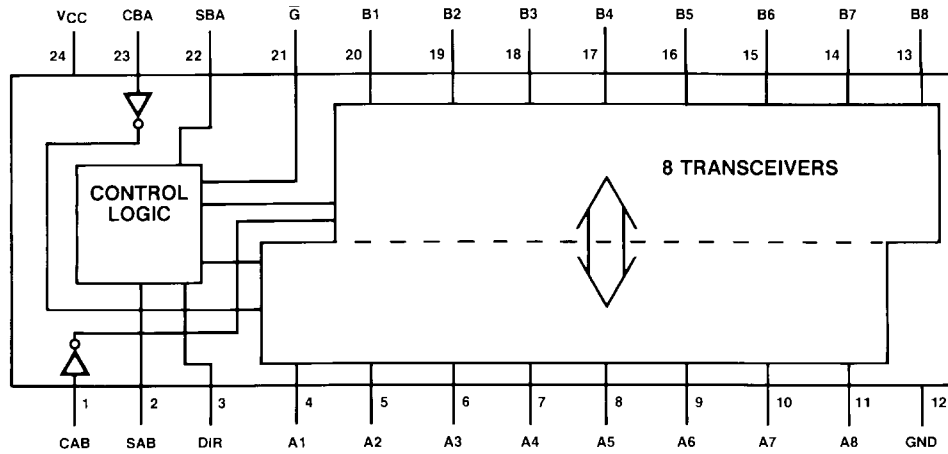
- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin-for-pin compatible with LS TTL counterpart
- 3-STATE buffer-type outputs drive bus lines directly

Ordering Code:

| Order Number | Package Number | Package Description |
|--------------|----------------|--|
| DM74AS646WM | M24B | 24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide |
| DM74AS646NT | N24C | 24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide |
| DM74AS648WM | M24B | 24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide |
| DM74AS648NT | N24C | 24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide |

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Function Table

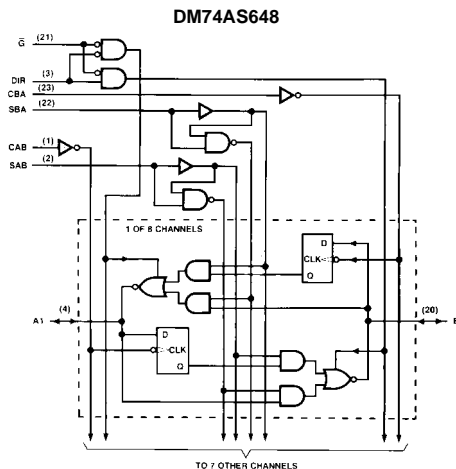
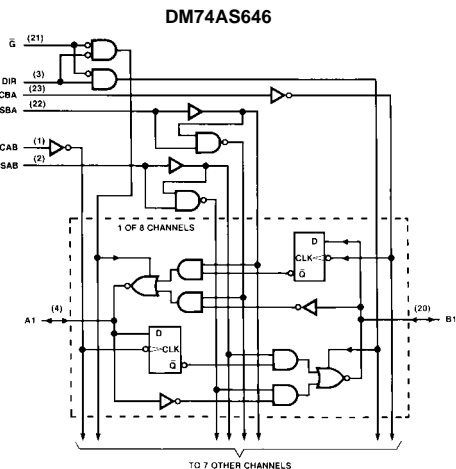
| Inputs | | | | | Data I/O (Note 1) | | Operation or Function | | |
|-----------|-----|------------|------------|-----|-------------------|-------------------------|-------------------------|---|---|
| \bar{G} | DIR | CAB | CBA | SAB | SBA | A1 thru A8 | B1 thru B8 | DM74AS646 | DM74AS648 |
| H | X | H or L | H or L | X | X | Input | Input | Isolation, Hold Storage Store A and B Data | Isolation, Hold Storage Store A and B Data |
| L | L | X | X | X | L | Output | Input | Real Time B Data to A Bus Stored B Data to A Bus | Real Time \bar{B} Data to A Bus Stored \bar{B} Data to A Bus |
| L | H | X | X | L | X | Input | Output | Real Time A Data to B Bus Stored A Data to B Bus | Real Time \bar{A} Data to B Bus Stored \bar{A} Data to B Bus |
| X | X | \uparrow | X | X | X | Input | Unspecified (Note 1) | Store A, B Unspecified (Note 1) | Store A, B Unspecified (Note 1) |
| X | X | X | \uparrow | X | X | Unspecified (Note 1) | Input | Store B, A Unspecified (Note 1) | Store B, A Unspecified (Note 1) |

H—HIGH level; L—LOW level; X—irrelevant; \uparrow —LOW-to-HIGH level transition

Note 1: The data output functions may be enabled or disabled by various signals at the \bar{G} and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW-to-HIGH transition on the clock inputs.

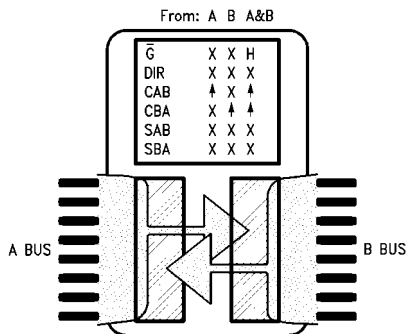
Logic Diagrams

(positive logic)

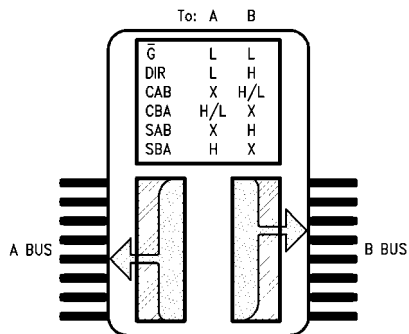


Different Modes of Control for DM74AS646, DM74AS648

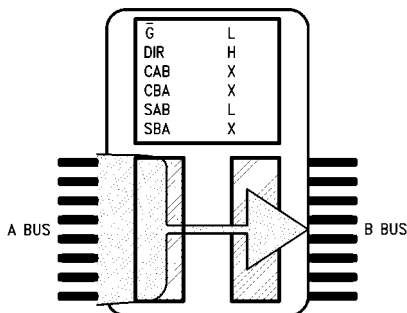
Storage From A, B or A and B



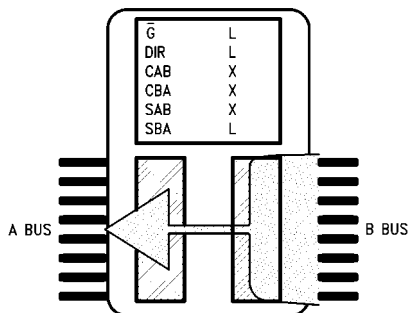
Transfer Stored Data to A or B (Note 2)



Real-Time Transfer Bus A to Bus B (Note 2)



Real-Time Transfer Bus B to Bus A (Note 2)



Note 2: The complement of A and B data are stored and transferred for DM74AS648

Absolute Maximum Ratings(Note 3)

| | |
|--------------------------------------|-----------------|
| Supply Voltage | 7V |
| Input Voltage | |
| Control Inputs | 7V |
| I/O Ports | 5.5V |
| Operating Free Air Temperature Range | 0°C to +70°C |
| Storage Temperature Range | -65°C to +150°C |
| Typical θ_{JA} | |
| N Package | 41.1°C/W |
| M Package | 81.5°C/W |

Note 3: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

| Symbol | Parameter | Min | Nom | Max | Units |
|-----------|--------------------------------|--------------|-----|-----|-------|
| V_{CC} | Supply Voltage | 4.5 | 5 | 5.5 | V |
| V_{IH} | HIGH Level Input Voltage | 2 | | | V |
| V_{IL} | LOW Level Input Voltage | | | 0.8 | V |
| I_{OH} | HIGH Level Output Current | | | -15 | mA |
| I_{OL} | LOW Level Output Current | | | 48 | mA |
| f_{CLK} | Clock Frequency | 0 | | 90 | MHz |
| t_W | Width of Clock Pulse | HIGH | 5 | | ns |
| | | LOW | 6 | | ns |
| t_{SU} | Data Setup Time (Note 4) | 6 \uparrow | | | ns |
| t_H | Data Hold Time (Note 4) | 0 \uparrow | | | ns |
| T_A | Free Air Operating Temperature | 0 | | 70 | °C |

Note 4: The (\uparrow) arrow indicates the positive edge of the Clock is used for reference.

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at $V_{CC} = 5V$, $T_A = 25^\circ C$.

| Symbol | Parameter | Conditions | Min | Typ | Max | Units | |
|----------|-----------------------------------|---|----------------|------------------|-------|---------|----|
| V_{IK} | Input Clamp Voltage | $V_{CC} = 4.5V$, $I_I = -18\text{ mA}$ | | | -1.2 | V | |
| V_{OH} | HIGH Level Output Voltage | $V_{CC} = 4.5V$, $V_{IL} = \text{Max}$, $I_{OH} = \text{Max}$ | 2 | | | V | |
| | | $V_{IH} = \text{Min}$, $I_{OH} = -3\text{ mA}$ | 2.4 | 3.2 | | | |
| | | $V_{CC} = 4.5V$ to $5.5V$, $I_{OH} = -2\text{ mA}$ | $V_{CC} - 2$ | | | | |
| V_{OL} | LOW Level Output Voltage | $V_{CC} = 4.5V$, $V_{IL} = \text{Min}$, $V_{IH} = 2V$, $I_{OL} = \text{Max}$ | | 0.35 | 0.5 | V | |
| I_I | Input Current @ Max Input Voltage | $V_{CC} = 5.5V$, $V_I = 7V$ | Control Inputs | | 0.1 | mA | |
| | | $V_I = 5.5V$ | A or B Ports | | 0.1 | | |
| I_{IH} | HIGH Level Input Current | $V_{CC} = 5.5V$, $V_{IH} = 2.7V$ (Note 5) | Control Inputs | | 20 | μA | |
| | | | A or B Ports | | 70 | | |
| I_{IL} | LOW Level Input Current | $V_{CC} = 5.5V$, $V_{IL} = 0.4V$ (Note 5) | Control Inputs | | -0.5 | mA | |
| | | | A or B Ports | | -0.75 | | |
| I_O | Output Drive Current | $V_{CC} = 5.5V$, $V_O = 2.25V$ | -30 | | -112 | mA | |
| I_{CC} | Supply Current | $V_{CC} = 5.5V$ | DM74AS646 | Outputs HIGH | 120 | 195 | mA |
| | | | | Outputs LOW | 130 | 211 | |
| | | | | Outputs Disabled | 130 | 211 | |
| | | | DM74AS648 | Outputs HIGH | 110 | 185 | |
| | | | | Outputs LOW | 120 | 195 | |
| | | | | Outputs Disabled | 120 | 195 | |

Note 5: For I/O ports, the parameters I_{IH} and I_{IL} include the OFF-State current, I_{OZH} and I_{OZL} .

| DM74AS646 Switching Characteristics | | | | | | | |
|-------------------------------------|--|--|------------------------|-------------|-----|-----|-------|
| Symbol | Parameter | Conditions | From (Input) | To (Output) | Min | Max | Units |
| f_{MAX} | Maximum Clock Frequency | $V_{CC} = 4.5V$ to $5.5V$, $R_1 = R_2 = 500\Omega$ | | | 90 | | MHz |
| t_{PLH} | Propagation Delay Time LOW-to-HIGH Level Output | $C_L = 50$ pF | CBA or CAB | A or B | 2 | 8.5 | ns |
| t_{PHL} | Propagation Delay Time HIGH-to-LOW Level Output | | | | 2 | 9 | ns |
| t_{PLH} | Propagation Delay Time LOW-to-HIGH Level Output | | A or B | B or A | 2 | 9 | ns |
| t_{PHL} | Propagation Delay Time HIGH-to-LOW Level Output | | | | 1 | 7 | ns |
| t_{PLH} | Propagation Delay Time LOW-to-HIGH Level Output | | SBA or SAB (Note 6) | A or B | 2 | 11 | ns |
| t_{PHL} | Propagation Delay Time HIGH-to-LOW Level Output | | | | 2 | 9 | ns |
| t_{PZH} | Output Enable Time to HIGH Level Output | | Enable \bar{G} | A or B | 2 | 9 | ns |
| t_{PZL} | Output Enable Time to LOW Level Output | | | | 3 | 14 | ns |
| t_{PHZ} | Output Disable Time from HIGH Level Output | | | | 2 | 9 | ns |
| t_{PLZ} | Output Disable Time from LOW Level Output | | | | 2 | 9 | ns |
| t_{PZH} | Output Enable Time to HIGH Level Output | | DIR | A or B | 3 | 16 | ns |
| t_{PZL} | Output Enable Time to LOW Level Output | | | | 3 | 18 | ns |
| t_{PHZ} | Output Disable Time from HIGH Level Output | | | | 2 | 10 | ns |
| t_{PLZ} | Output Disable Time from LOW Level Output | | | | 2 | 10 | ns |

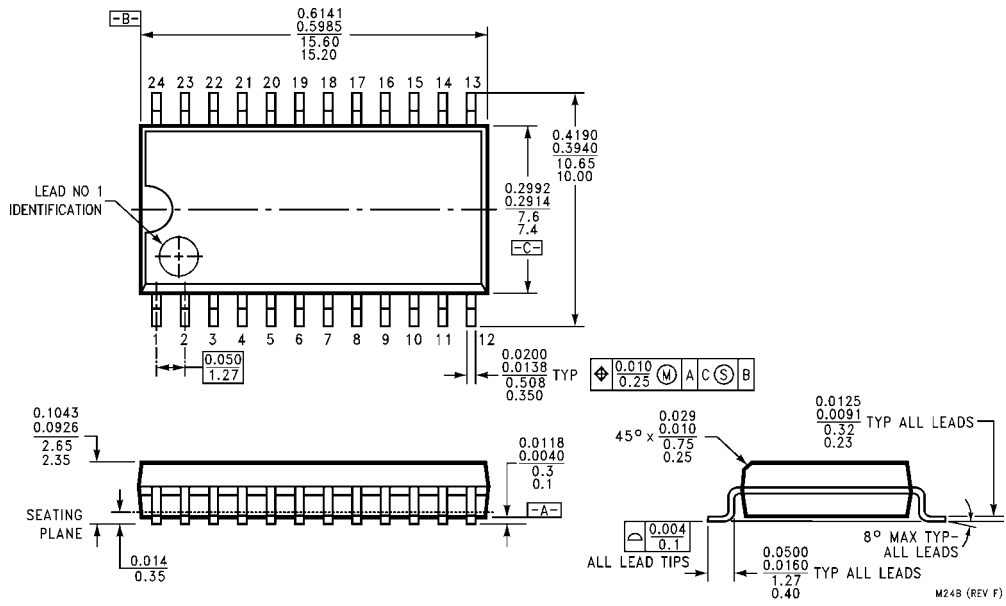
Note 6: These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

DM74AS648 Switching Characteristics

| Symbol | Parameter | Conditions | From (Input) | To (Output) | Min | Max | Units |
|-----------|--|--|------------------------|-------------|-----|-----|-------|
| f_{MAX} | Maximum Clock Frequency | $V_{CC} = 4.5V$ to $5.5V$, | | | 90 | | MHz |
| t_{PLH} | Propagation Delay Time LOW-to-HIGH Level Output | $R_1 = R_2 = 500\Omega$ $C_L = 50$ pF | CAB or CBA | A or B | 2 | 8.5 | ns |
| t_{PHL} | Propagation Delay Time HIGH-to-LOW Level Output | 2 | | | 9 | ns | |
| t_{PLH} | Propagation Delay Time LOW-to-HIGH Level Output | | A or B | B or A | 2 | 8 | ns |
| t_{PHL} | Propagation Delay Time HIGH-to-LOW Level Output | | | | 1 | 7 | ns |
| t_{PLH} | Propagation Delay Time LOW-to-HIGH Level Output | | SBA or SAB (Note 7) | A or B | 2 | 11 | ns |
| t_{PHL} | Propagation Delay Time HIGH-to-LOW Level Output | | | | 2 | 9 | ns |
| t_{pZH} | Output Enable Time to HIGH Level Output | | Enable \bar{G} | A or B | 2 | 9 | ns |
| t_{pZL} | Output Enable Time to LOW Level Output | | | | 3 | 15 | ns |
| t_{pHZ} | Output Disable Time from HIGH Level Output | | | | 2 | 9 | ns |
| t_{pLZ} | Output Disable Time from LOW Level Output | | | | 2 | 9 | ns |
| t_{pZH} | Output Enable Time to HIGH Level Output | | DIR | A or B | 3 | 16 | ns |
| t_{pZL} | Output Enable Time to LOW Level Output | | | | 3 | 18 | ns |
| t_{pHZ} | Output Disable Time from HIGH Level Output | | | | 2 | 10 | ns |
| t_{pLZ} | Output Disable Time from LOW Level Output | | | | 2 | 10 | ns |

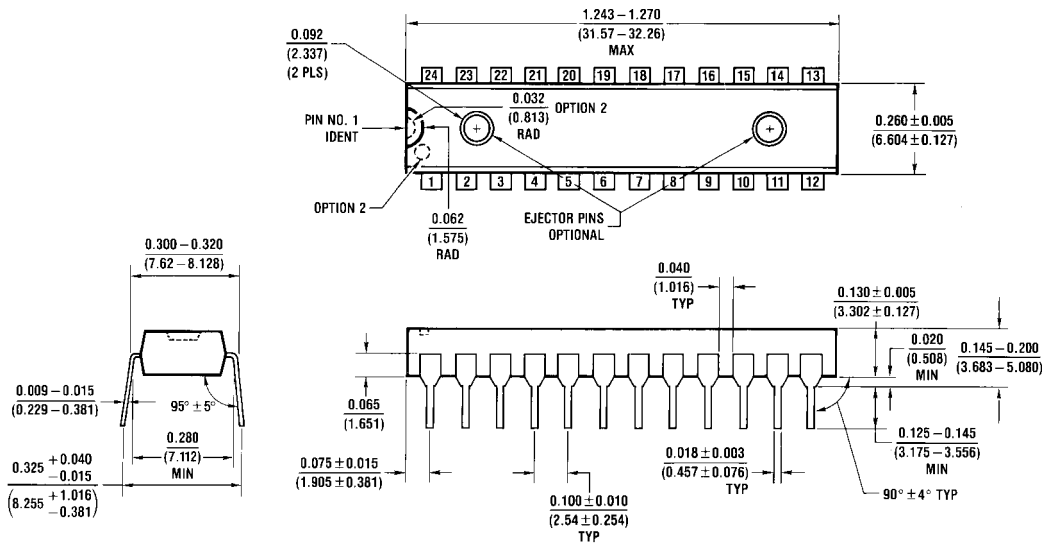
Note 7: These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

Physical Dimensions inches (millimeters) unless otherwise noted



**24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
Package Number M24B**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



N24C (REV F)

24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N24C

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