

MC14511B

BCD-To-Seven Segment Latch/Decoder/Driver

The MC14511B BCD-to-seven segment latch/decoder/driver is constructed with complementary MOS (CMOS) enhancement mode devices and NPN bipolar output drivers in a single monolithic structure. The circuit provides the functions of a 4-bit storage latch, an 8421 BCD-to-seven segment decoder, and an output drive capability. Lamp test (\overline{LT}), blanking (\overline{BI}), and latch enable (LE) inputs are used to test the display, to turn-off or pulse modulate the brightness of the display, and to store a BCD code, respectively. It can be used with seven-segment light-emitting diodes (LED), incandescent, fluorescent, gas discharge, or liquid crystal readouts either directly or indirectly.

Applications include instrument (e.g., counter, DVM, etc.) display driver, computer/calculator display driver, cockpit display driver, and various clock, watch, and timer uses.

- Low Logic Circuit Power Dissipation
- High-Current Sourcing Outputs (Up to 25 mA)
- Latch Storage of Code
- Blanking Input
- Lamp Test Provision
- Readout Blanking on all Illegal Input Combinations
- Lamp Intensity Modulation Capability
- Time Share (Multiplexing) Facility
- Supply Voltage Range = 3.0 V to 18 V
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Chip Complexity: 216 FETs or 54 Equivalent Gates
- Triple Diode Protection on all Inputs

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

| Rating | Symbol | Value | Unit |
|---|-------------|-------------------------|------|
| DC Supply Voltage | V_{DD} | - 0.5 to + 18 | V |
| Input Voltage, All Inputs | V_{in} | - 0.5 to $V_{DD} + 0.5$ | V |
| DC Current Drain per Input Pin | I | 10 | mA |
| Operating Temperature Range | T_A | - 55 to + 125 | °C |
| Power Dissipation per Package† | P_D | 500 | mW |
| Storage Temperature Range | T_{stg} | - 65 to + 150 | °C |
| Maximum Output Drive Current (Source) per Output | I_{OHmax} | 25 | mA |
| Maximum Continuous Output Power (Source) per Output ‡ | P_{OHmax} | 50 | mW |

‡ $P_{OHmax} = I_{OH} (V_{DD} - V_{OH})$

* Maximum Ratings are those values beyond which damage to the device may occur.

† Temperature Derating:

Plastic "P and D/DW" Packages: - 7.0 mW/°C From 65°C To 125°C

Ceramic "L" Packages: - 12 mW/°C From 100°C To 125°C



L SUFFIX
CERAMIC
CASE 620



P SUFFIX
PLASTIC
CASE 648



D SUFFIX
SOIC
CASE 751B



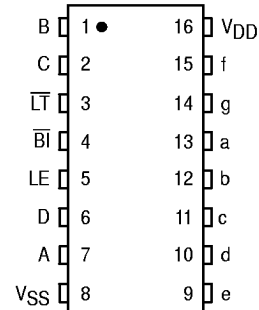
DW SUFFIX
SOIC
CASE 751G

ORDERING INFORMATION

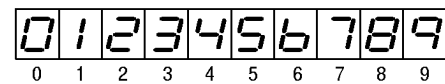
| | |
|------------|---------|
| MC14XXXBCP | Plastic |
| MC14XXXBCL | Ceramic |
| MC14XXXBDW | SOIC |
| MC14XXXBD | SOIC |

$T_A = -55^\circ$ to 125° C for all packages.

PIN ASSIGNMENT



DISPLAY



TRUTH TABLE

| Inputs | | | | Outputs | | | | | | | |
|--------|----|----|---------|---------|---|---|---|---|---|---|---------|
| LE | BI | LT | D C B A | a | b | c | d | e | f | g | Display |
| X | X | 0 | X X X X | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 8 |
| X | 0 | 1 | X X X X | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Blank |
| 0 | 1 | 1 | 0 0 0 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 0 0 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |
| 0 | 1 | 1 | 0 0 1 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 2 |
| 0 | 1 | 1 | 0 0 1 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 3 |
| 0 | 1 | 1 | 0 1 0 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 4 |
| 0 | 1 | 1 | 0 1 0 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 5 |
| 0 | 1 | 1 | 0 1 1 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 6 |
| 0 | 1 | 1 | 0 1 1 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 7 |
| 0 | 1 | 1 | 1 0 0 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 8 |
| 0 | 1 | 1 | 1 0 0 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 9 |
| 0 | 1 | 1 | 1 0 1 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Blank |
| 0 | 1 | 1 | 1 0 1 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Blank |
| 0 | 1 | 1 | 1 1 0 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Blank |
| 0 | 1 | 1 | 1 1 0 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Blank |
| 0 | 1 | 1 | 1 1 1 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Blank |
| 0 | 1 | 1 | 1 1 1 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Blank |
| 1 | 1 | 1 | X X X X | - | - | - | - | - | - | - | - |

X = Don't Care

* Depends upon the BCD code previously applied when LE = 0



ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

| Characteristic | Symbol | V _{DD} Vdc | - 55°C | | 25°C | | | 125°C | | Unit | |
|--|---|------------------------|---|-------|------|-----------|-------|-------|-------|------|-----|
| | | | Min | Max | Min | Typ # | Max | Min | Max | | |
| Output Voltage V _{in} = V _{DD} or 0 | "0" Level V _{OL} | 5.0 | — | 0.05 | — | 0 | 0.05 | — | 0.05 | Vdc | |
| | | 10 | — | 0.05 | — | 0 | 0.05 | — | 0.05 | | |
| 15 | | — | 0.05 | — | 0 | 0.05 | — | 0.05 | | | |
| V _{in} = 0 or V _{DD} | "1" Level V _{OH} | 5.0 | 4.1 | — | 4.1 | 4.57 | — | 4.1 | — | Vdc | |
| | | 10 | 9.1 | — | 9.1 | 9.58 | — | 9.1 | — | | |
| | | 15 | 14.1 | — | 14.1 | 14.59 | — | 14.1 | — | | |
| Input Voltage # (V _O = 3.8 or 0.5 Vdc) (V _O = 8.8 or 1.0 Vdc) (V _O = 13.8 or 1.5 Vdc) | "0" Level V _{IL} | 5.0 | — | 1.5 | — | 2.25 | 1.5 | — | 1.5 | Vdc | |
| | | 10 | — | 3.0 | — | 4.50 | 3.0 | — | 3.0 | | |
| | | 15 | — | 4.0 | — | 6.75 | 4.0 | — | 4.0 | | |
| | "1" Level (V _O = 0.5 or 3.8 Vdc) (V _O = 1.0 or 8.8 Vdc) (V _O = 1.5 or 13.8 Vdc) | V _{IH} | 5.0 | 3.5 | — | 3.5 | 2.75 | — | 3.5 | — | Vdc |
| | | | 10 | 7.0 | — | 7.0 | 5.50 | — | 7.0 | — | |
| | | | 15 | 11 | — | 11 | 8.25 | — | 11 | — | |
| Output Drive Voltage (I _{OH} = 0 mA) (I _{OH} = 5.0 mA) (I _{OH} = 10 mA) (I _{OH} = 15 mA) (I _{OH} = 20 mA) (I _{OH} = 25 mA) | Source V _{OH} | 5.0 | 4.1 | — | 4.1 | 4.57 | — | 4.1 | — | Vdc | |
| | | | — | — | — | 4.24 | — | — | — | | |
| | | | 3.9 | — | 3.9 | 4.12 | — | 3.5 | — | | |
| | | | — | — | — | 3.94 | — | — | — | | |
| | | | 3.4 | — | 3.4 | 3.70 | — | 3.0 | — | | |
| | | | — | — | — | 3.54 | — | — | — | | |
| | | 10 | 9.1 | — | 9.1 | 9.58 | — | 9.1 | — | Vdc | |
| | | | — | — | — | 9.26 | — | — | — | | |
| | | | 9.0 | — | 9.0 | 9.17 | — | 8.6 | — | | |
| | | | — | — | — | 9.04 | — | — | — | | |
| | | | 8.6 | — | 8.6 | 8.90 | — | 8.2 | — | | |
| | | | — | — | — | 8.70 | — | — | — | | |
| | | 15 | 14.1 | — | 14.1 | 14.59 | — | 14.1 | — | Vdc | |
| | | | — | — | — | 14.27 | — | — | — | | |
| | | | 14 | — | 14 | 14.18 | — | 13.6 | — | | |
| — | — | | — | 14.07 | — | — | — | | | | |
| 13.6 | — | | 13.6 | 13.95 | — | 13.2 | — | | | | |
| — | — | | — | 13.70 | — | — | — | | | | |
| Output Drive Current (V _{OL} = 0.4 V) (V _{OL} = 0.5 V) (V _{OL} = 1.5 V) | Sink I _{OL} | 5.0 | 0.64 | — | 0.51 | 0.88 | — | 0.36 | — | mAdc | |
| | | 10 | 1.6 | — | 1.3 | 2.25 | — | 0.9 | — | | |
| | | 15 | 4.2 | — | 3.4 | 8.8 | — | 2.4 | — | | |
| Input Current | I _{in} | 15 | — | ± 0.1 | — | ± 0.00001 | ± 0.1 | — | ± 1.0 | μAdc | |
| Input Capacitance | C _{in} | — | — | — | — | 5.0 | 7.5 | — | — | pF | |
| Quiescent Current (Per Package) V _{in} = 0 or V _{DD} , I _{out} = 0 μA | I _{DD} | 5.0 | — | 5.0 | — | 0.005 | 5.0 | — | 150 | μAdc | |
| | | 10 | — | 10 | — | 0.010 | 10 | — | 300 | | |
| | | 15 | — | 20 | — | 0.015 | 20 | — | 600 | | |
| Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching) | I _T | 5.0 | I _T = (1.9 μA/kHz) f + I _{DD} | | | | | | μAdc | | |
| | | 10 | I _T = (3.8 μA/kHz) f + I _{DD} | | | | | | | | |
| | | 15 | I _T = (5.7 μA/kHz) f + I _{DD} | | | | | | | | |

#Noise immunity specified for worst-case input combination.

Noise Margin for both "1" and "0" level =
 1.0 Vdc min @ V_{DD} = 5.0 Vdc
 2.0 Vdc min @ V_{DD} = 10 Vdc
 2.5 Vdc min @ V_{DD} = 15 Vdc

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + 3.5 \times 10^{-3} (C_L - 50) V_{DD} f$$

where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

SWITCHING CHARACTERISTICS* ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

| Characteristic | Symbol | VDD Vdc | Min | Typ | Max | Unit |
|--|------------------------------------|--|--------------------------------|--|--|------|
| Output Rise Time $t_{TLH} = (0.40 \text{ ns/pF}) C_L + 20 \text{ ns}$ $t_{TLH} = (0.25 \text{ ns/pF}) C_L + 17.5 \text{ ns}$ $t_{TLH} = (0.20 \text{ ns/pF}) C_L + 15 \text{ ns}$ | t_{TLH} | 5.0 10 15 | — — — | 40 30 25 | 80 60 50 | ns |
| Output Fall Time $t_{THL} = (1.5 \text{ ns/pF}) C_L + 50 \text{ ns}$ $t_{THL} = (0.75 \text{ ns/pF}) C_L + 37.5 \text{ ns}$ $t_{THL} = (0.55 \text{ ns/pF}) C_L + 37.5 \text{ ns}$ | t_{THL} | 5.0 10 15 | — — — | 125 75 65 | 250 150 130 | ns |
| Data Propagation Delay Time $t_{PLH} = (0.40 \text{ ns/pF}) C_L + 620 \text{ ns}$ $t_{PLH} = (0.25 \text{ ns/pF}) C_L + 237.5 \text{ ns}$ $t_{PLH} = (0.20 \text{ ns/pF}) C_L + 165 \text{ ns}$ $t_{PHL} = (1.3 \text{ ns/pF}) C_L + 655 \text{ ns}$ $t_{PHL} = (0.60 \text{ ns/pF}) C_L + 260 \text{ ns}$ $t_{PHL} = (0.35 \text{ ns/pF}) C_L + 182.5 \text{ ns}$ | t_{PLH} t_{PHL} | 5.0 10 15 5.0 10 15 | — — — — — — | 640 250 175 720 290 200 | 1280 500 350 1440 580 400 | ns |
| Blank Propagation Delay Time $t_{PLH} = (0.30 \text{ ns/pF}) C_L + 585 \text{ ns}$ $t_{PLH} = (0.25 \text{ ns/pF}) C_L + 187.5 \text{ ns}$ $t_{PLH} = (0.15 \text{ ns/pF}) C_L + 142.5 \text{ ns}$ $t_{PHL} = (0.85 \text{ ns/pF}) C_L + 442.5 \text{ ns}$ $t_{PHL} = (0.45 \text{ ns/pF}) C_L + 177.5 \text{ ns}$ $t_{PHL} = (0.35 \text{ ns/pF}) C_L + 142.5 \text{ ns}$ | t_{PLH} t_{PHL} | 5.0 10 15 5.0 10 15 | — — — — — — | 600 200 150 485 200 160 | 750 300 220 970 400 320 | ns |
| Lamp Test Propagation Delay Time $t_{PLH} = (0.45 \text{ ns/pF}) C_L + 290.5 \text{ ns}$ $t_{PLH} = (0.25 \text{ ns/pF}) C_L + 112.5 \text{ ns}$ $t_{PLH} = (0.20 \text{ ns/pF}) C_L + 80 \text{ ns}$ $t_{PHL} = (1.3 \text{ ns/pF}) C_L + 248 \text{ ns}$ $t_{PHL} = (0.45 \text{ ns/pF}) C_L + 102.5 \text{ ns}$ $t_{PHL} = (0.35 \text{ ns/pF}) C_L + 72.5 \text{ ns}$ | t_{PLH} t_{PHL} | 5.0 10 15 5.0 10 15 | — — — — — — | 313 125 90 313 125 90 | 625 250 180 625 250 180 | ns |
| Setup Time | t_{su} | 5.0 10 15 | 100 40 30 | — — — | — — — | ns |
| Hold Time | t_h | 5.0 10 15 | 60 40 30 | — — — | — — — | ns |
| Latch Enable Pulse Width | t_{WL} | 5.0 10 15 | 520 220 130 | 260 110 65 | — — — | ns |

* The formulas given are for the typical characteristics only.

This device contains protection circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. A destructive high current mode may occur if V_{in} and V_{out} are not constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

Due to the sourcing capability of this circuit, damage can occur to the device if V_{DD} is applied, and the outputs are shorted to V_{SS} and are at a logical 1 (See Maximum Ratings).

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

Input LE low, and Inputs D, $\overline{B1}$ and $\overline{L1}$ high.
 f in respect to a system clock.
 All outputs connected to respective C_L loads.

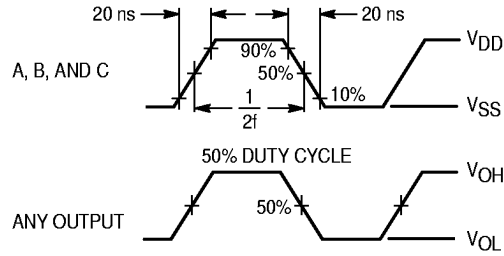
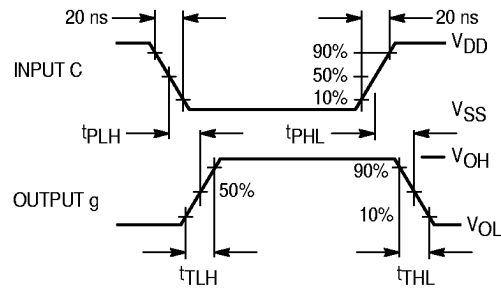
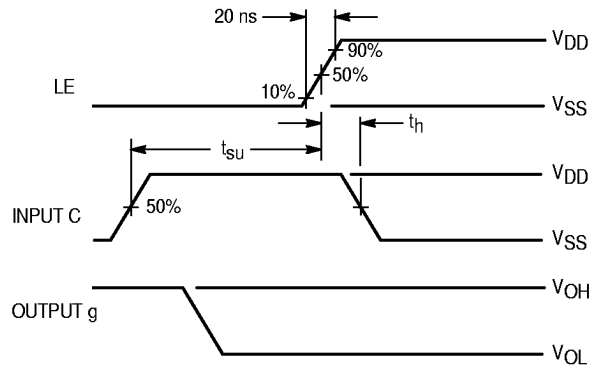


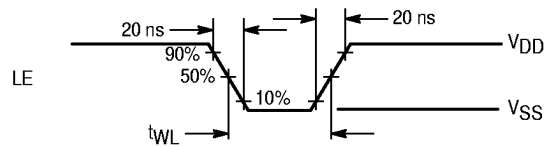
Figure 1. Dynamic Power Dissipation Signal Waveforms



(a) Inputs D and LE low, and Inputs A, B, $\overline{B1}$ and $\overline{L1}$ high.



(b) Input D low, Inputs A, B, $\overline{B1}$ and $\overline{L1}$ high.

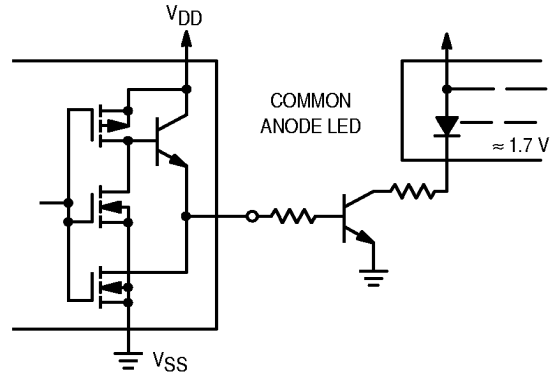
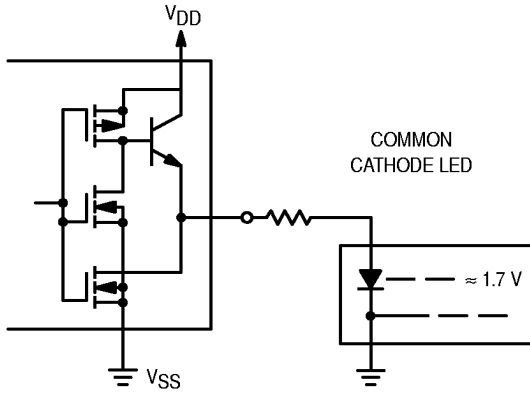


(c) Data DCBA strobed into latches.

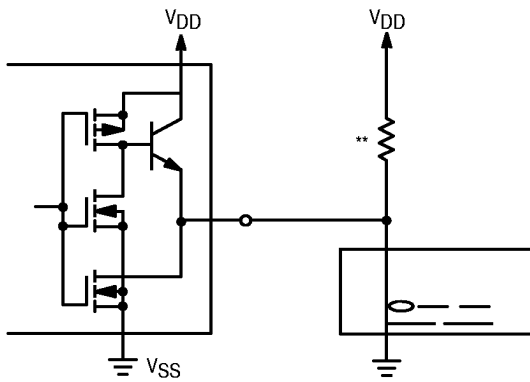
Figure 2. Dynamic Signal Waveforms

CONNECTIONS TO VARIOUS DISPLAY READOUTS

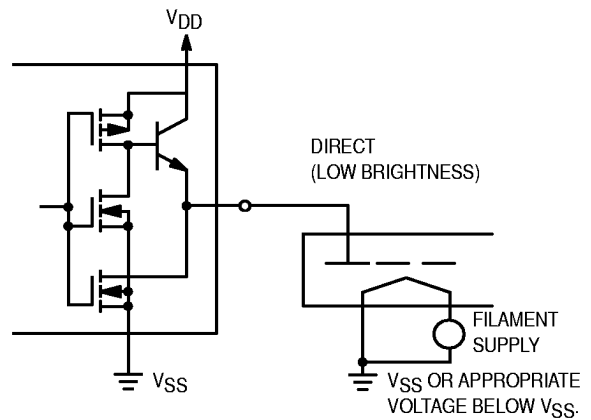
LIGHT EMITTING DIODE (LED) READOUT



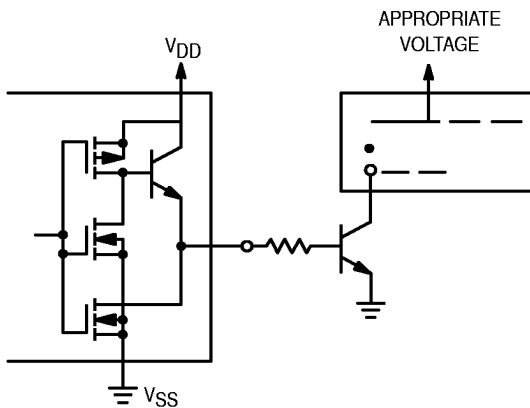
INCANDESCENT READOUT



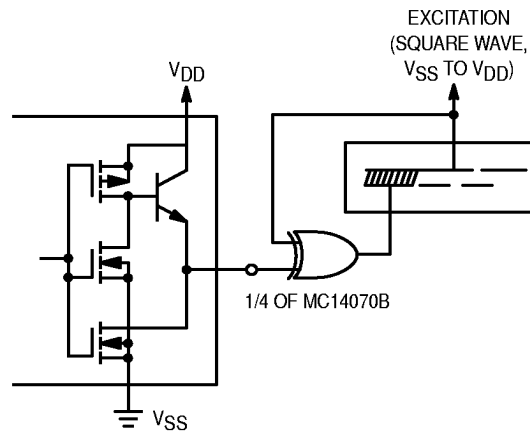
FLUORESCENT READOUT



GAS DISCHARGE READOUT



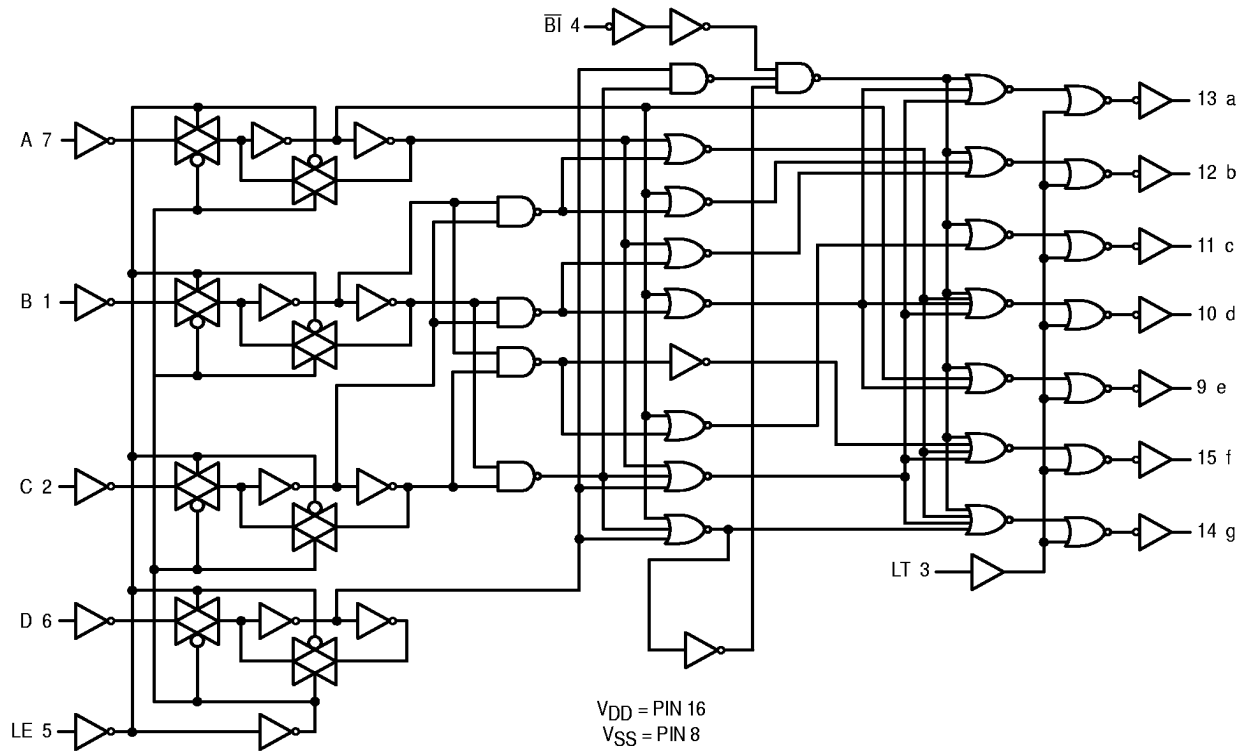
LIQUID CRYSTAL (LCD) READOUT



** A filament pre-warm resistor is recommended to reduce filament thermal shock and increase the effective cold resistance of the filament.

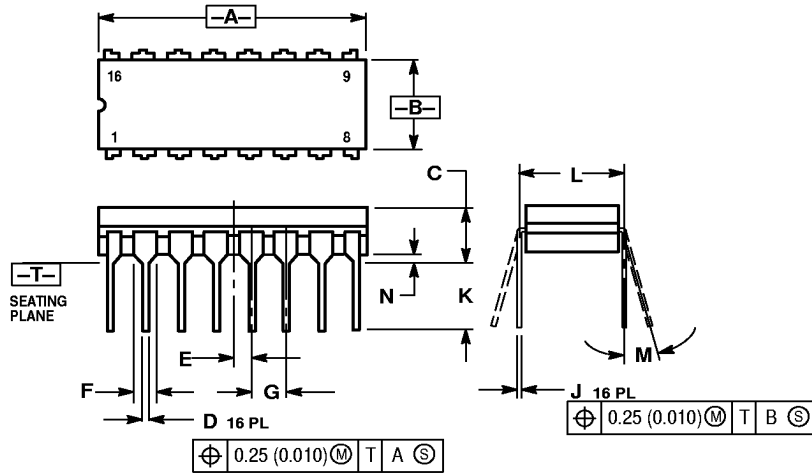
Direct dc drive of LCD's not recommended for life of LCD readouts.

LOGIC DIAGRAM



OUTLINE DIMENSIONS

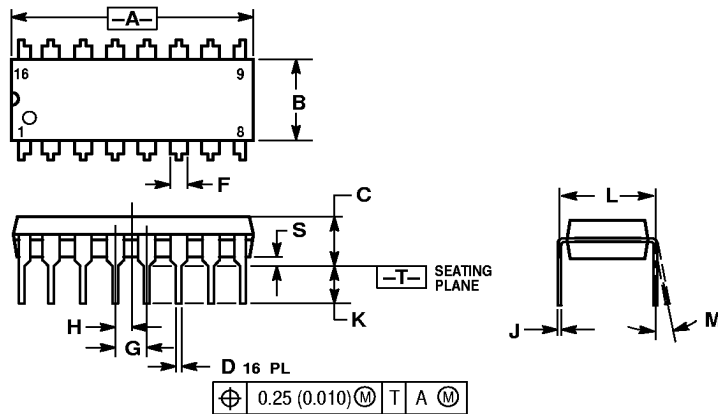
L SUFFIX CERAMIC DIP PACKAGE CASE 620-10 ISSUE V



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
 4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.750 | 0.785 | 19.05 | 19.93 |
| B | 0.240 | 0.295 | 6.10 | 7.49 |
| C | — | 0.200 | — | 5.08 |
| D | 0.015 | 0.020 | 0.39 | 0.50 |
| E | 0.050 BSC | | 1.27 BSC | |
| F | 0.055 | 0.065 | 1.40 | 1.65 |
| G | 0.100 BSC | | 2.54 BSC | |
| H | 0.008 | 0.015 | 0.21 | 0.38 |
| K | 0.125 | 0.170 | 3.18 | 4.31 |
| L | 0.300 BSC | | 7.62 BSC | |
| M | 0° | 15° | 0° | 15° |
| N | 0.020 | 0.040 | 0.51 | 1.01 |

P SUFFIX PLASTIC DIP PACKAGE CASE 648-08 ISSUE R

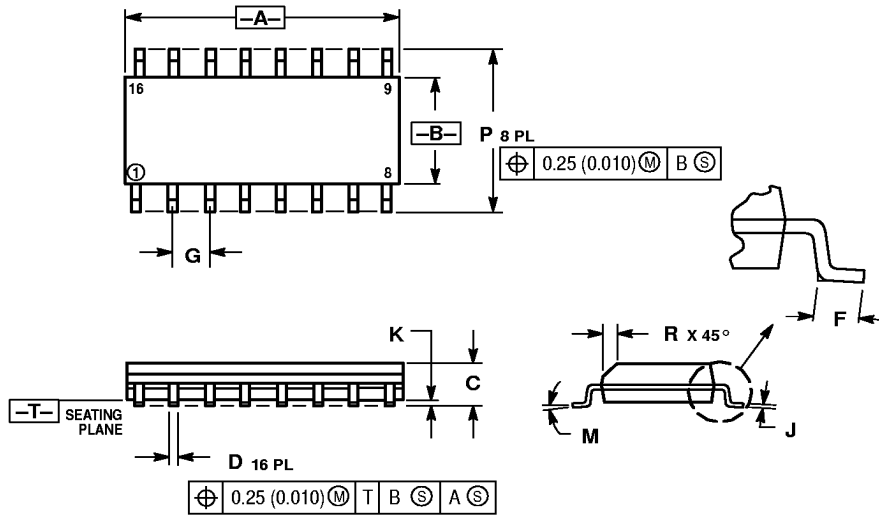


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
 4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
 5. ROUNDED CORNERS OPTIONAL.

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.740 | 0.770 | 18.80 | 19.55 |
| B | 0.250 | 0.270 | 6.35 | 6.85 |
| C | 0.145 | 0.175 | 3.69 | 4.44 |
| D | 0.015 | 0.021 | 0.39 | 0.53 |
| F | 0.040 | 0.70 | 1.02 | 1.77 |
| G | 0.100 BSC | | 2.54 BSC | |
| H | 0.050 BSC | | 1.27 BSC | |
| J | 0.008 | 0.015 | 0.21 | 0.38 |
| K | 0.110 | 0.130 | 2.80 | 3.30 |
| L | 0.295 | 0.305 | 7.50 | 7.74 |
| M | 0° | 10° | 0° | 10° |
| S | 0.020 | 0.040 | 0.51 | 1.01 |

OUTLINE DIMENSIONS

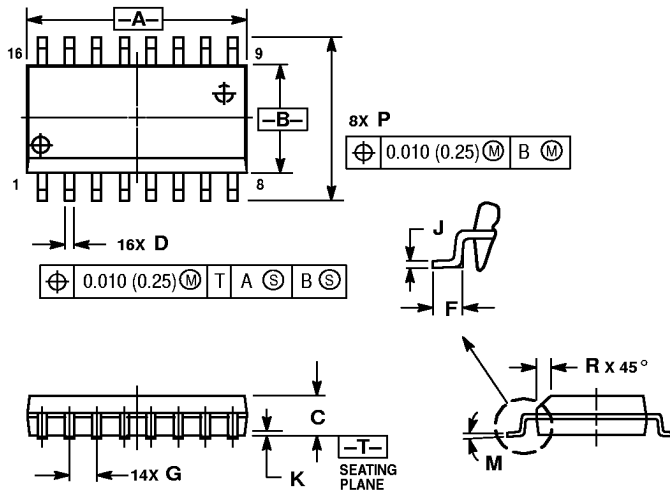
D SUFFIX PLASTIC SOIC PACKAGE CASE 751B-05 ISSUE J



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|-------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 9.80 | 10.00 | 0.386 | 0.393 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.054 | 0.068 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.40 | 1.25 | 0.016 | 0.049 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.19 | 0.25 | 0.008 | 0.009 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | 0° | 7° | 0° | 7° |
| P | 5.80 | 6.20 | 0.229 | 0.244 |
| R | 0.25 | 0.50 | 0.010 | 0.019 |

DW SUFFIX PLASTIC SOIC PACKAGE CASE 751G-02 ISSUE A



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|-------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 10.15 | 10.45 | 0.400 | 0.411 |
| B | 7.40 | 7.60 | 0.292 | 0.299 |
| C | 2.35 | 2.65 | 0.093 | 0.104 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.50 | 0.90 | 0.020 | 0.035 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.25 | 0.32 | 0.010 | 0.012 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | 0° | 7° | 0° | 7° |
| P | 10.05 | 10.55 | 0.395 | 0.415 |
| R | 0.25 | 0.75 | 0.010 | 0.029 |