Data Sheet | March 4, 2002 | FN7296

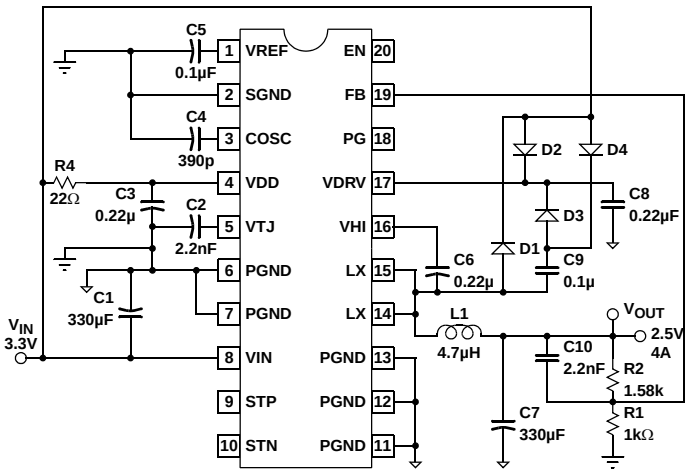
Monolithic 4 Amp DC:DC Step-Down Regulator

The EL7563 is an integrated, full-featured synchronous step-down regulator with output voltage adjustable from 1.0V to 2.5V. It is capable of delivering 4A continuous current at up to 95% efficiency. The EL7563 operates at a constant frequency pulse width modulation (PWM) mode, making external synchronization possible. Patented on-chip resistorless current sensing enables current mode control, which provides cycle-by-cycle current limiting, over-current protection, and excellent step load response. The EL7563 features power tracking, which makes the start-up sequencing of multiple converters possible. A junction temperature indicator conveniently monitors the silicon die temperature, saving the designer time on the tedious thermal characterization. The minimal external components and full functionality make this EL7563 ideal for desktop and portable applications.

The EL7563 is specified for operation over the full -40°C to +85°C temperature range.

Pinout

EL7563
(20-PIN SO)
TOP VIEW



Typical Application Diagrams continued on page 3

Manufactured Under U.S. Patent No. 5,7323,974

Features

- Integrated synchronous MOSFETs and current mode controller
- 4A continuous output current
- Up to 95% efficiency
- Internal patented current sense
- Cycle-by-cycle current limit
- 3V to 3.6V input voltage
- Adjustable output voltage 1V to 2.5V
- Precision reference
- ±0.5% load and line regulation
- Adjustable switching frequency to 1MHz
- Oscillator synchronization possible
- Internal soft-start
- Over-voltage protection
- Junction temperature indicator
- Over-temperature protection
- Under-voltage lockout
- Multiple supply start-up tracking
- Power-good indicator
- 20-pin SO (0.300”) package
- 28-pin HTSSOP package

Applications

- DSP, CPU core, and I/O supplies
- Logic/Bus supplies
- Portable equipment
- DC:DC converter modules
- GTL + Bus power supply

Ordering Information

PART NUMBER	PACKAGE	TAPE & REEL	PKG. NO.
EL7563CM	20-Pin SO (0.300”)	-	MDP0027
EL7563CM-T13	20-Pin SO (0.300”)	13”	MDP0027
EL7563CRE-T7	28-Pin HTSSOP	7”	MDP0048
EL7563CRE-T13	28-Pin HTSSOP	13”	MDP0048

Absolute Maximum Ratings (T_A = 25°C)

Supply Voltage between V_{IN} or V_{DD} and GND . . . . . +4.5V
V_{LX} Voltage . . . . . V_{IN} +0.3V
Input Voltage . . . . . GND -0.3V, V_{DD} +0.3V
V_{HI} Voltage . . . . . GND -0.3V, V_{LX} +6V

Storage Temperature . . . . . -65°C to +150°C
Operating Ambient Temperature . . . . . -40°C to +85°C
Operating Junction Temperature . . . . . +135°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

DC Electrical Specifications

$V_{DD} = V_{IN} = 3.3V$, $T_A = T_J = 25°C$, $C_{OSC} = 1.2nF$, unless otherwise specified.

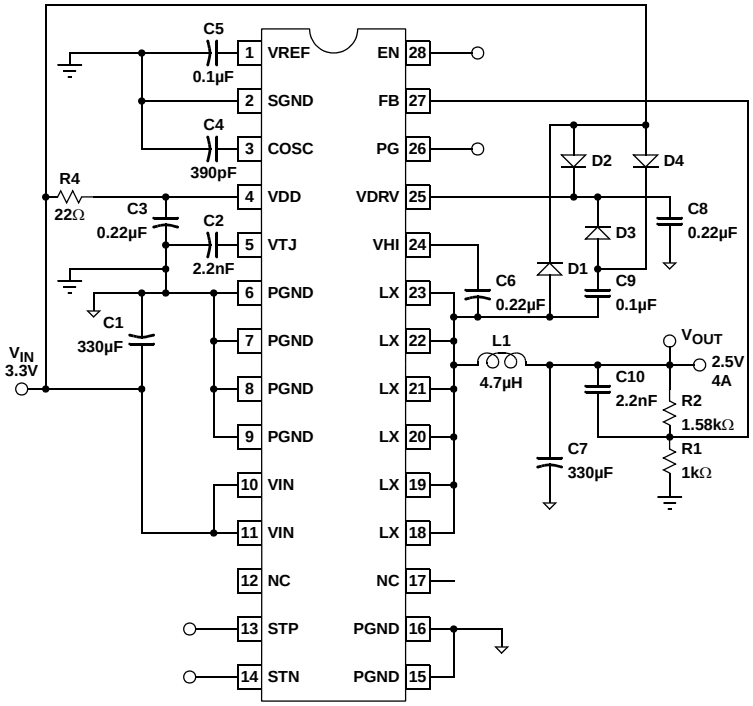
PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
V_{REF}	Reference Accuracy		1.24	1.26	1.28	V
V_{REFTC}	Reference Temperature Coefficient			50		ppm/°C
$V_{REFLOAD}$	Reference Load Regulation	$0 < I_{REF} < 50\mu A$	-1			%
V_{RAMP}	Oscillator Ramp Amplitude			1.15		V
I_{OSC_CHG}	Oscillator Charge Current	$0.1V < V_{OSC} < 1.25V$		200		µA
I_{OSC_DIS}	Oscillator Discharge Current	$0.1V < V_{OSC} < 1.25V$		8		mA
$I_{VDD}+V_{DRV}$	$V_{DD}+V_{DRV}$ Supply Current	$V_{EN} = 2.7V$, $F_{OSC} = 120kHz$	2	3.5	5	mA
I_{VDD_OFF}	V_{DD} Standby Current	EN = 0		1	1.5	mA
V_{DD_OFF}	V_{DD} for Shutdown		2.4		2.65	V
V_{DD_ON}	V_{DD} for Startup		2.6		2.95	V
T_{OT}	Over Temperature Threshold			135		°C
T_{HYS}	Over Temperature Hysteresis			20		°C
I_{LEAK}	Internal FET Leakage Current	EN = 0, L_X = 3.3V (low FET), L_X = 0V (high FET)			10	µA
I_{LMAX}	Peak Current Limit		5			A
R_{DSON}	FET On Resistance	Wafer level test only		30	60	mΩ
R_{DSONTC}	R_{DSON} Tempco			0.2		mΩ/°C
I_{STP}	Auxilliary Supply Tracking Positive Input Pull Down Current	$V_{STP} = V_{IN}/2$	-4	2.5		µA
I_{STN}	Auxilliary Supply Tracking Negative Input Pull Up Current	$V_{STN} = V_{IN}/2$		2.5	4	µA
V_{PGP}	Positive Power Good Threshold	With respect to target output voltage	8		16	%
V_{PGN}	Negative Power Good Threshold	With respect to target output voltage	-16		-8	%
V_{PG_HI}	Power Good Drive High	I_{PG} = 1mA	2.7			V
V_{PG_LO}	Power Good Drive Low	I_{PG} = -1mA			0.5	V
V_{OVP}	Over Voltage Protection			10		%
V_{FB}	Output Initial Accuracy	I_{LOAD} = 0A	0.977	0.992	1.007	V
V_{FB_LINE}	Output Line Regulation	$V_{IN} = 3.3V$, $\Delta V_{IN} = 10\%$, I_{LOAD} = 0A		0.5		%
V_{FB_LOAD}	Output Load Regulation	$0.5A < I_{LOAD} < 4A$		0.5		%
V_{FB_TC}	Output Temperature Stability	$-40°C < T_A < 85°C$, I_{LOAD} = 2A		±1		%
I_{FB}	Feedback Input Pull Up Current	V_{FB} = 0V		100	200	nA
V_{EN_HI}	EN Input High Level				2.7	V
V_{EN_LO}	EN Input Low Level		1			V
I_{EN}	Enable Pull Up Current	V_{EN} = 0	-4	-2.5		µA

Closed-Loop AC Electrical Specifications

$V_S = V_{IN} = 3.3V$, $T_A = T_J = 25°C$, $C_{OSC} = 1.2nF$, unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
F_{OSC}	Oscillator Initial Accuracy		100	115	125	kHz
t_{SYNC}	Minimum Oscillator Sync Width			25		ns
M_{SS}	Soft Start Slope			0.5		V/ms
t_{BRM}	FET Break Before Make Delay			15		ns
t_{LEB}	High Side FET Minimum On Time			150		ns
D_{MAX}	Maximum Duty Cycle			95		%

Typical Application Diagrams (Continued)



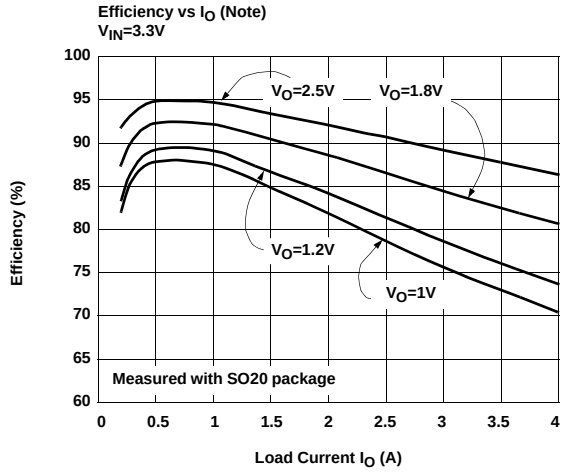
28-Pin HTSSOP

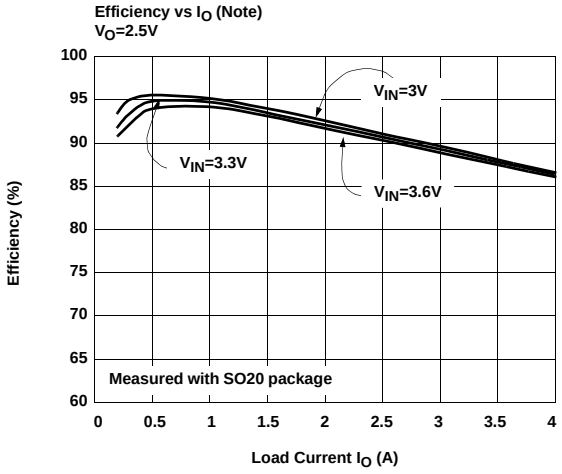
Pin Descriptions

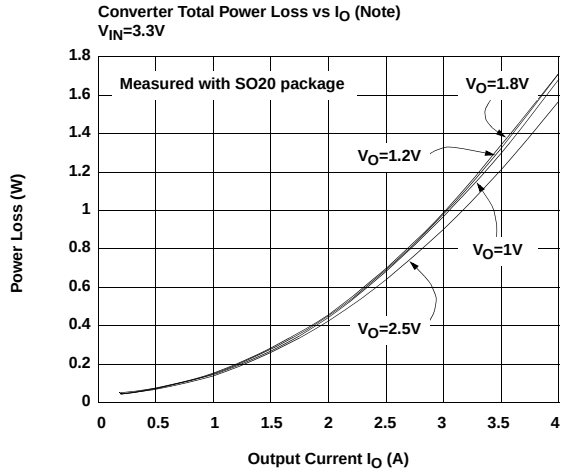
PIN NUMBER	PIN NAME	PIN FUNCTION
1	VREF	Bandgap reference bypass capacitor; typically 0.1µF to SGND
2	SGND	Control circuit negative supply or signal ground
3	COSC	Oscillator timing capacitor (see performance curves)
4	VDD	Control circuit positive supply; normally connected to VIN through an RC filter
5	VTJ	Junction temperature monitor; connected with 2.2nF to 3.3nF to SGND
6	PGND	Ground return of the regulator; connected to the source of the low-side synchronous NMOS power FET
7	PGND	Ground return of the regulator; connected to the source of the low-side synchronous NMOS power FET
8	VIN	Power supply input of the regulator; connected to the drain of the high-side NMOS power FET
9	STP	Auxilliary supply tracking positive input; tied to regulator output to synchronize start up with a second supply; leave open for stand alone operation; 2µA internal pull down current
10	STN	Auxilliary supply tracking negative input; connect to output of a second supply to synchronize start up; leave open for stand alone operation; 2µA internal pull up current
11	PGND	Ground return of the regulator; connected to the source of the low-side synchronous NMOS power FET
12	PGND	Ground return of the regulator; connected to the source of the low-side synchronous NMOS power FET
13	PGND	Ground return of the regulator; connected to the source of the low-side synchronous NMOS power FET
14	LX	Inductor drive pin; high current output whose average voltage equals the regulator output voltage
15	LX	Inductor drive pin; high current output whose average voltage equals the regulator output voltage
16	VHI	Positive supply of high-side driver; boot strapped from VDRV to LX with an external 0.22µF capacitor
17	VDRV	Positive supply of low-side driver and input voltage for high side boot strap
18	PG	Power good window comparator output; logic 1 when regulator output is within ±10% of target output voltage
19	FB	Voltage feedback input; connected to external resistor divider between VOUT and SGND; a 125nA pull-up current forces VOUT to SGND in the event that FB is floating
20	EN	Chip enable, active high; a 2µA internal pull up current enables the device if the pin is left open; a capacitor can be added at this pin to delay the start of converter

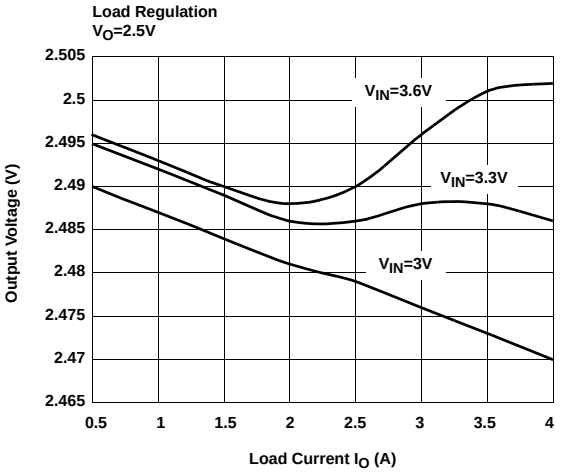
Typical Performance Curves (20-Pin SO Package)

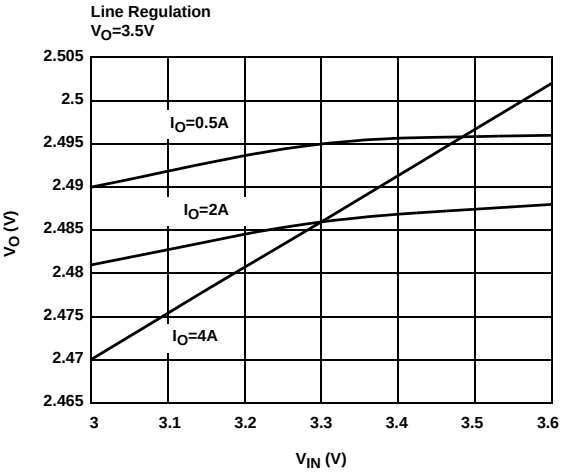
NOTE: The 28-Pin HTSSOP Package Offers Improved Performance

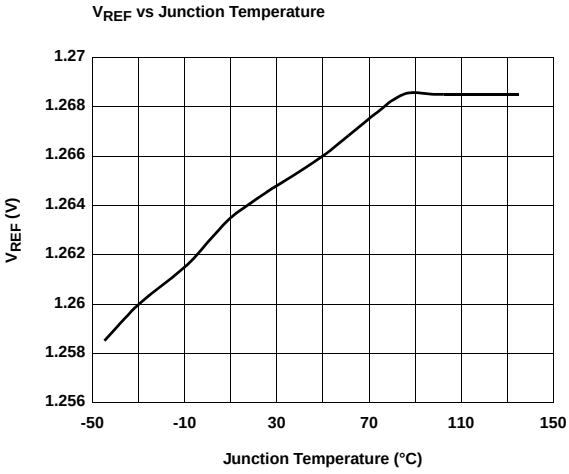








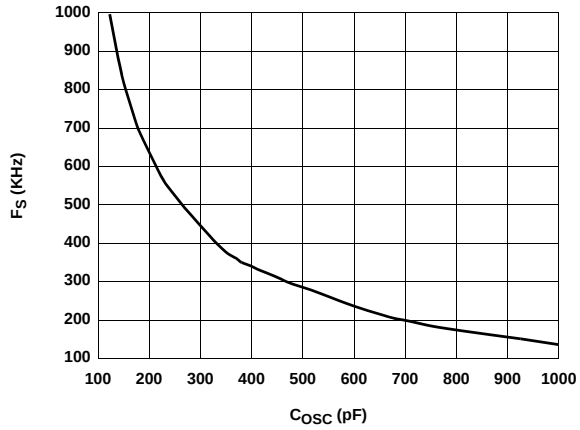




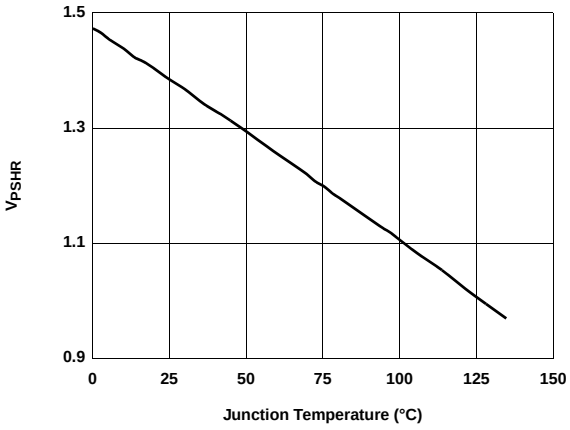
Typical Performance Curves (20-Pin SO Package) (Continued)

NOTE: The 28-Pin HTSSOP Package Offers Improved Performance

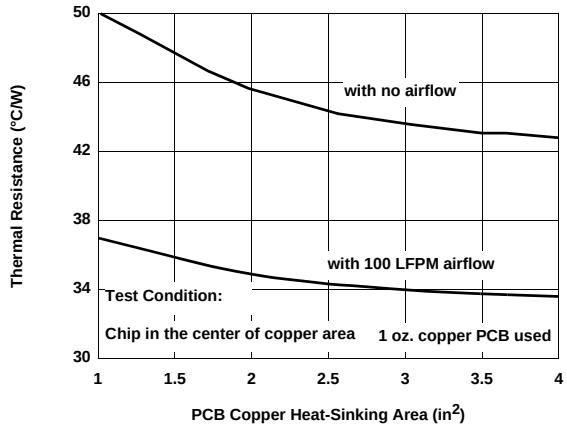
Switching Frequency vs C_{OSC}



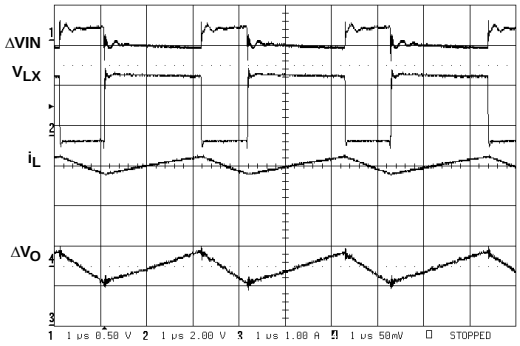
VTJ vs Junction Temperature



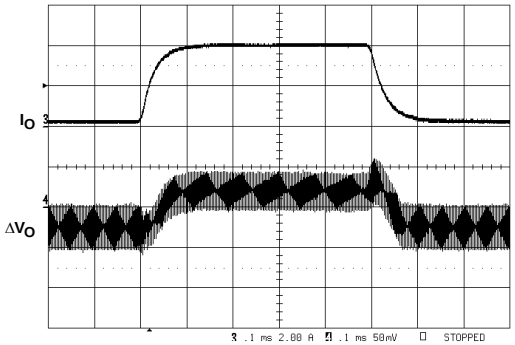
θ_{JA} vs Copper Area (Note)
SO20 Package



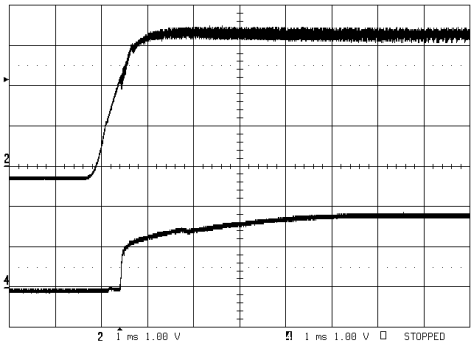
Switching Waveforms
V_{IN}=3.3V, V_O=1.8V, I_O=4A



Transient Response
V_{IN}=3.3V, V_O=1.8V, I_O=0.2A-4A

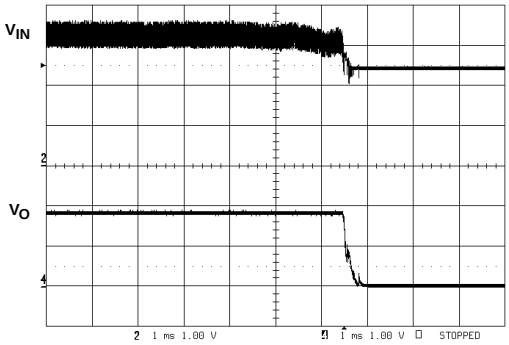


Power-Up
V_{IN}=3.3V, V_O=1.8V, I_O=0.2A

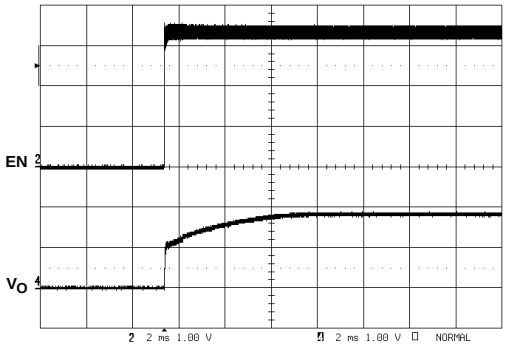


Typical Performance Curves (20-Pin SO Package) (Continued)

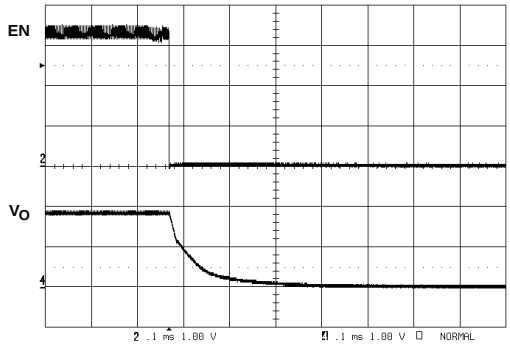
Power-Down
V_{IN}=3.3V, V_O=1.8V, I_O=4A



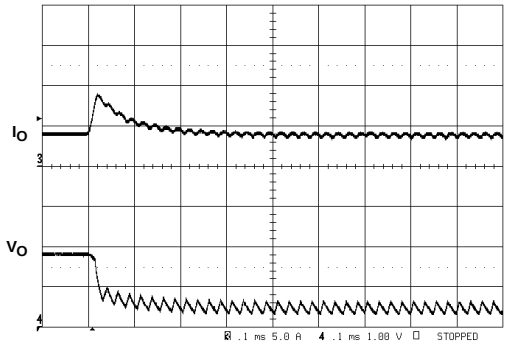
Enable
V_{IN}=3.3V, V_O=1.8V at 4A



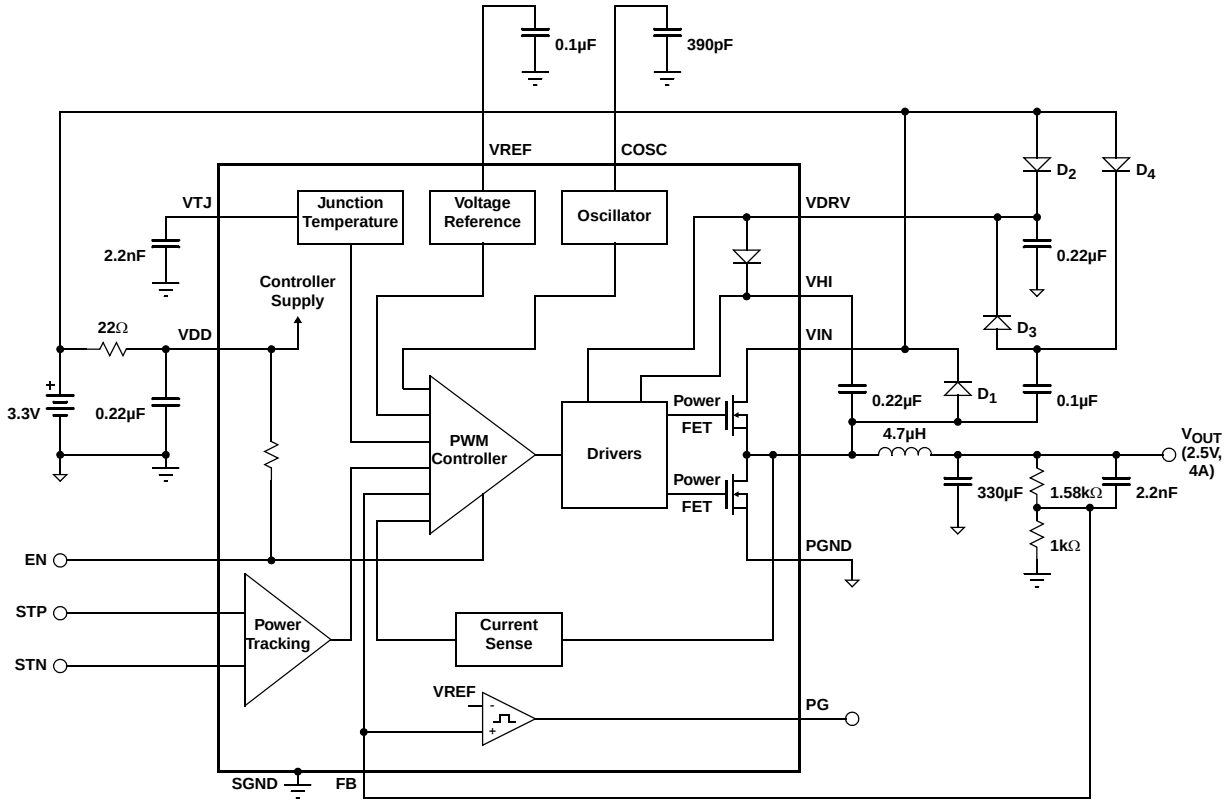
Disable
V_{IN}=3.3V, V_O=1.8V at 4A



Short-Circuit Protection
V_{IN}=3.3V, V_O=1.8V, I_O=4A to short



Block Diagram



Applications Information

Circuit Description

General

The EL7563 is a fixed frequency, current mode controlled DC:DC converter with integrated N-channel power MOSFETs and a high precision reference. The device incorporates all the active circuitry required to implement a cost effective, user-programmable 4A synchronous step-down regulator suitable for use in DSP core power supplies. By combining fused-lead packaging technology with an efficient synchronous switching architecture, high power output (10W) can be realized without the use of discrete external heat sinks.

Theory of Operation

The EL7563 is composed of 7 major blocks:

1. PWM Controller
2. NMOS Power FETs and Drive Circuitry
3. Bandgap Reference
4. Oscillator
5. Temperature Sensor
6. Power Good and Power On Reset
7. Auxiliary Supply Tracking

PWM Controller

The EL7563 regulates output voltage through the use of current-mode controlled pulse width modulation. The three main elements in a PWM controller are the feedback loop and reference, a pulse width modulator whose duty cycle is controlled by the feedback error signal, and a filter which averages the logic level modulator output. In a step-down (buck) converter, the feedback loop forces the time-averaged output of the modulator to equal the desired output voltage. Unlike pure voltage-mode control systems, current-mode control utilizes dual feedback loops to provide both output voltage and inductor current information to the controller. The voltage loop minimizes DC and transient errors in the output voltage by adjusting the PWM duty-cycle in response to changes in line or load conditions. Since the output voltage is equal to the time-averaged of the modulator output, the relatively large LC time constant found in power supply applications generally results in low bandwidth and poor transient response. By directly monitoring changes in inductor current via a series sense resistor the controller's response time is not entirely limited by the output LC filter and can react more quickly to changes in line and load conditions. This feed-forward characteristic also simplifies AC loop compensation since it adds a zero to the overall loop response. Through proper selection of the current-feedback to voltage-feedback ratio the overall loop response will approach a one-pole system. The resulting system offers

several advantages over traditional voltage control systems, including simpler loop compensation, pulse by pulse current limiting, rapid response to line variation and good load step response.

The heart of the controller is an input direct summing comparator which sum voltage feedback, current feedback, slope compensation ramp and power tracking signals together. Slope compensation is required to prevent system instability that occurs in current-mode topologies operating at duty-cycles greater than 50% and is also used to define the open-loop gain of the overall system. The slope compensation is fixed internally and optimized for 500mA inductor ripple current. The power tracking will not contribute any input to the comparator steady-state operation. Current feedback is measured by the patented sensing scheme that senses the inductor current flowing through the high-side switch whenever it is conducting. At the beginning of each oscillator period the high-side NMOS switch is turned on. The comparator inputs are gated off for a minimum period of time of about 150ns (LEB) after the high-side switch is turned on to allow the system to settle. The Leading Edge Blanking (LEB) period prevents the detection of erroneous voltages at the comparator inputs due to switching noise. If the inductor current exceeds the maximum current limit (ILMAX) a secondary over-current comparator will terminate the high-side switch on time. If ILMAX has not been reached, the feedback voltage FB derived from the regulator output voltage VOUT is then compared to the internal feedback reference voltage. The resultant error voltage is summed with the current feedback and slope compensation ramp. The high-side switch remains on until all four comparator inputs have summed to zero, at which time the high-side switch is turned off and the low-side switch is turned on. However, the maximum on-duty ratio of the high-side switch is limited to 95%. In order to eliminate cross-conduction of the high-side and low-side switches a 15ns break-before-make delay is incorporated in the switch drive circuitry. The output enable (EN) input allows the regulator output to be disabled by an external logic control signal.

Output Voltage Setting

In general:

$$V_{OUT} = 0.992V \times \left(1 + \frac{R_2}{R_1}\right)$$

However, due to the relatively low open loop gain of the system, gain errors will occur as the output voltage and loop-gain is changed. This is shown in the performance curves. A 100nA pull-up current from FB to VDD forces VOUT to GND in the event that FB is floating.

NMOS Power FETs and Drive Circuitry

The EL7563 integrates low on-resistance (30mΩ) NMOS FETs to achieve high efficiency at 4A. In order to use an NMOS switch for the high-side drive it is necessary to drive the gate voltage above the source voltage (LX). This is accomplished by bootstrapping the VHI pin above the LX voltage with an external capacitor CVHI and internal switch and diode. When the low-side switch is turned on and the LX voltage is close to GND potential, capacitor CVHI is charged through internal switch to VDRV, typically 6V with external charge-pump. At the beginning of the next cycle the high-side switch turns on and the LX pins begin to rise from GND to VIN potential. As the LX pin rises the positive plate of capacitor CVHI follows and eventually reaches a value of VDRV+VIN, typically 9V, for VIN=3.3V. This voltage is then level shifted and used to drive the gate of the high-side FET, via the VHI pin. A value of 0.22µF for CVHI is recommended.

Reference

A 1.5% temperature compensated bandgap reference is integrated in the EL7563. The external VREF capacitor acts as the dominant pole of the amplifier and can be increased in size to maximize transient noise rejection. A value of 0.1µF is recommended.

Oscillator

The system clock is generated by an internal relaxation oscillator with a maximum duty-cycle of approximately 95%. Operating frequency can be adjusted through the COSC pin or can be driven by an external source. If the oscillator is driven by an external source care must be taken in selecting the ramp amplitude. Since CSLOPE value is derived from the COSC ramp, changes to COSC ramp will change the CSLOPE compensation ramp which determine the open-loop gain of the system.

When external synchronization is required, always choose C_{OSC} such that the free-running frequency is at least 20% lower than that of sync source to accommodate component and temperature variations. Figure 1 shows a typical connection.

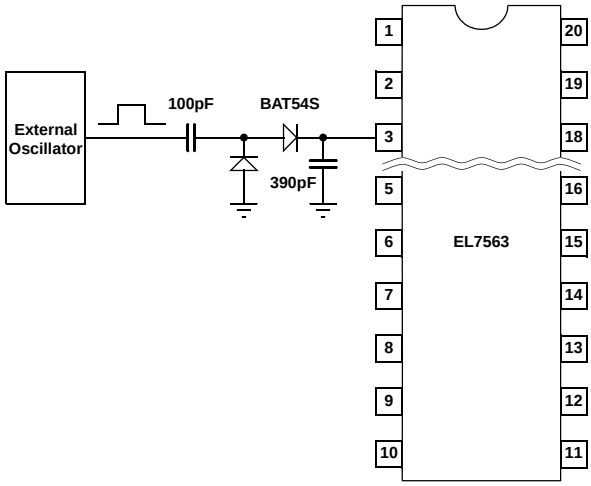


FIGURE 1. OSCILLATOR SYNCHRONIZATION

Junction Temperature Sensor

An internal temperature sensor continuously monitors die temperature. In the event that die temperature exceeds the thermal trip-point, the system is in fault state and will be shut down. The upper and low trip-points are set to 135°C and 115°C respectively.

The VTJ pin is an accurate indication of the internal silicon junction temperature (see performance curve.) The junction temperature T_J (°C) can be deducted from the following relation:

$$T_J = 75 + \frac{1.2 - VTJ}{0.00384}$$

Where VTJ is the voltage at VTJ pin in volts.

Power Good and Power On Reset

During power up the output regulator will be disabled until VIN reaches a value of approximately 2.9V. About 300mV hysteresis is present to eliminate noise-induced oscillations.

Under-voltage and over-voltage conditions on the regulator output are detected through an internal window comparator. A logic high on the PG output indicates that the regulated output voltage is within about +10% of the nominal selected output voltage.

Power Tracking

The power tracking pins STP and STN are the inputs to a comparator, whose HI output forces the PWM controller to skip switching cycle.

1. Linear Tracking

In this application, it is always the case that the lower voltage supply V_C tracks the higher output supply V_P. Please see Figure 2 below.

2. Offset Tracking

The intended start-up sequence is shown in Figure 3. In this configuration, V_C will not start until V_P reaches a preset value of:

$$\frac{R_B}{R_A + R_B} \times V_{IN}$$

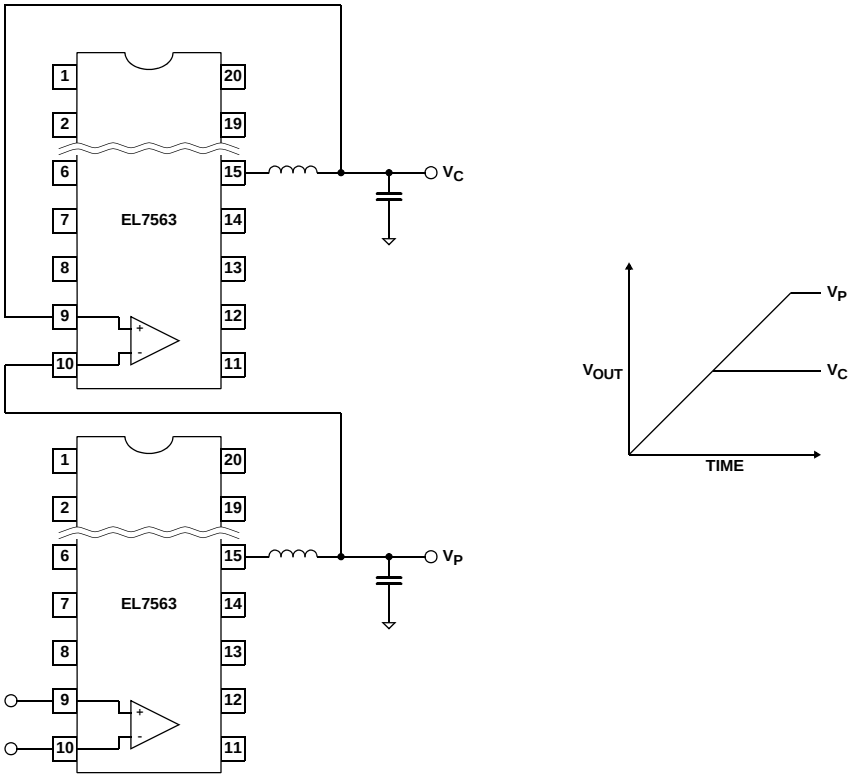


FIGURE 2. LINEAR POWER TRACKING

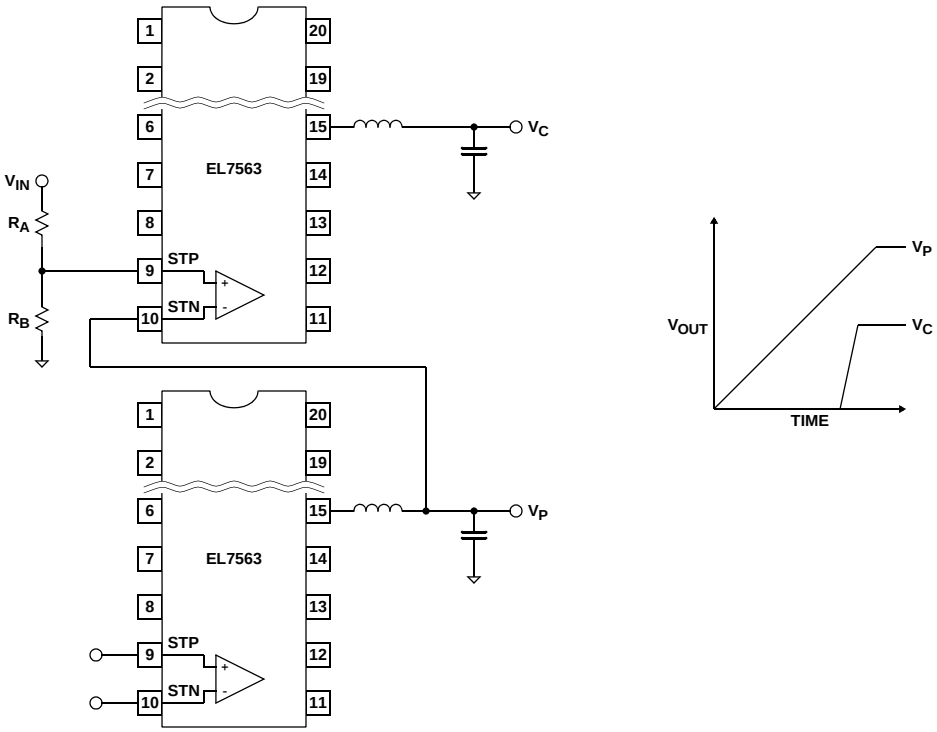


FIGURE 3. OFFSET POWER TRACKING

The second way of offset tracking is to use the EN and Power Good pins, as shown in Figure 4. In this configuration, V_P does not have to be larger than V_C.

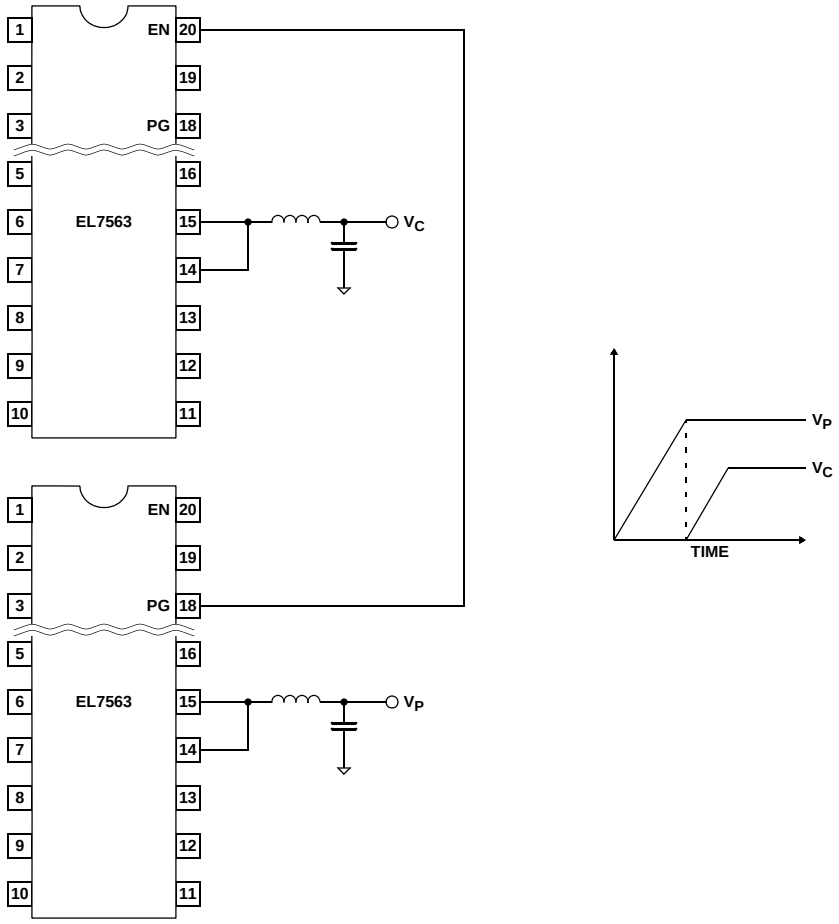


FIGURE 4. OFFSET TRACKING

3. External Soft Start

An external soft start can be combined with auxilliary supply tracking to provide desired soft start other than internally preset soft start (Figure 5). The appropriate start-up time is:

$$t_S = R \times C \times \frac{V_O}{V_{IN}}$$

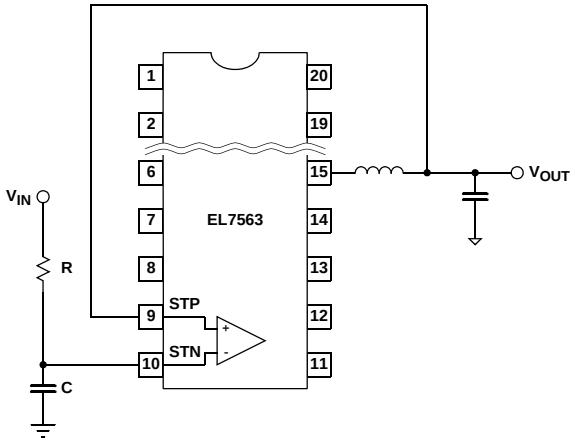


FIGURE 5. EXTERNAL SOFT START

4. Start-up Delay

A capacitor can be added to the EN pin to delay the converter start-up (Figure 6) by utilizing the pull-up current. The delay time is approximately:

$$t_d(ms) = 1200 \times C(\mu F)$$

Thermal Management

The EL7563CM utilizes “fused lead” packaging technology in conjunction with the system board layout to achieve a lower thermal resistance than typically found in standard SO20 packages. By fusing (or connecting) multiple external leads to the die substrate within the package, a very conductive heat path is created to the outside of the package. This conductive heat path MUST then be connected to a heat sinking area on the PCB in order to dissipate heat out and away from the device. The conductive paths for the SO20 package are the fused leads: # 6, 7, 11, 12, and 13. If a sufficient amount of PCB metal area is connected to the fused package leads, a junction-to-ambient resistance of 43°C/W can be achieved (compared to 85°C/W for a standard SO20 package). The general relationship between PCB heat-sinking metal area and the thermal resistance for this package is shown in the Performance Curves section of this data sheet. It can be readily seen that the thermal resistance for this package approaches an asymptotic value of approximately 43°C/W without any airflow, and 33°C/W with 100 LFPM airflow. Additional information can be found in Application Note #8 (Measuring the Thermal Resistance of Power Surface-Mount Packages). For a thermal shutdown die junction temperature of 135°C, and power dissipation of 1.5W, the ambient temperature can be as high as 70°C without airflow. With 100 LFPM airflow, the ambient temperature can be extended to 85°C.

The EL7563CRE utilizes the 28-pin HTSSOP package. The majority of heat is dissipated through the heat pad exposed at the bottom of the package. Therefore, the heat pad needs to be soldered to the PCB. The thermal resistance for this package is better than that of the SO20. Actual test results

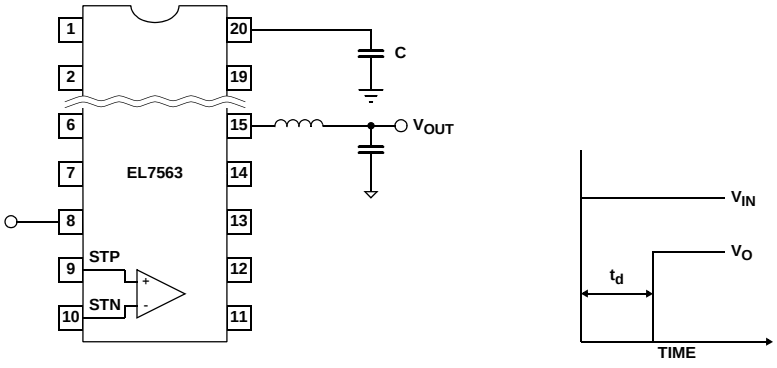


FIGURE 6. START-UP DELAY

are available from Elantec Applications staff. The actual junction temperature can be measured at VTJ pin.

Since the thermal performance of the IC is heavily dependent on the board layout, the system designer should exercise care during the design phase to ensure that the IC will operate under the worst-case environmental conditions.

Layout Considerations

The layout is very important for the converter to function properly. Power Ground (⏚) and Signal Ground (⏚) should be separated to ensure that the high pulse current in the Power Ground never interferes with the sensitive signals connected to Signal Ground. They should only be connected at one point (normally at the negative side of either the input or output capacitor.)

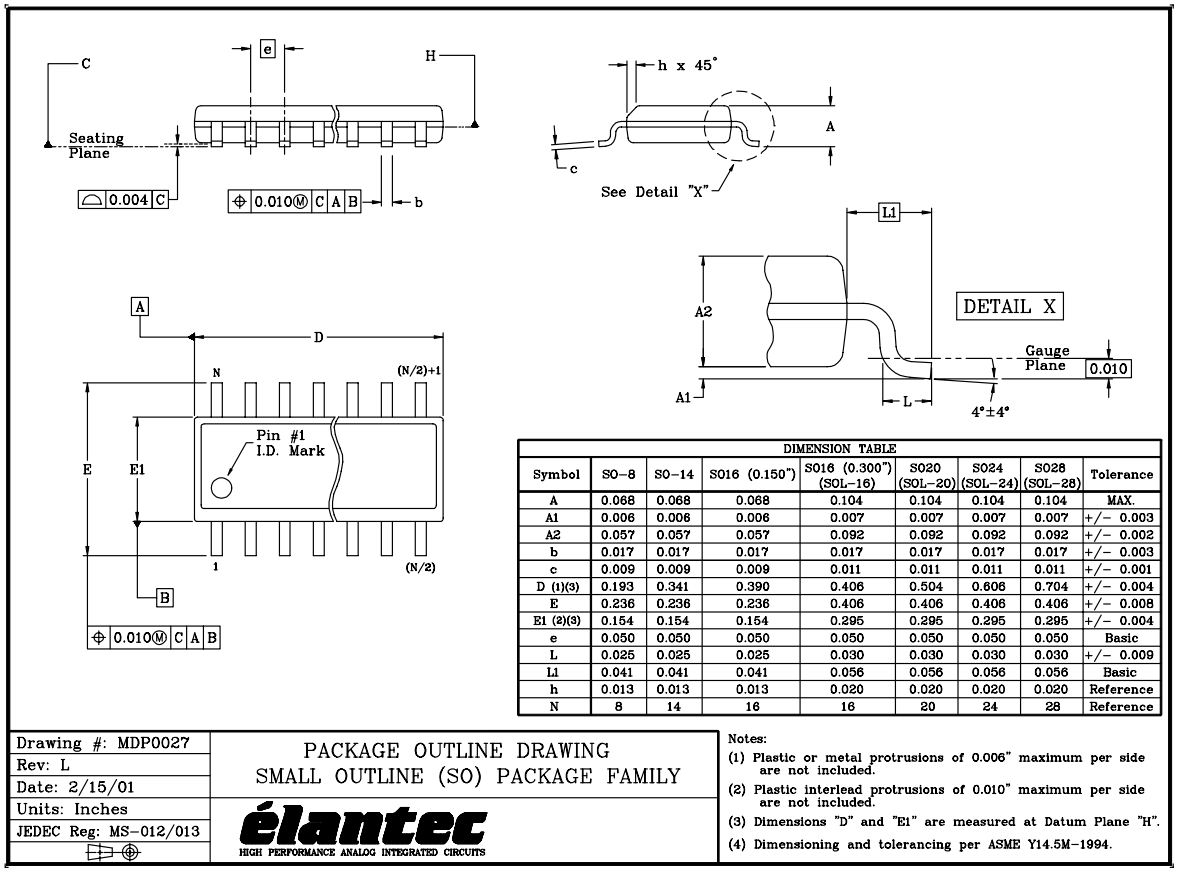
The trace connected to the FB pin is the most sensitive trace. It needs to be as short as possible and in a “quiet” place, preferably between PGND or SGND traces.

In addition, the bypass capacitor connected to the VDD pin needs to be as close to the pin as possible.

The heat of the chip is mainly dissipated through the PGND pins. Maximizing the copper area around these pins is preferable. In addition, a solid ground plane is always helpful for the EMI performance.

The demo board is a good example of layout based on these principles. Please refer to the EL7563 Application Brief for the layout.

Package Outline Drawing



DIMENSION TABLE								
Symbol	SO-8	SO-14	SO16 (0.150")	SO16 (0.300") (SOL-16)	SO20 (SOL-20)	SO24 (SOL-24)	SO28 (SOL-28)	Tolerance
A	0.068	0.068	0.068	0.104	0.104	0.104	0.104	MAX.
A1	0.006	0.006	0.006	0.007	0.007	0.007	0.007	+/- 0.003
A2	0.057	0.057	0.057	0.092	0.092	0.092	0.092	+/- 0.002
b	0.017	0.017	0.017	0.017	0.017	0.017	0.017	+/- 0.003
c	0.009	0.009	0.009	0.011	0.011	0.011	0.011	+/- 0.001
D (1)(3)	0.193	0.341	0.390	0.406	0.504	0.606	0.704	+/- 0.004
E	0.236	0.236	0.236	0.406	0.406	0.406	0.406	+/- 0.008
E1 (2)(3)	0.154	0.154	0.154	0.295	0.295	0.295	0.295	+/- 0.004
e	0.050	0.050	0.050	0.050	0.050	0.050	0.050	Basic
L	0.025	0.025	0.025	0.030	0.030	0.030	0.030	+/- 0.009
L1	0.041	0.041	0.041	0.056	0.056	0.056	0.056	Basic
h	0.013	0.013	0.013	0.020	0.020	0.020	0.020	Reference
N	8	14	16	16	20	24	28	Reference

Drawing #: MDP0027	PACKAGE OUTLINE DRAWING SMALL OUTLINE (SO) PACKAGE FAMILY	Notes: (1) Plastic or metal protrusions of 0.006" maximum per side are not included. (2) Plastic interlead protrusions of 0.010" maximum per side are not included. (3) Dimensions "D" and "E1" are measured at Datum Plane "H". (4) Dimensioning and tolerancing per ASME Y14.5M-1994.
Rev: L		
Date: 2/15/01		
Units: Inches		
JEDEC Reg: MS-012/013	élantec HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS	

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