

Features

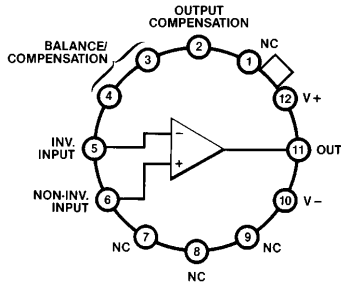
- 500 V/ μ s slew rate
- 70 MHz bandwidth
- $10^{12}\Omega$ input impedance
- 5 mV max. input offset voltage
- FET input
- Offset nulls with single pot
- No compensation required for gains above 50
- Peak output current to 100 mA
- MIL-STD-883 devices 100% manufactured in U.S.A.

Ordering Information

Part No.	Temp. Range	Pkg.	Outline #
ELH0032G/883B	-55°C to +125°C	TO-8	MDP0002

8001301ZX is the SMD version of this device.

Connection Diagram



Top View

Case is electrically isolated.

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Manufactured under U.S. Patent No. 4,746,877

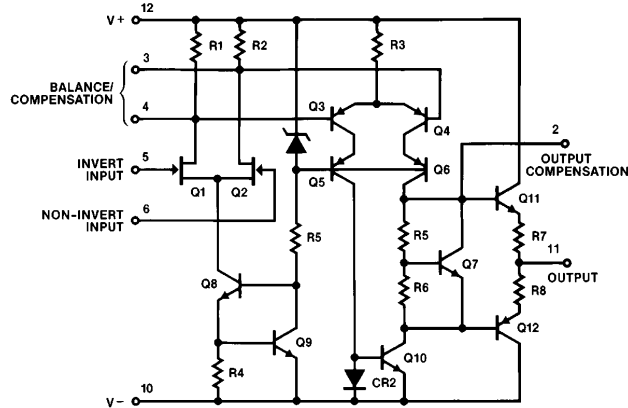
General Description

The ELH0032 is a high slew rate, high input impedance differential operational amplifier suitable for diverse application in fast signal handling. The high allowable differential input voltage, ease of output clamping, and high output drive capability make the ELH0032 particularly suitable for comparator applications. It may be used in applications normally reserved for video amplifiers allowing the use of operational gain setting and frequency response shaping into the megahertz region.

The ELH0032's wide bandwidth, high input impedance and high output drive capability make it an ideal choice for applications such as summing amplifiers in high-speed D to A's, buffers in data acquisition systems, and sample and hold circuits. Additional applications include high-speed integrators and video amplifiers. The ELH0032 is guaranteed over the temperature range -55°C to +125°C.

Elantec facilities comply with MIL-I-45208A and other applicable quality specifications. Elantec's Military devices are 100% fabricated and assembled in our rigidly controlled, ultra-clean facilities in Milpitas, California. For additional information on Elantec's Quality and Reliability Assurance policy and procedures request brochure QRA-1.

Simplified Schematic



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Note: All information contained in this data sheet has been carefully checked and is believed to be accurate as of the date of publication; however, this data sheet cannot be a "controlled document". Current revisions, if any, to these specifications are maintained at the factory and are available upon your request. We recommend checking the revision level before finalization of your design documentation. CMS # 0032DS

ELH0032G/883/8001301ZX

Fast Operational Amplifier

Absolute Maximum Ratings

V_S	Supply Voltage	$\pm 18V$	T_A	Operating Temperature Range:	
V_{IN}	Input Voltage	$\pm 15 V_S$		ELH0032	$-55^{\circ}C$ to $+125^{\circ}C$
	Differential Input Voltage	$\pm 30V$ or $\pm 2 V_S$	T_J	Operating Junction Temperature	$175^{\circ}C$
P_D	Power Dissipation (Note 1)		T_{ST}	Storage Temperature	$-65^{\circ}C$ to $+150^{\circ}C$
	$T_A = 25^{\circ}C$	1.5W, derate $100^{\circ}C/W$ to $+125^{\circ}C$		Lead Temperature	
	$T_C = 25^{\circ}C$	2.2W, derate $70^{\circ}C/W$ to $+125^{\circ}C$		(Soldering, 10 seconds)	$300^{\circ}C$

Important Note:

All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at $T_A = 25^{\circ}C$ and QA sample tested at $T_A = 25^{\circ}C$, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at $T_A = 25^{\circ}C$ for information purposes only.

DC Electrical Characteristics $V_S = \pm 15V$, $T_{MIN} \leq T_A \leq T_{MAX}$, $V_{IN} = 0V$

Parameter	Description	Test Conditions	ELH0032				Units
			Min	Typ	Max	Test Level	
V_{OS}	Input Offset Voltage	$T_J = 25^{\circ}C$ (Note 2)		2	5	I	mV
					10	I	mV
$\Delta V_{OS}/\Delta T$	Average Offset Voltage Drift			25	150	I	$\mu V/^{\circ}C$
I_{OS}	Input Offset Current	$T_J = 25^{\circ}C$ (Note 2)			25	I	pA
		$T_A = 25^{\circ}C$ (Note 3)			250	IV	pA
		$T_J = Max$			25	I	nA
I_B	Input Bias Current	$T_J = 25^{\circ}C$ (Note 2)			100	I	pA
		$T_A = 25^{\circ}C$ (Note 3)			1	IV	nA
		$T_J = T_{MAX}$			50	I	nA
V_{INCM}	Input Voltage Range		± 10	± 12		I	V
CMRR	Common-Mode Rejection Ratio	$V_{IN} = \pm 10V$	50	60		I	dB
A_{VOL}	Open-Loop Voltage Gain	$V_O = \pm 10V$, $R_L = 1 k\Omega$, $T_J = 25^{\circ}C$	48	60		I	dB
		$V_O = \pm 10V$, $R_L = 1 k\Omega$	45			I	dB
		$V_O = \pm 10V$, $f = 1 kHz$, $R_L = 1 k\Omega$, $T_J = 25^{\circ}C$	60	70		I	dB
		$V_O = \pm 10V$, $f = 1 kHz$, $R_L = 1 k\Omega$	57			I	dB

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DC Electrical Characteristics $V_S = \pm 15V, T_{MIN} \leq T_A \leq T_{MAX}, V_{IN} = 0V$ — Contd.

Parameter	Description	Test Conditions	ELH0032				Units
			Min	Typ	Max	Test Level	
V_O	Output Voltage Swing	$R_L = 1\text{ k}\Omega$	± 10	± 13.5		I	V
I_S	Power Supply Current	$T_J = 25^\circ\text{C}, I_O = 0\text{ mA}$		21	23	I	mA
		$T_A = 25^\circ\text{C}, I_O = 0\text{ mA}$ (Note 3)		18	20	IV	mA
PSRR	Power Supply Rejection Ratio	$\pm 5V \leq V_S \leq 15V$	50	60		I	dB
		$+5V \leq V_S(+) \leq +20V,$ $V_S(-) = -15V$	50			I	dB
		$-5V \geq V_S(-) \geq -20V,$ $V_S(+) = +15V$	50			I	dB

AC Electrical Characteristics $V_S = \pm 15V, R_L = 1\text{ k}\Omega, T_J = 25^\circ\text{C}$

Parameter	Description	Test Conditions	Min	Typ	Max	Test Level	Units
SR	Slew Rate	$A_V = +1, \Delta V_{IN} = 20V$	350	500		I	$V/\mu\text{s}$
t_S	Settling Time to 1% of Final Value	$A_V = -1, \Delta V_{IN} = 20V$		100	500	IV	ns
t_S	Settling Time to 0.1% of Final Value	$A_V = -1, \Delta V_{IN} = 20V$		300		V	ns
t_R	Small Signal Rise Time	$A_V = +1, \Delta V_{IN} = 1V$		8	20	I	ns
t_D	Small Signal Delay Time	$A_V = +1, \Delta V_{IN} = 1V$		10	25	I	ns

Note 1: In order to limit maximum junction temperature to $+175^\circ\text{C}$, it may be necessary to operate with $V_S < \pm 15V$ when T_A or T_C exceeds specific values depending on the P_D within the device package. Total P_D is the sum of quiescent and load-related dissipation.

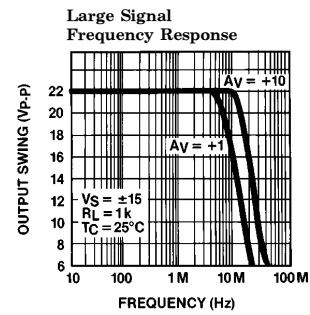
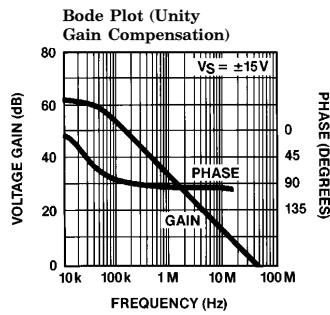
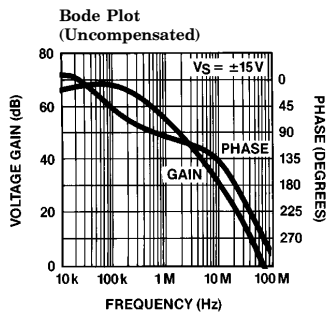
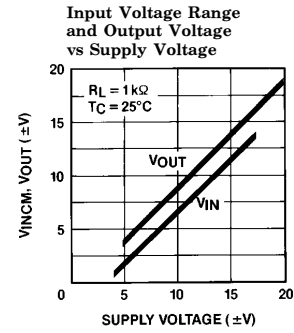
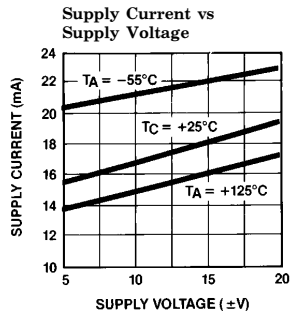
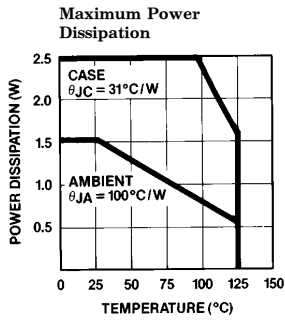
Note 2: Specification is at 25°C junction temperature due to requirements of high-speed automatic testing. Actual values at operating temperature will exceed the value at $T_J = 25^\circ\text{C}$. When supply voltage are $\pm 15V$, no-load operating junction temperature may rise 40°C – 60°C above ambient and more under load conditions. Accordingly, V_{OS} may change one to several mV, and I_B and I_{OS} will change significantly during warm-up. Refer to I_B and I_{OS} vs temperature graph for expected values.

Note 3: Measured in still air 7 minutes after application of power.

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Typical Performance Curves

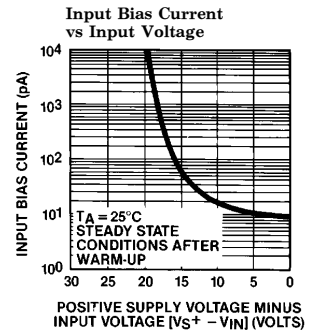
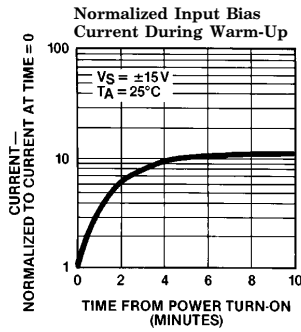
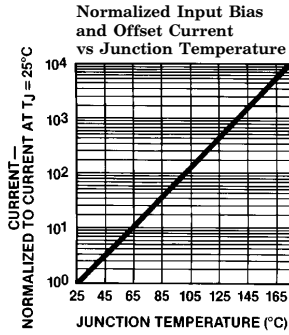
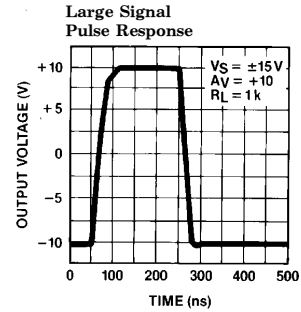
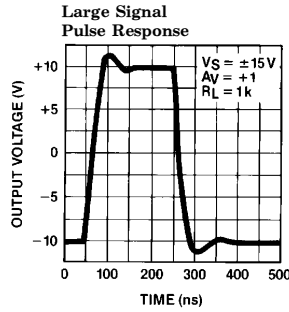
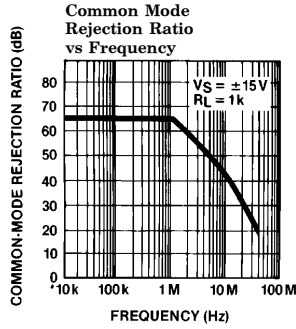


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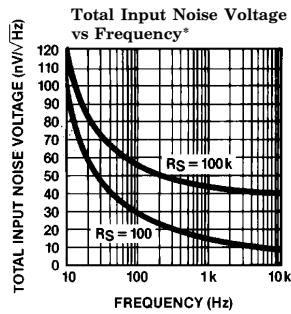
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Fast Operational Amplifier

Typical Performance Curves — Contd.



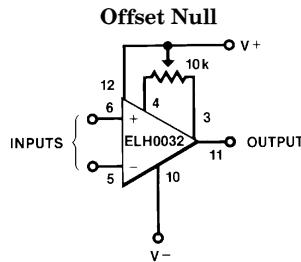
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0032-5

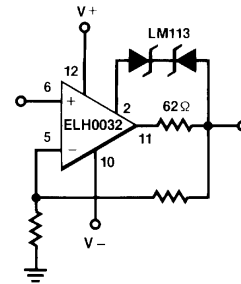
*Noise voltage includes contribution from source resistance.

Auxiliary Circuits



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Output Short Circuit Protection



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Applications Information

Power Supply Decoupling

The ELH0032, like most high-speed circuits, is sensitive to layout and stray capacitance. Power supplies should be bypassed as near to pins 10 and 12 as possible with low inductance capacitors such as 0.01 μF disc ceramics. Compensation components should also be located close to the appropriate pins to minimize stray reactances.

Input Current

Because the input devices are FETs, the input bias current may be expected to double for each 11°C junction temperature rise. This characteristic is plotted in the typical performance characteristics graphs. The device will self-heat due to internal power dissipation after application of power, thus raising the FET junction temperature 40°C–60°C above the free-air ambient temperature when supplies are $\pm 15\text{V}$. The device temperature will stabilize within 5–10 minutes after application of power, and the input bias currents measured at the time will be indicative of normal operating currents. An additional rise will occur as power is delivered to a load due to additional internal power dissipation.

There is an additional effect on input bias current as the input voltage is changed. The effect, common to all FETs, is an avalanche-like increase in gate current as the FET gate-to-drain voltage is increased above a critical value, depending on FET geometry and doping levels. This effect will be noted as the input voltage of the ELH0032 is taken below ground potential when the supplies are $\pm 15\text{V}$. All of the effects described here may be minimized by operating the device with $V_S \leq \pm 15\text{V}$.

These effects are indicated in the typical performance curves.

Input Capacitance

The input capacitance to the ELH0032 is typically 5 pF and thus may form a significant time constant with high value resistors. For optimum performance, the input capacitance to the inverting input should be compensated by a small capacitor across the feedback resistor. The value is strongly dependent on layout and closed loop gain, but will typically be in the neighborhood of several picofarads.

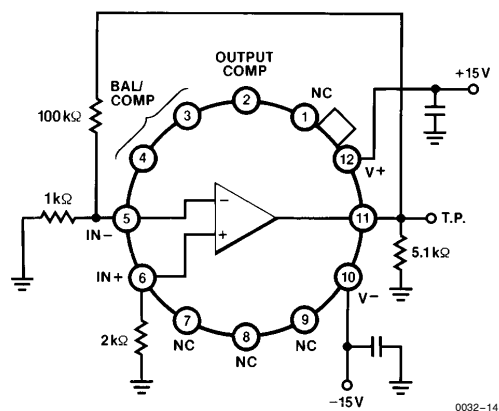
In the non-inverting configuration, it may be advantageous to bootstrap the case and/or a guard conductor to the inverting input. This serves both to divert leakage currents away from the non-inverting input and to reduce the effective input capacitance. A unity gain follower so treated will have an input capacitance under a 1 pF.

Heatsinking

While the ELH0032 is specified for operation without any explicit heatsink, internal power dissipation does cause a significant temperature rise. Improved bias current performance can thus be obtained by limiting this temperature rise with a small heat sink such as the Thermalloy No. 2241 or equivalent. The case of the device has no internal connection, so it may be electrically connected to the sink if this is advantageous. Be aware, however, that this will affect the stray capacitances to all pins and may thus require adjustment of circuit compensation values.

Burn-In Circuit

(Functional Diagram)



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ELH0032 Macromodel

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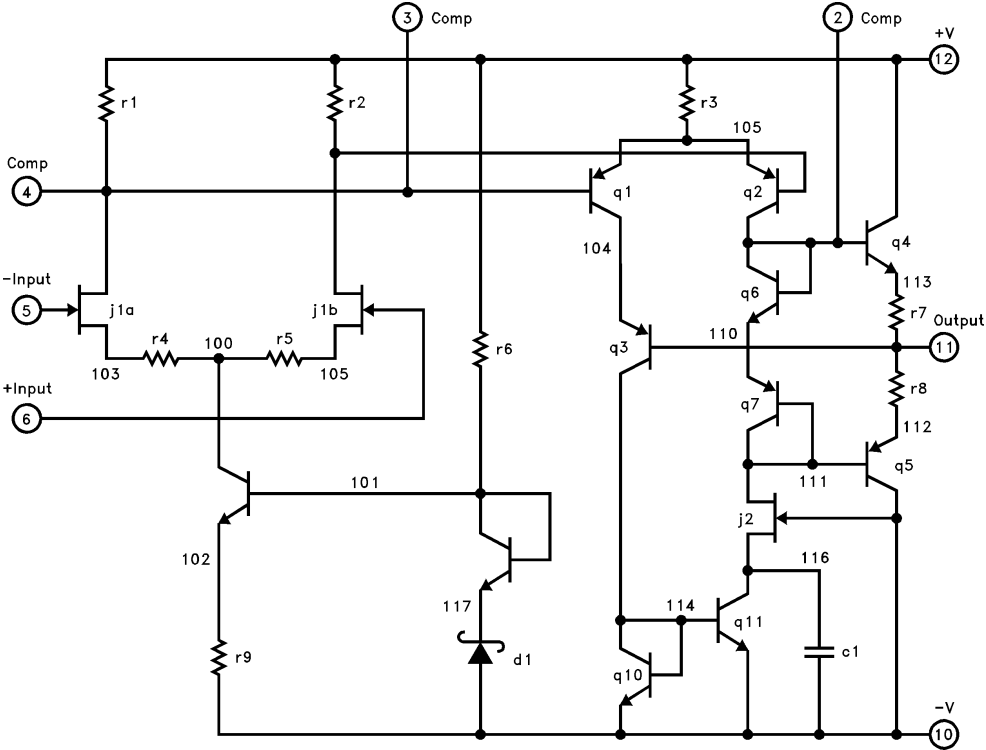
* Connections:
+ input
*
*      - input
*
*      + Vsupply
*      - Vsupply
*      Comp 3
*      Comp 4
*      Comp 2
*      Output
*
.subckt M0032 6 5 12 10 3 4 2 11
* Models
.model qfa njf (vto = -2.5V beta = 1.11e-3 cgd = 2pF cgs = 5pF m = 0.3744)
.model qp pnp (is = 5e-14 bf = 150 vaf = 100 ikf = 100mA tf = .53nS vtf = 0 ise = 1nA
+ cjc = 4pF cje = 5.7pF tr = 170nS rb = 3 br = 5 mje = .32 mjc = .43 xtb = 2.1 ne = 4
+ isc = 1nA nc = 4 itf = .4 vtf = 4 xtf = 6)
.model qn npn (is = 5e-14 bf = 150 vaf = 800 ikf = 200mA tf = .53nS vtf = 0
+ cjc = 4pF cje = 5pF rb = 3 br = 5 mje = .42 MJC = .23 tr = 200nS xtb = 2.1
+ ise = 4nA ne = 4 isc = 4nA nc = 4 itf = .4 vtf = 4 xtf = 2)
.model qfb njf (vto = -2.8V beta = 4e-3 cgd = 7pF cgs = 8pF lambda = 4e-3)
.model zener d (bv = 2.49V ibv = 1mA)
* Resistors and Capacitors
r1 12 4 700
r2 12 3 700
r3 12 105 160
r4 103 100 10
r5 108 100 10
r6 12 101 22K
r7 113 11 10
r8 11 112 10
r9 102 10 407
cs2 10 116 100pF
* Transistors and Diodes
j1a 4 5 103 qfa
j1b 3 6 108 qfa
j2 111 10 116 qfb
q1 104 4 105 qp
q2 2 3 105 qp
q3 114 11 104 qp
q4 12 2 113 qn
q5 10 111 112 qp
q6 2 2 110 qn
q7 111 111 110 qp
q8 100 101 102 qn
d1 10 117 zener
q9 101 101 117 qn
q10 114 114 10 qn
q11 116 114 10 qn
.ends

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ELH0032G/883/8001301ZX

Fast Operational Amplifier

ELH0032 Macromodel — Contd.



0032-15

BLANK

BLANK

ELH0032G/883/8001301ZX

Fast Operational Amplifier

General Disclaimer

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