

## FCB11N60

### 600V N-Channel MOSFET

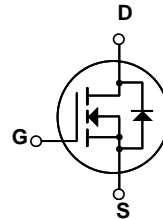
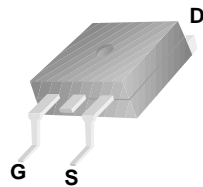
#### Features

- 650V @ $T_J = 150^\circ\text{C}$
- Typ.  $R_{DS(on)} = 0.32\Omega$
- Ultra low gate charge (typ.  $Q_g = 40\text{nC}$ )
- Low effective output capacitance (typ.  $C_{OSS,eff} = 95\text{pF}$ )
- 100% avalanche tested

#### Description

SuperFET™ is, Fairchild's proprietary, new generation of high voltage MOSFET family that is utilizing an advanced charge balance mechanism for outstanding low on-resistance and lower gate charge performance.

This advanced technology has been tailored to minimize conduction loss, provide superior switching performance, and withstand extreme  $dv/dt$  rate and higher avalanche energy. Consequently, SuperFET is very suitable for various AC/DC power conversion in switching mode operation for system miniaturization and higher efficiency.



#### Absolute Maximum Ratings

Symbol	Parameter	FCB11N60	Unit
$V_{DSS}$	Drain-Source Voltage	600	V
$I_D$	Drain Current - Continuous ( $T_C = 25^\circ\text{C}$ ) - Continuous ( $T_C = 100^\circ\text{C}$ )	11 7	A A
$I_{DM}$	Drain Current - Pulsed (Note 1)	33	A
$V_{GSS}$	Gate-Source voltage	$\pm 30$	V
$E_{AS}$	Single Pulsed Avalanche Energy (Note 2)	340	mJ
$I_{AR}$	Avalanche Current (Note 1)	11	A
$E_{AR}$	Repetitive Avalanche Energy (Note 1)	12.5	mJ
$dv/dt$	Peak Diode Recovery $dv/dt$ (Note 3)	4.5	V/ns
$P_D$	Power Dissipation ( $T_C = 25^\circ\text{C}$ ) - Derate above $25^\circ\text{C}$	125 1.0	W W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
$T_L$	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

#### Thermal Characteristics

Symbol	Parameter	FCB11N60	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	1.0	$^\circ\text{C}/\text{W}$
$R_{\theta JA}^*$	Thermal Resistance, Junction-to-Ambient*	40	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62.5	$^\circ\text{C}/\text{W}$

\* When mounted on the minimum pad size recommended (PCB Mount)

## Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FCB11N60	FCB11N60	D <sup>2</sup> -PAK	330mm	24m	800

## Electrical Characteristics T<sub>C</sub> = 25°C unless otherwise noted

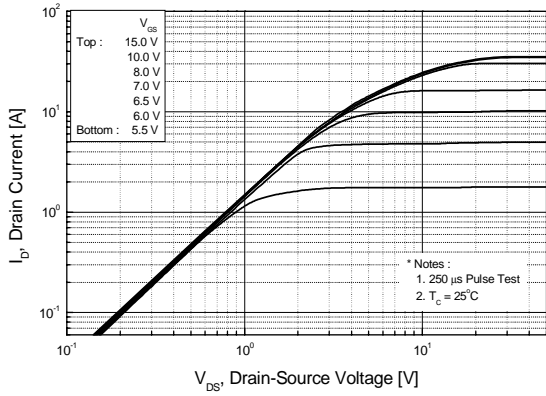
Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>Off Characteristics</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA, T <sub>J</sub> = 25°C	600	--	--	V
		V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA, T <sub>J</sub> = 150°C	--	650	--	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250μA, Referenced to 25°C	--	0.6	--	V/°C
BV <sub>DS</sub>	Drain-Source Avalanche Breakdown Voltage	V <sub>GS</sub> = 0V, I <sub>D</sub> = 11A	--	700	--	V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 600V, V <sub>GS</sub> = 0V	--	--	1	μA
		V <sub>DS</sub> = 480V, T <sub>C</sub> = 125°C	--	--	10	μA
I <sub>GSSF</sub>	Gate-Body Leakage Current, Forward	V <sub>GS</sub> = 30V, V <sub>DS</sub> = 0V	--	--	100	nA
I <sub>GSSR</sub>	Gate-Body Leakage Current, Reverse	V <sub>GS</sub> = -30V, V <sub>DS</sub> = 0V	--	--	-100	nA
<b>On Characteristics</b>						
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA	3.0	--	5.0	V
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> = 10V, I <sub>D</sub> = 5.5A	--	0.32	0.38	Ω
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 40V, I <sub>D</sub> = 5.5A (Note 4)	--	9.7	--	S
<b>Dynamic Characteristics</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 25V, V <sub>GS</sub> = 0V, f = 1.0MHz	--	1148	1490	pF
C <sub>oss</sub>	Output Capacitance		--	671	870	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		--	63	--	pF
C <sub>oss</sub>	Output Capacitance	V <sub>DS</sub> = 480V, V <sub>GS</sub> = 0V, f = 1.0MHz	--	35	--	pF
C <sub>oss eff.</sub>	Effective Output Capacitance	V <sub>DS</sub> = 0V to 400V, V <sub>GS</sub> = 0V	--	95	--	pF
<b>Switching Characteristics</b>						
t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = 300V, I <sub>D</sub> = 11A R <sub>G</sub> = 25Ω	--	34	80	ns
t <sub>r</sub>	Turn-On Rise Time		--	98	205	ns
t <sub>d(off)</sub>	Turn-Off Delay Time		--	119	250	ns
t <sub>f</sub>	Turn-Off Fall Time		(Note 4, 5)	--	56	120
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> = 480V, I <sub>D</sub> = 11A V <sub>GS</sub> = 10V	--	40	52	nC
Q <sub>gs</sub>	Gate-Source Charge		--	7.2	--	nC
Q <sub>gd</sub>	Gate-Drain Charge		(Note 4, 5)	--	21	--
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current		--	--	11	A
I <sub>SM</sub>	Maximum Pulsed Drain-Source Diode Forward Current		--	--	33	A
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	V <sub>GS</sub> = 0V, I <sub>S</sub> = 11A	--	--	1.4	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0V, I <sub>S</sub> = 11A di <sub>f</sub> /dt = 100A/μs (Note 4)	--	390	--	ns
Q <sub>rr</sub>	Reverse Recovery Charge		--	5.7	--	μC

### Notes:

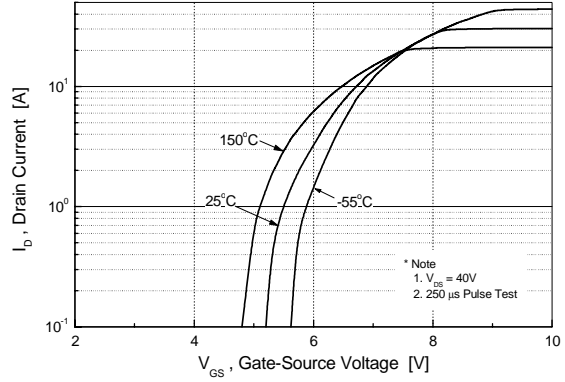
1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. I<sub>AS</sub> = 11A, V<sub>DD</sub> = 50V, R<sub>G</sub> = 25Ω, Starting T<sub>J</sub> = 25°C
3. I<sub>SD</sub> ≤ 11A, di<sub>f</sub>/dt ≤ 200A/μs, V<sub>DD</sub> ≤ BV<sub>DSS</sub>, Starting T<sub>J</sub> = 25°C
4. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
5. Essentially Independent of Operating Temperature Typical Characteristics

## Typical Performance Characteristics

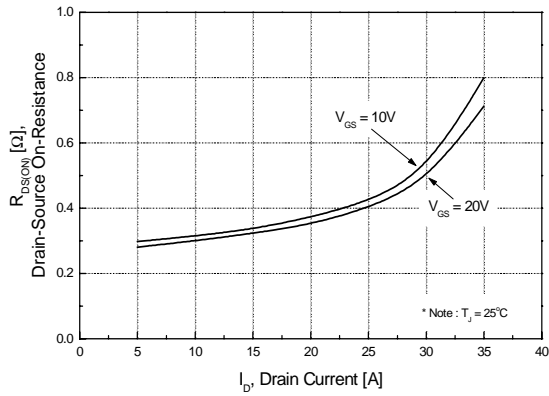
**Figure 1. On-Region Characteristics**



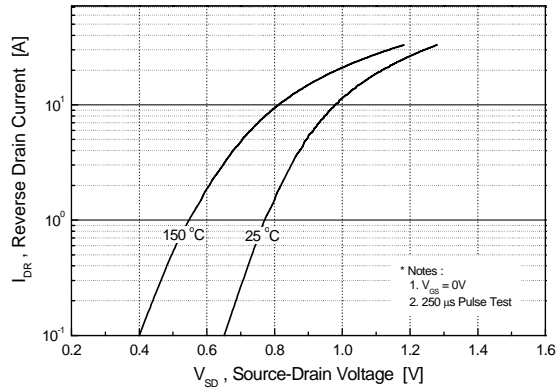
**Figure 2. Transfer Characteristics**



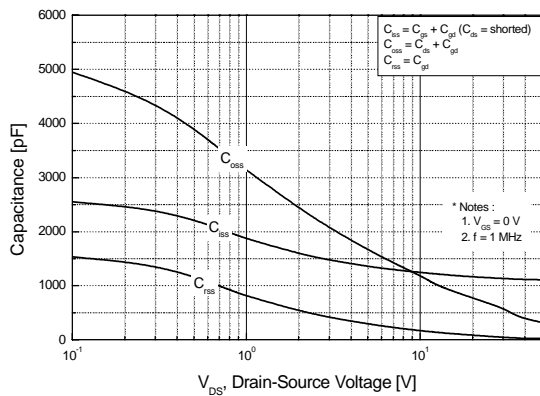
**Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage**



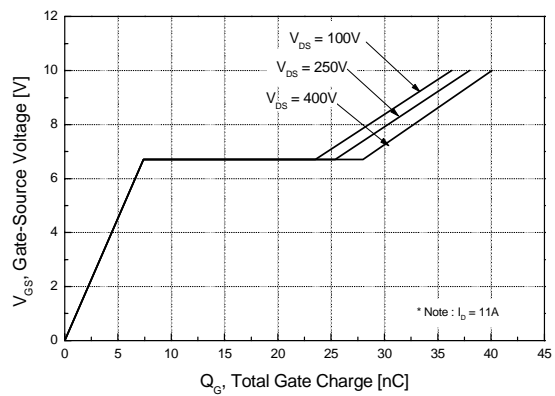
**Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature**



**Figure 5. Capacitance Characteristics**

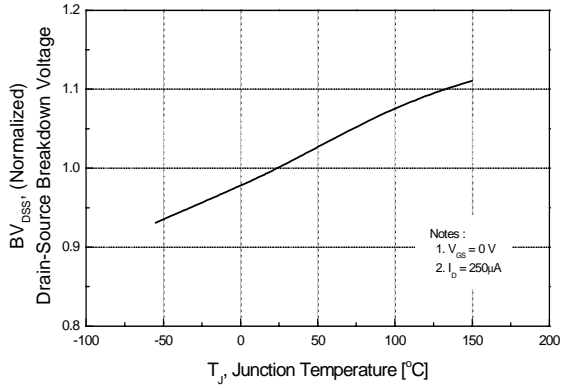


**Figure 6. Gate Charge Characteristics**

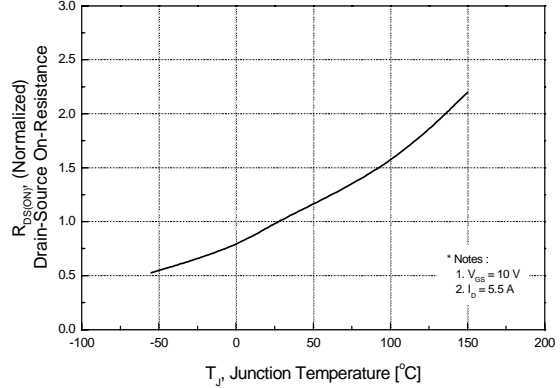


**Typical Performance Characteristics** (Continued)

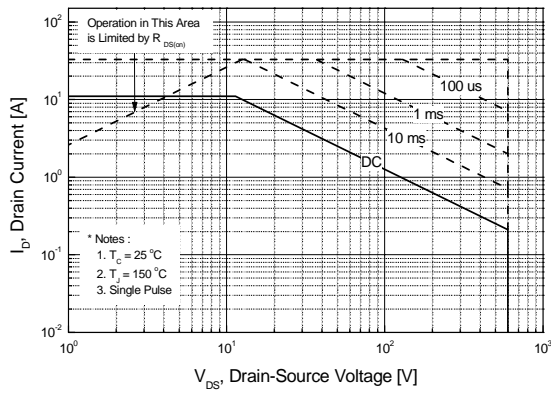
**Figure 7. Breakdown Voltage Variation vs. Temperature**



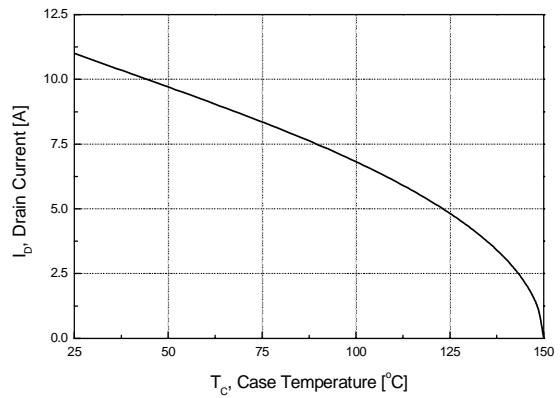
**Figure 8. On-Resistance Variation vs. Temperature**



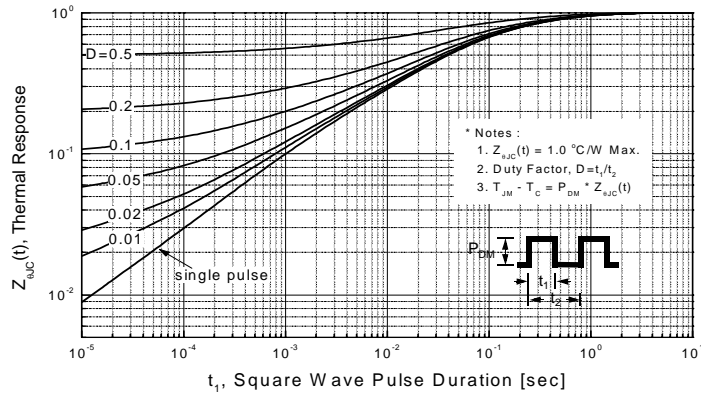
**Figure 9-1. Maximum Safe Operating Area**



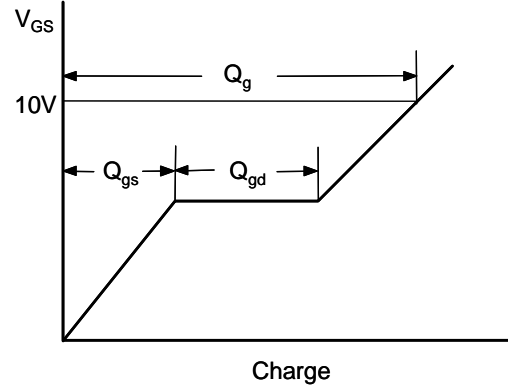
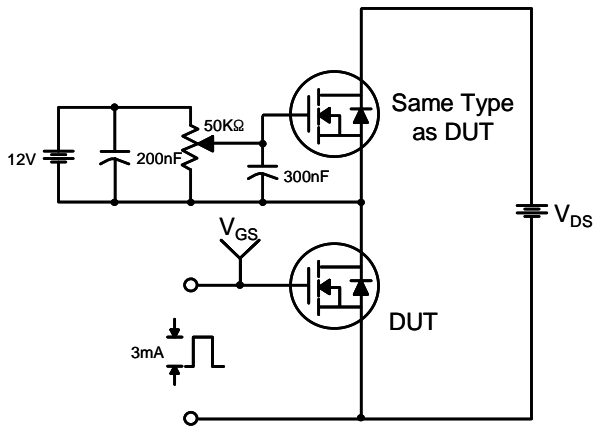
**Figure 10. Maximum Drain Current vs. Case Temperature**



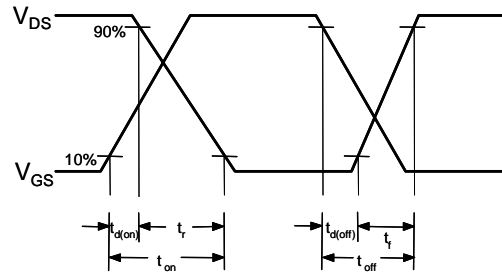
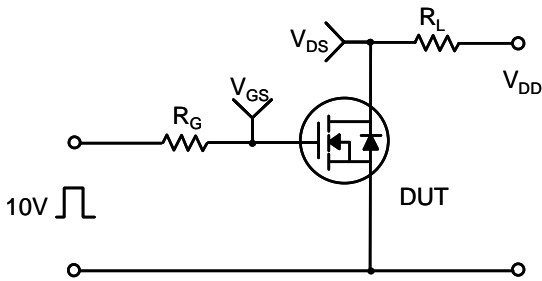
**Figure 11. Transient Thermal Response Curve**



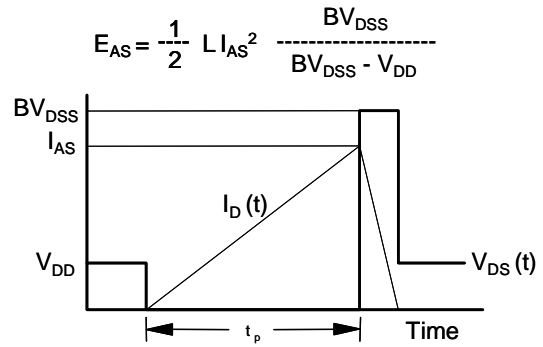
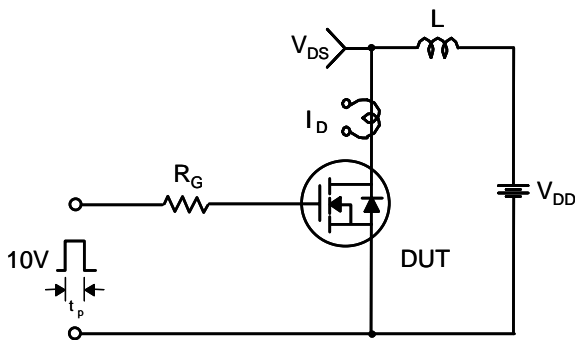
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



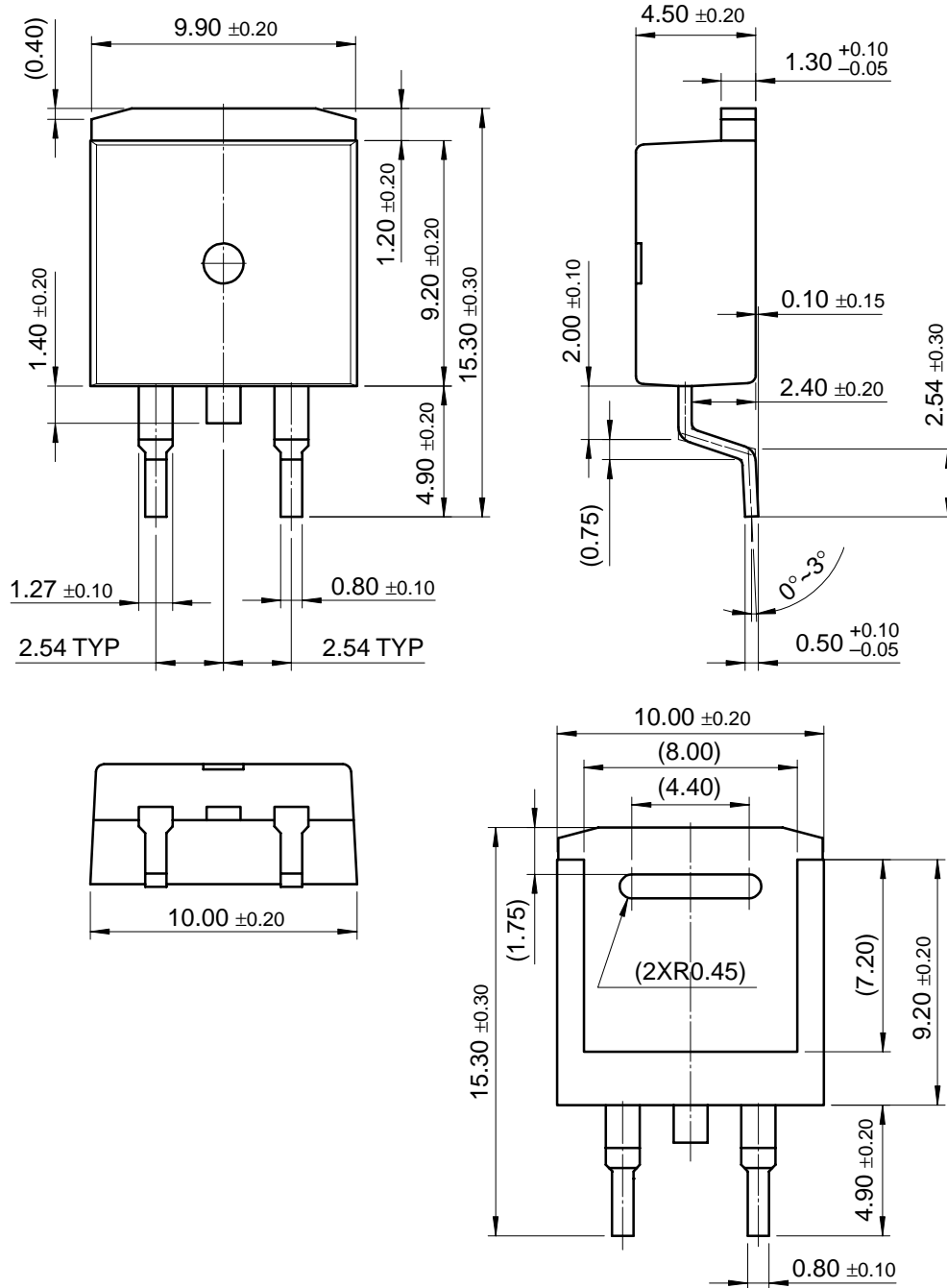
Unclamped Inductive Switching Test Circuit & Waveforms





Mechanical Dimensions

D<sup>2</sup>-PAK



Dimensions in Millimeters

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No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
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