



# FCI7N60

## N-Channel SuperFET® MOSFET

### 600 V, 7 A, 600 mΩ

#### Features

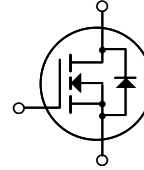
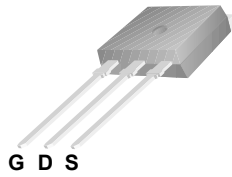
- 650V @T<sub>J</sub> = 150°C
- Typ. R<sub>DS(on)</sub> = 530 mΩ
- Ultra Low Gate Charge (Typ. Q<sub>g</sub> = 23 nC)
- Low Effective Output Capacitance (Typ. C<sub>oss,eff</sub> = 60 pF)
- 100% Avalanche Tested
- RoHS compliant

#### Description

SuperFET® MOSFET is Fairchild Semiconductor®'s first generation of high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This technology is tailored to minimize conduction loss, provide superior switching performance, dv/dt rate and higher avalanche energy. Consequently, SuperFET MOSFET is very suitable for the switching power applications such as PFC, server/telecom power, FPD TV power, ATX power and industrial power applications.

#### Application

- Lighting
- Solar Inverter
- AC-DC Power Supply



#### MOSFET Maximum Ratings T<sub>C</sub> = 25°C unless otherwise noted\*

Symbol	Parameter	FCI47N60	Unit
V <sub>DSS</sub>	Drain to Source Voltage	600	V
I <sub>D</sub>	Drain Current	-Continuous (T <sub>C</sub> = 25°C)	7
		-Continuous (T <sub>C</sub> = 100°C)	4.4
I <sub>DM</sub>	Drain Current	- Pulsed (Note 1)	21
V <sub>GSS</sub>	Gate to Source Voltage	±30	V
E <sub>AS</sub>	Single Pulsed Avalanche Energy	(Note 2)	230
I <sub>AR</sub>	Avalanche Current	(Note 1)	7
E <sub>AR</sub>	Repetitive Avalanche Energy	(Note 1)	8.3
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	4.5
P <sub>D</sub>	Power Dissipation	(T <sub>C</sub> = 25°C)	83
		- Derate above 25°C	0.67
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature Range	-55 to +150	°C
T <sub>L</sub>	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds	300	°C

\*Drain current limited by maximum junction temperature

#### Thermal Characteristics

Symbol	Parameter	FCI47N60	Unit
R <sub>θJC</sub>	Thermal Resistance, Junction to Case, Max	1.5	°C/W
R <sub>θJA</sub>	Thermal Resistance, Junction to Ambient, Max	62.5	°C/W

## Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FCI7N60	FCI7N60	I <sup>2</sup> -PAK	-	-	50

## Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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### Off Characteristics

BV <sub>DSS</sub>	Drain to Source Breakdown Voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA, T <sub>C</sub> = 25°C	600	-	-	V
		V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA, T <sub>C</sub> = 150°C	-	650	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, Referenced to 25°C	-	0.6	-	V/°C
BV <sub>DS</sub>	Drain-Source Avalanche Breakdown Voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 7 A	-	700	-	V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 600 V, V <sub>GS</sub> = 0 V	-	-	1	μA
		V <sub>DS</sub> = 480 V, T <sub>C</sub> = 125°C	-	-	10	
I <sub>GSS</sub>	Gate to Body Leakage Current	V <sub>GS</sub> = ±30 V, V <sub>DS</sub> = 0 V	-	-	±100	nA

### On Characteristics

V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 250 μA	3.0	-	5.0	V
R <sub>DS(on)</sub>	Static Drain to Source On Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 3.5 A	-	0.53	0.6	Ω
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 40 V, I <sub>D</sub> = 3.5 A (Note 4)	-	6	-	S

### Dynamic Characteristics

C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0 V f = 1.0 MHz	-	710	920	pF
C <sub>oss</sub>	Output Capacitance		-	380	500	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		-	34	-	pF
C <sub>oss</sub>	Output Capacitance	V <sub>DS</sub> = 480 V, V <sub>GS</sub> = 0 V, f = 1.0 MHz	-	22	29	pF
C <sub>oss,eff.</sub>	Effective Output Capacitance	V <sub>DS</sub> = 0 V to 400 V, V <sub>GS</sub> = 0 V	-	60	-	pF

### Switching Characteristics

t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = 300 V, I <sub>D</sub> = 7 A R <sub>G</sub> = 25 Ω (Note 4, 5)	-	35	80	ns
t <sub>r</sub>	Turn-On Rise Time		-	55	120	ns
t <sub>d(off)</sub>	Turn-Off Delay Time		-	75	160	ns
t <sub>f</sub>	Turn-Off Fall Time		-	32	75	ns
Q <sub>g(tot)</sub>	Total Gate Charge at 10V		V <sub>DS</sub> = 480 V, I <sub>D</sub> = 7 A, V <sub>GS</sub> = 10 V (Note 4, 5)	-	23	30
Q <sub>gs</sub>	Gate to Source Gate Charge		-	4.2	5.5	nC
Q <sub>gd</sub>	Gate to Drain "Miller" Charge		-	11.5	-	nC

### Drain-Source Diode Characteristics

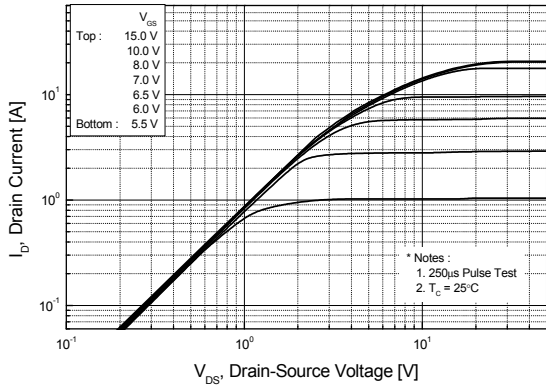
I <sub>S</sub>	Maximum Continuous Drain to Source Diode Forward Current	-	-	7	A	
I <sub>SM</sub>	Maximum Pulsed Drain to Source Diode Forward Current	-	-	21	A	
V <sub>SD</sub>	Drain to Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>SD</sub> = 7 A	-	-	1.4	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0 V, I <sub>SD</sub> = 7 A di <sub>F</sub> /dt = 100 A/μs (Note 4)	-	360	-	ns
Q <sub>rr</sub>	Reverse Recovery Charge		-	4.5	-	μC

#### NOTES:

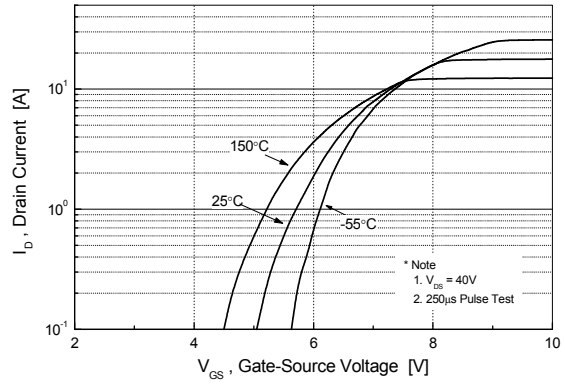
1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. I<sub>AS</sub> = 3.5 A, V<sub>DD</sub> = 50 V, R<sub>G</sub> = 25Ω, Starting T<sub>J</sub> = 25°C
3. I<sub>SD</sub> ≤ 7 A, di/dt ≤ 200 A/μs, V<sub>DD</sub> ≤ BV<sub>DSS</sub>, Starting T<sub>J</sub> = 25°C
4. Pulse Test: Pulse width ≤ 300 μs, Duty Cycle ≤ 2%
5. Essentially Independent of Operating Temperature Typical Characteristics

## Typical Performance Characteristics

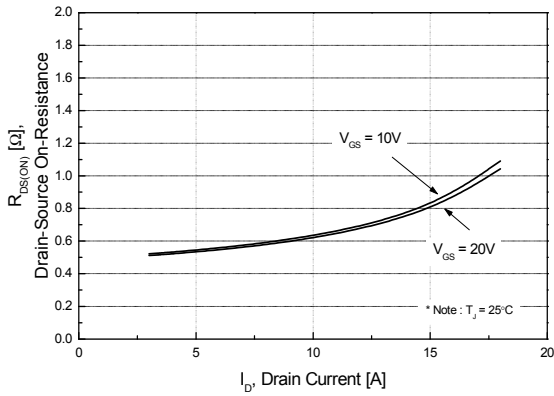
**Figure 1. On-Region Characteristics**



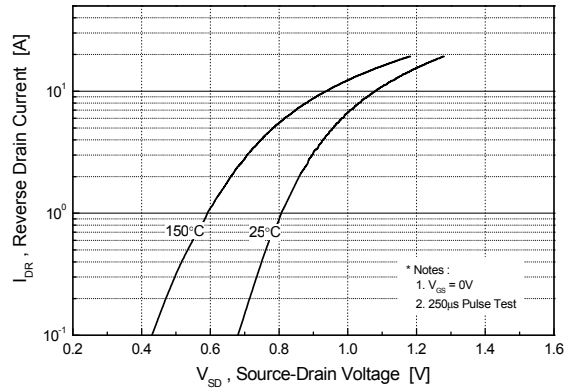
**Figure 2. Transfer Characteristics**



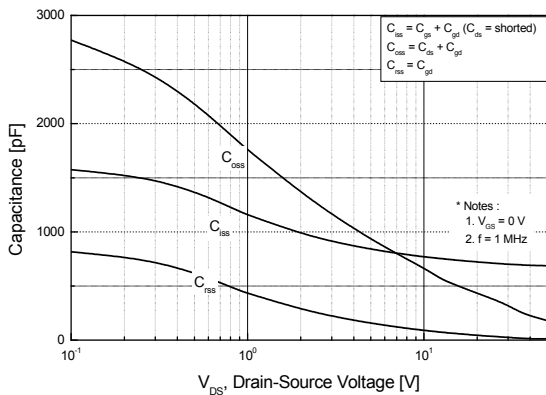
**Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage**



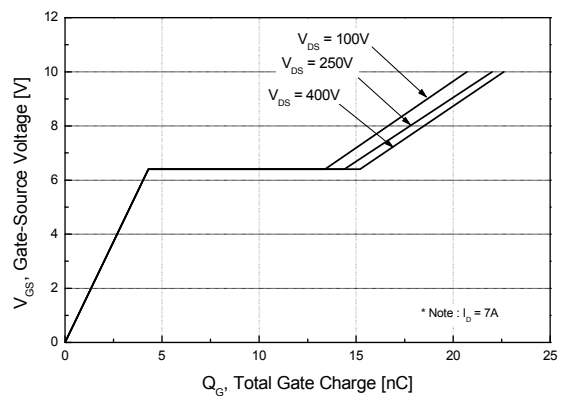
**Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature**



**Figure 5. Capacitance Characteristics**

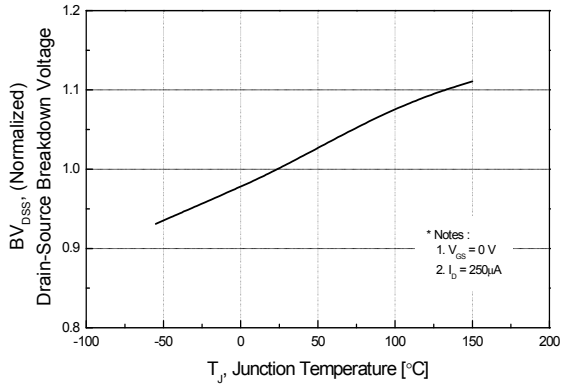


**Figure 6. Gate Charge Characteristics**

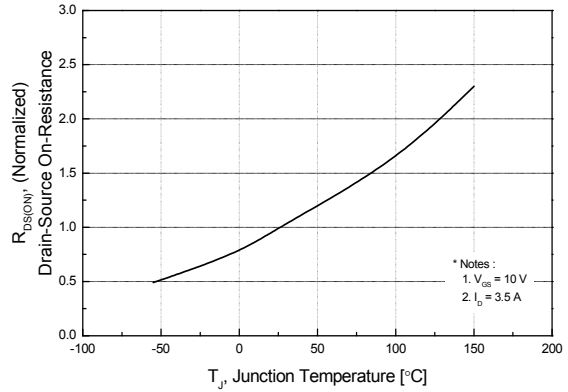


## Typical Performance Characteristics (Continued)

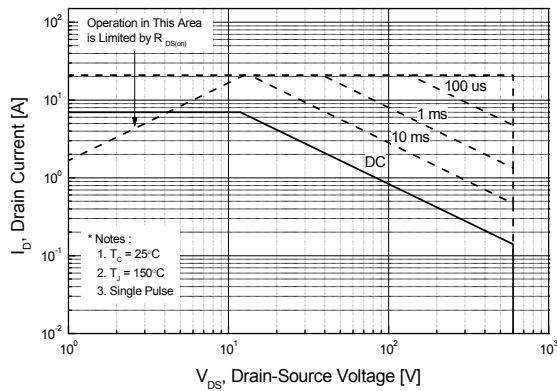
**Figure 7. Breakdown Voltage Variation vs. Temperature**



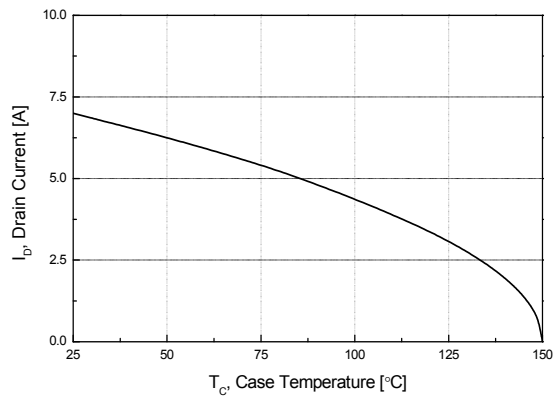
**Figure 8. On-Resistance Variation vs. Temperature**



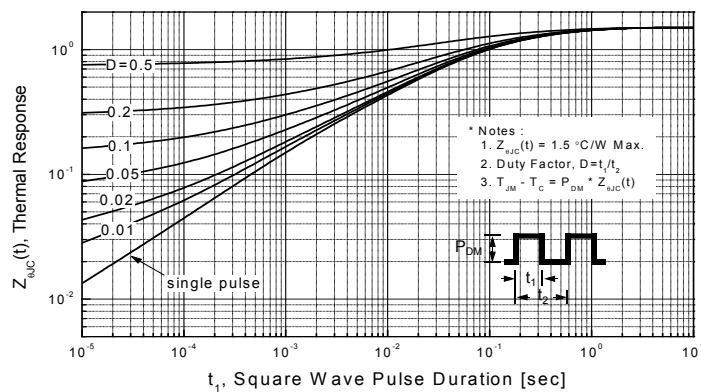
**Figure 9. Maximum Safe Operating Area**



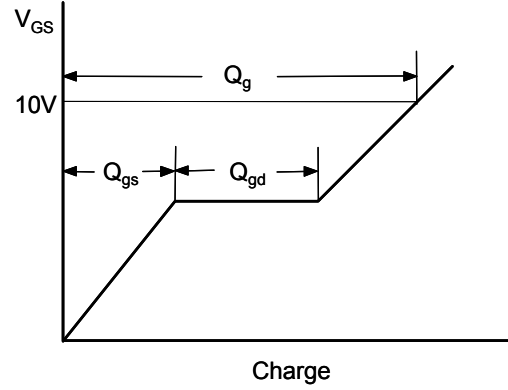
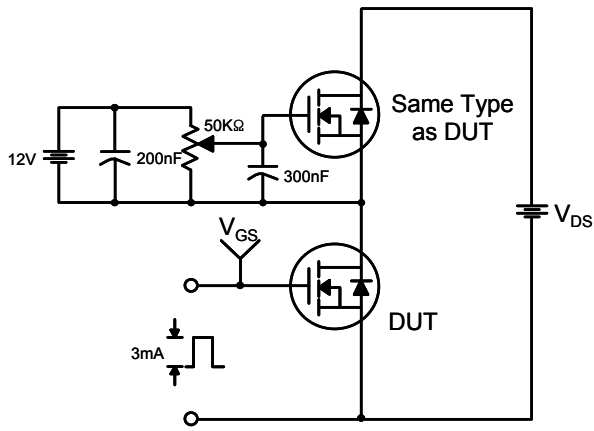
**Figure 10. Maximum Drain Current vs. Case Temperature**



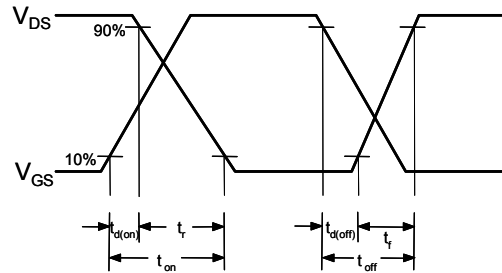
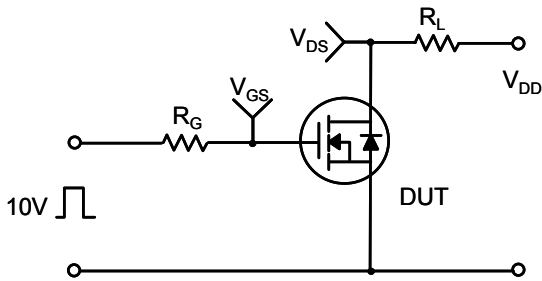
**Figure 10. Transient Thermal Response Curve**



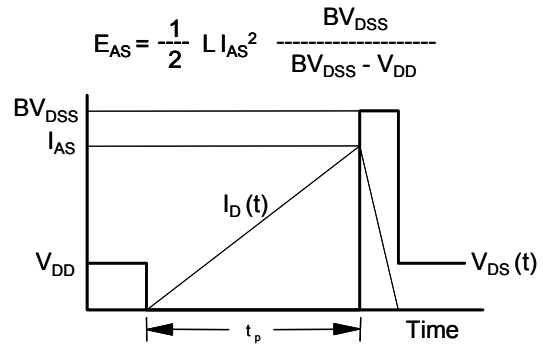
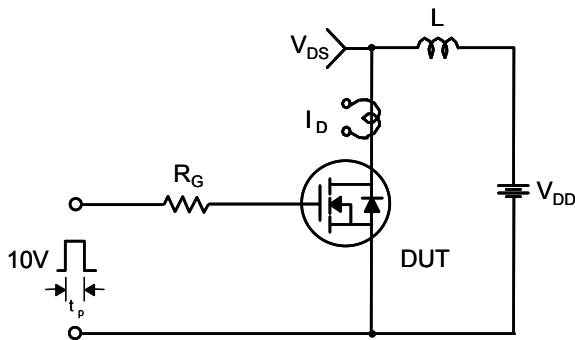
**Gate Charge Test Circuit & Waveform**



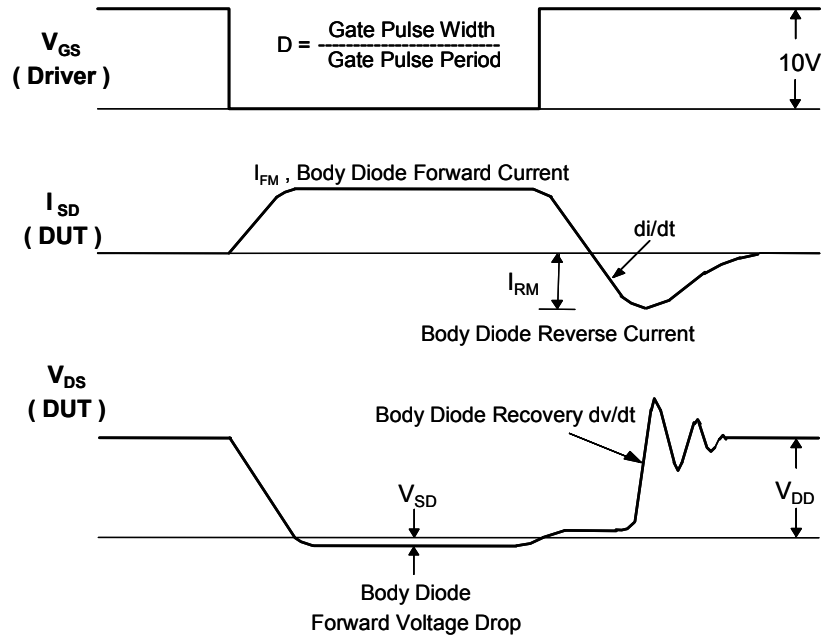
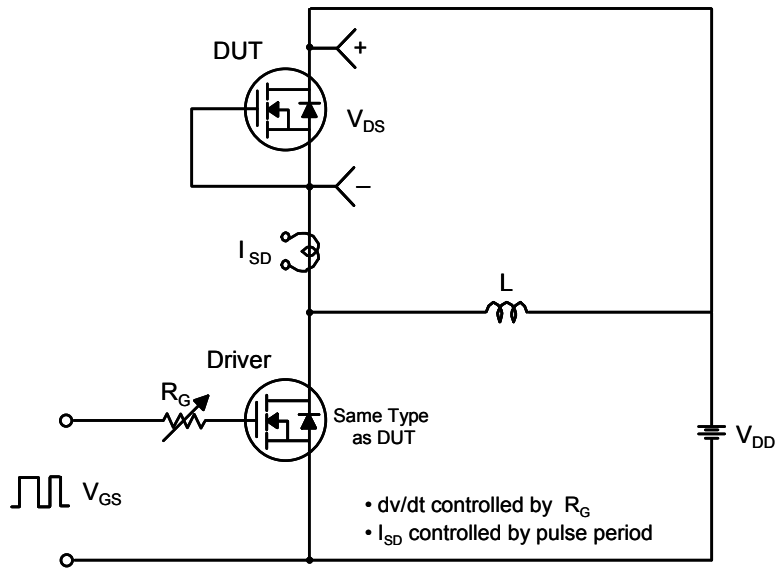
**Resistive Switching Test Circuit & Waveforms**



**Unclamped Inductive Switching Test Circuit & Waveforms**

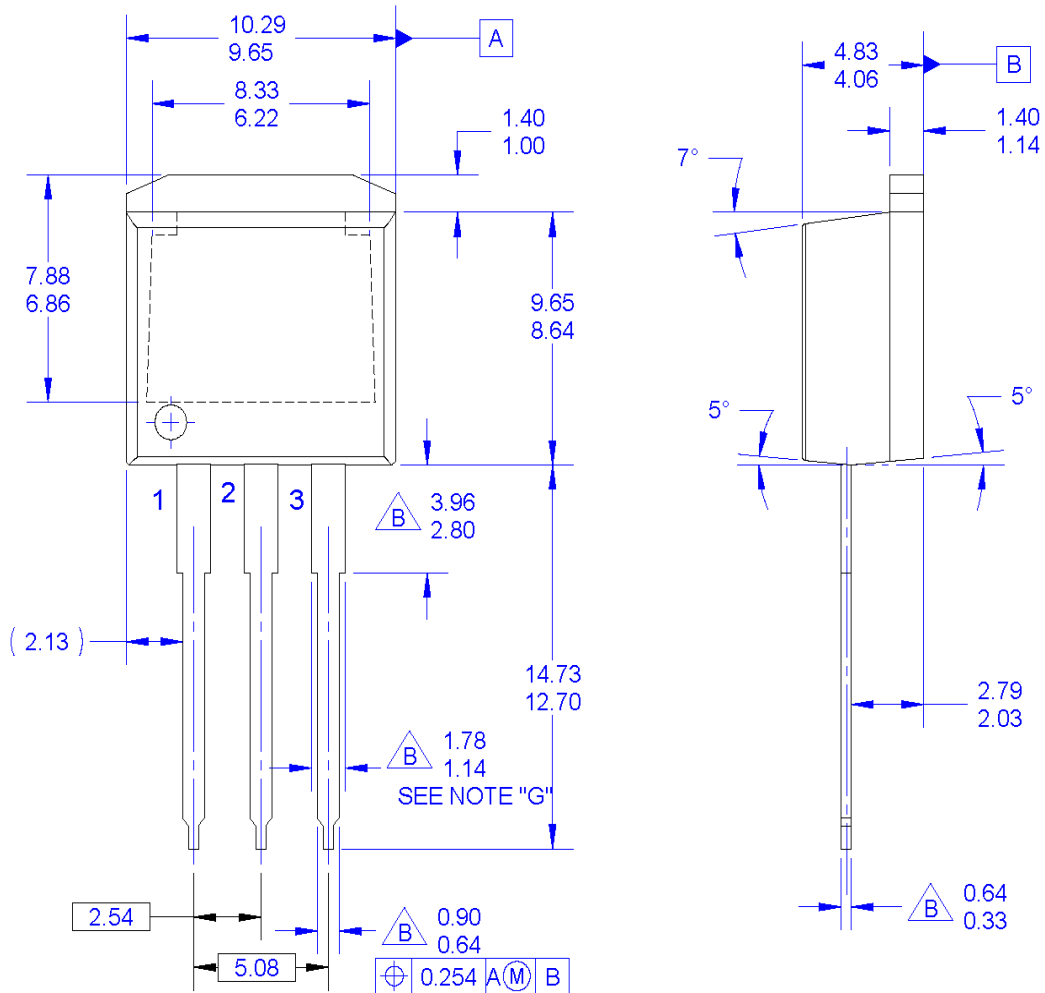


Peak Diode Recovery dv/dt Test Circuit & Waveforms



Mechanical Dimensions

I<sup>2</sup>-PAK



NOTES:



- A. EXCEPT WHERE NOTED CONFORMS TO TO262 JEDEC VARIATION AA.
- B. DOES NOT COMPLY JEDEC STD. VALUE.
- C. ALL DIMENSIONS ARE IN MILLIMETERS.
- D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.
- E. DIMENSION AND TOLERANCE AS PER ANSI Y14.5-1994.
- F. LOCATION OF PIN HOLE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF PACKAGE)
- G. MAXIMUM WIDTH FOR F-102 DEVICE = 1.35 MAX.
- H. DRAWING FILE NAME: TO262A03REV5

Dimensions in Millimeters



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| AX-CAP®*  | FRFET®  | Programmable Active Droop™            | TinyBoost™  |
| BitSiC™   | Global Power Resource <sup>SM</sup>             | QFET®                                 | TinyBuck™   |
| Build it Now™   | Green Bridge™                                   | QS™                                   | TinyCalc™   |
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|  | MicroPak™                                       | SuperFET®                             | UHC®  |
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| FETBench™   | OPTOPLANAR®                                     |                                       |   |

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