FAIRCHILD
SEMICONDUCTOR ™

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FDD6030L

N-Channel Logic Level Enhancement Mode Field Effect Transistor

General Description

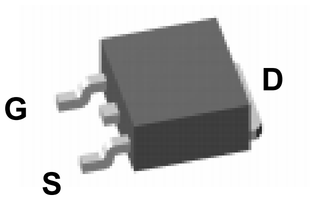
These N-Channel logic level enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage applications such as DC/DC converters and high efficiency switching circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Applications

- DC/DC converter
- Motor drives

Features

- 12 A, 30 V. $R_{DS(ON)} = 0.0145\ \Omega$ @ $V_{GS} = 10$ V
  $R_{DS(ON)} = 0.0210\ \Omega$ @ $V_{GS} = 4.5$ V.
- Low gate charge.
- Fast switching speed.
- Low C_{RSS}.



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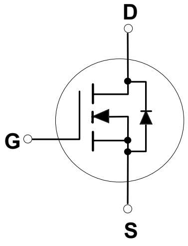


Absolute Maximum Ratings

$T_C = 25°C$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain-Source Voltage	30	V
V_{GSS}	Gate-Source Voltage	±20	V
I_D	Maximum Drain Current -Continuous (Note 1)	50	A
	(Note 1a)	12	
	Maximum Drain Current -Pulsed	100	
P_D	Maximum Power Dissipation @ $T_C = 25°C$ (Note 1)	60	W
	$T_A = 25°C$ (Note 1a)	3.2	
	$T_A = 25°C$ (Note 1b)	1.3	
T_J, T_{stg}	Operating and Storage Junction Temperature Range	-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	2.1	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	39	°C/W
	(Note 1b)	96	°C/W

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
FDD6030L	FDD6030L	13''	16mm	2500

Electrical Characteristics

T_A = 25°C unless otherwise noted

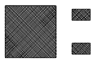
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
W_{DSS}	Single Pulse Drain-Source Avalanche Energy	V_{DD} = 15 V, I_D = 12 A			100	mJ
I_{AR}	Maximum Drain-Source Avalanche Current				12	A
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250μA, Referenced to 25°C		37		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V			1	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = 20V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = -20 V, V_{DS} = 0 V			-100	nA
On Characteristics (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 μA	1	1.6	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = 250 μA,Referenced to 25°C		-4		mV/°C
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 12 A V_{GS} = 10 V, I_D = 12 A,T_J=125°C V_{GS} = 4.5 V, I_D = 10 A		.0115 .0160 .0175	.0145 .0250 .0210	Ω
$I_{D(on)}$	On-State Drain Current	V_{GS} = 10 V, V_{DS} = 5 V	50			A
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 9 A		25		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 15 V, V_{GS} = 0 V, f = 1.0 MHz		1230		pF
C_{oss}	Output Capacitance			640		pF
C_{rss}	Reverse Transfer Capacitance			175		pF
Switching Characteristics (Note 2)						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 10 V, I_D = 1 A, V_{GS} = 10 V, R_{GEN} = 6 Ω		11	20	ns
t_r	Turn-On Rise Time			15	28	ns
$t_{d(off)}$	Turn-Off Delay Time			37	60	ns
t_f	Turn-Off Fall Time			23	37	ns
Q_g	Total Gate Charge	V_{DS} = 15 V, I_D = 12 A, V_{GS} = 10 V,		36	50	nC
Q_{gs}	Gate-Source Charge			4.5		nC
Q_{gd}	Gate-Drain Charge			10		nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current (Note 1)				50	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 2.3 A (Note 2)		0.75	1.2	V

Notes:

1. R_{qJA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the drain tab. R_{qJC} is guaranteed by design while R_{qCA} is determined by the user's board design. R_{qJC} has been used to determine some maximum ratings.

a) R_{qJA}= 40°C/W when mounted on a 1in^2 pad of 2oz copper.

Scale 1 : 1 on letter size paper



b) R_{qJA}= 96°C/W on a minimum mounting pad.

2. Pulse Test: Pulse Width £ 300 ms, Duty Cycle £ 2.0%

Typical Characteristics

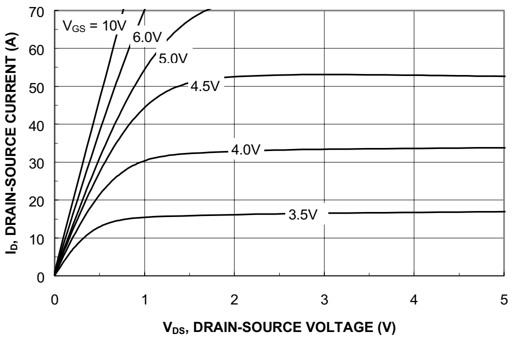


Figure 1. On-Region Characteristics.

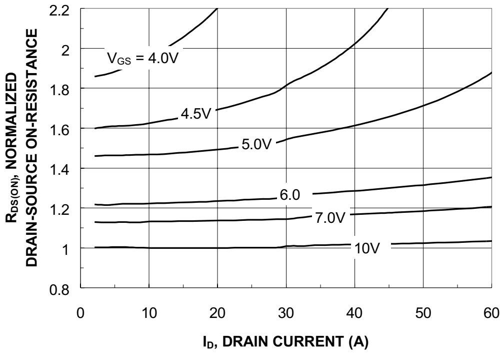


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

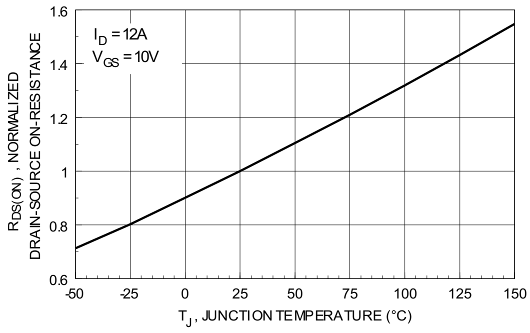


Figure 3. On-Resistance Variation with Temperature.

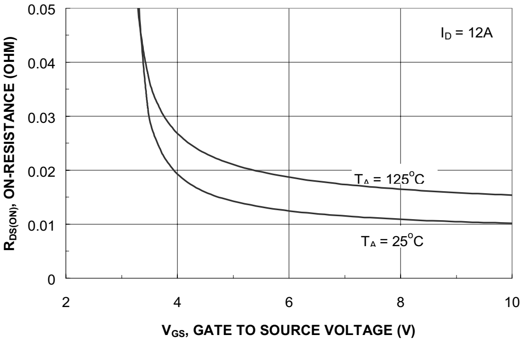


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

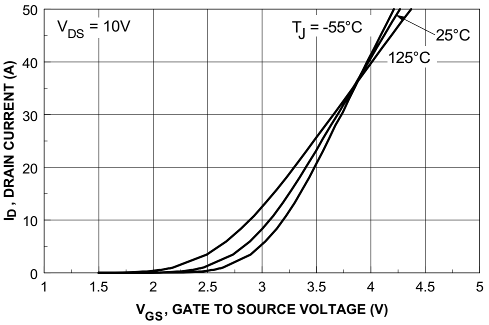


Figure 5. Transfer Characteristics.

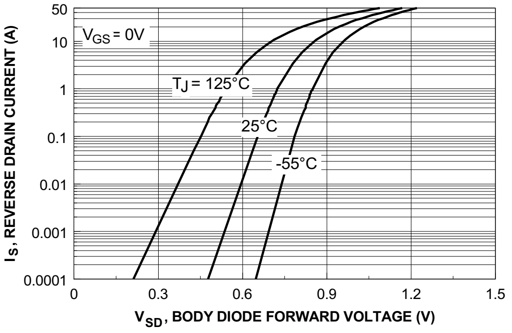


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics (continued)

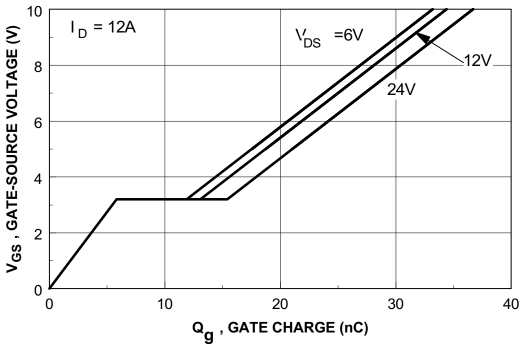


Figure 7. Gate-Charge Characteristics.

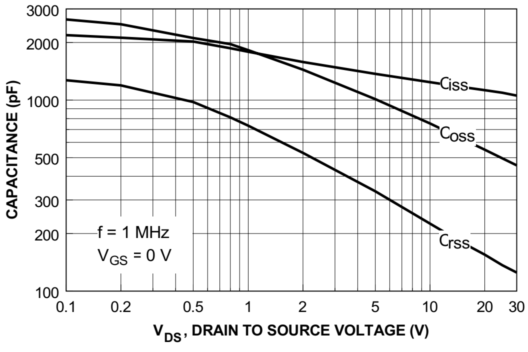


Figure 8. Capacitance Characteristics.

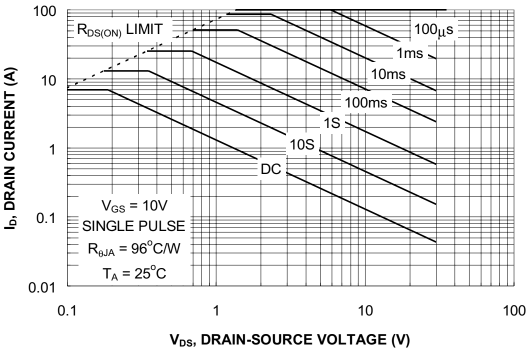


Figure 9. Maximum Safe Operating Area.

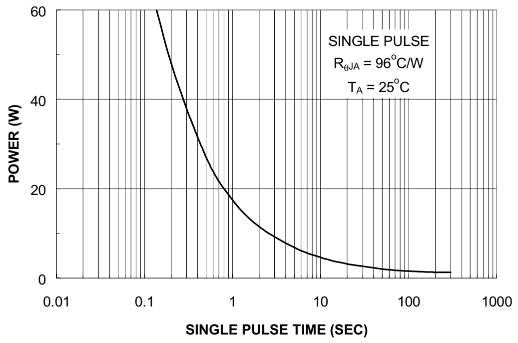


Figure 10. Single Pulse Maximum Power Dissipation.

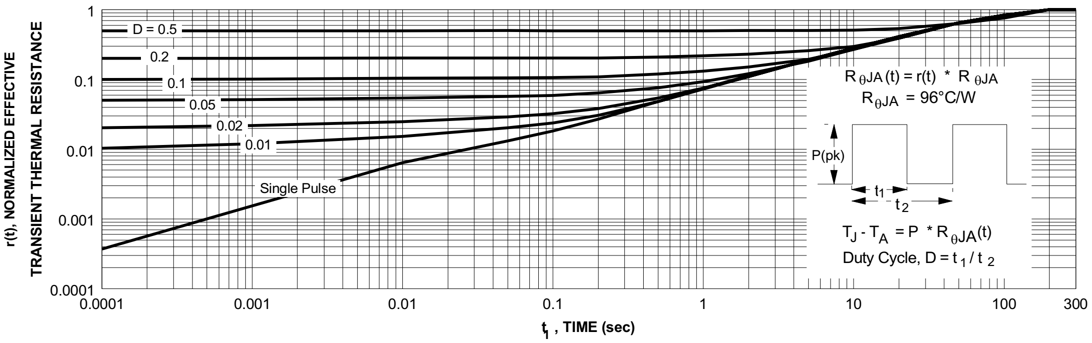


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b.
Transient themal response will change depending on the circuit board design.

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