

FDD603AL

N-Channel Logic Level Enhancement Mode Field Effect Transistor

General Description

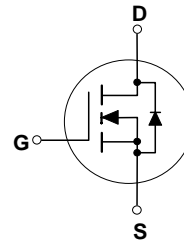
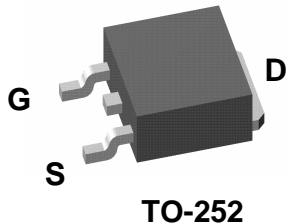
This N-Channel logic level enhancement mode power field effect transistor is produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is tailored to minimize on-state resistance. These devices are particularly suited for low voltage applications such as DC/DC converters and high efficiency switching circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Applications

- DC/DC converters
- Motor drives

Features

- 33 A, 30 V. $R_{DS(ON)} = 0.023 \Omega @ V_{GS} = 10 \text{ V}$
 $R_{DS(ON)} = 0.037 \Omega @ V_{GS} = 4.5 \text{ V}$.
- Critical DC electrical parameters specified at elevated temperature.
- Rugged avalanche-rated internal source-drain diode can eliminate the need for external Zener Diode.
- High density cell design for extremely low $R_{DS(ON)}$.



Absolute Maximum Ratings T_c=25°C unless otherwise noted

Symbol	Parameter	Rated	Units
V _{DSS}	Drain-Source Voltage	30	V
V _{GSS}	Gate-Source Voltage	±20	V
I _D	Maximum Drain Current - Continuous <small>(Note 1)</small> <small>T_A = 25°C (Note 1a)</small>	33	A
	Maximum Drain Current - Pulsed	80	
P _D	Maximum Power Dissipation @ <small>T_C = 25°C (Note 1)</small> <small>T_A = 25°C (Note 1a)</small> <small>T_A = 25°C (Note 1b)</small>	39	W
		3.2	
		1.3	
T _J , T _{stg}	Operating and Storage Junction Temperature Range	-55 to +150	°C

Thermal Characteristics

R _{θJC}	Thermal Resistance, Junction-to-Case <small>(Note 1)</small>	2.5	°C/W
R _{θJA}	Thermal Resistance, Junction-to-Ambient <small>(Note 1a)</small> <small>(Note 1b)</small>	40	°C/W
		96	°C/W

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape Width	Quantity
FDD603AL	FDD603AL	13"	16mm	2500

Electrical Characteristics

$T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
W_{DSS}	Single Pulse Drain-Source Avalanche Energy	$V_{DD} = 15\text{ V}, I_D = 12\text{ A}$			100	mJ
I_{AR}	Maximum Drain-Source Avalanche Current				12	A
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C		32		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{ V}, V_{GS} = 0\text{ V}$			10	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$			100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -20\text{ V}, V_{DS} = 0\text{ V}$			-100	nA

On Characteristics (Note 2)

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	1	1.7	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C		-4.5		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 9.5\text{ A}$ $V_{GS} = 10\text{ V}, I_D = 9.5\text{ A}, T_J = 125^\circ\text{C}$ $V_{GS} = 4.5\text{ V}, I_D = 7.5\text{ A}$		0.016 0.024 0.026	0.023 0.035 0.037	Ω
$I_{D(on)}$	On-State Drain Current	$V_{GS} = 10\text{ V}, V_{DS} = 10\text{ V}$	60			A
g_{FS}	Forward Transconductance	$V_{DS} = 10\text{ V}, I_D = 9.5\text{ A}$		18		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}$ $f = 1.0\text{ MHz}$		670		pF
C_{oss}	Output Capacitance			345		pF
C_{riss}	Reverse Transfer Capacitance			95		pF

Switching Characteristics (Note 2)

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 15\text{ V}, I_D = 1\text{ A}$ $V_{GS} = 10\text{ V}, R_{GEN} = 6\ \Omega$		10	20	ns
t_r	Turn-On Rise Time			16	30	ns
$t_{d(off)}$	Turn-Off Delay Time			27	45	ns
t_f	Turn-Off Fall Time			12	22	ns
Q_g	Total Gate Charge	$V_{DS} = 10\text{ V}, I_D = 9.5\text{ A}$ $V_{GS} = 10\text{ V}$		19	26	nC
Q_{gs}	Gate-Source Charge			3.5		nC
Q_{gd}	Gate-Drain Charge			5.5		nC

Drain-Source Diode Characteristics and Maximum Ratings

I_S	Maximum Continuous Drain-Source Diode Forward Current <small>(Note 1)</small>			33	A	
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 2.3\text{ A}$ <small>(Note 2)</small>		0.78	1.2	V

Notes:

- $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the drain tab. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design. $R_{\theta JC}$ has been used to determine some maximum ratings.



Scale 1 : 1 on letter size paper

■ a) $R_{\theta JA} = 40^\circ\text{C/W}$ when mounted on a 1 in^2 pad of 2oz copper.

■ b) $R_{\theta JA} = 96^\circ\text{C/W}$ on a minimum mounting pad.

- Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2.0\%$

Typical Characteristics

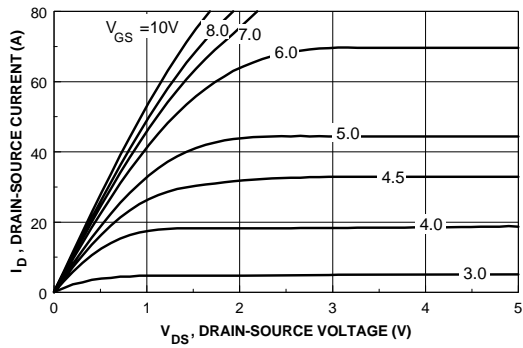


Figure 1. On-Region Characteristics.

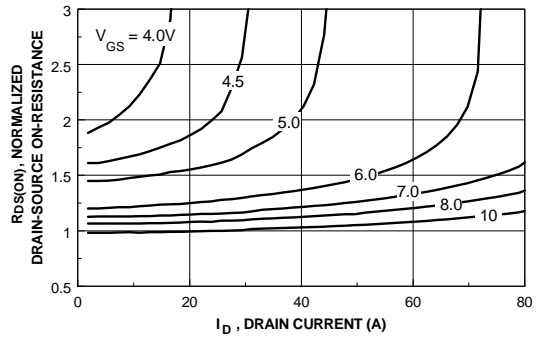


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

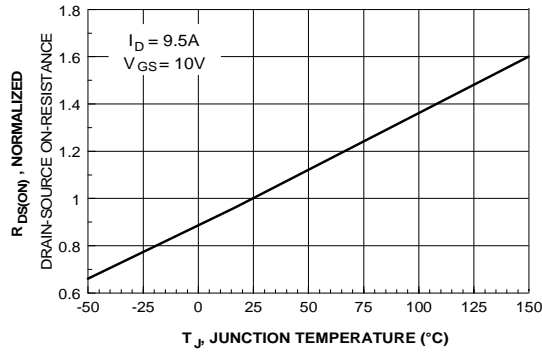


Figure 3. On-Resistance Variation with Temperature.

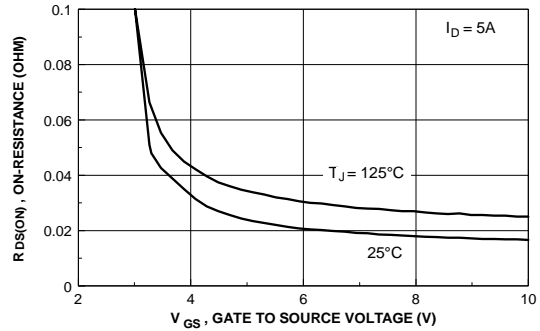


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

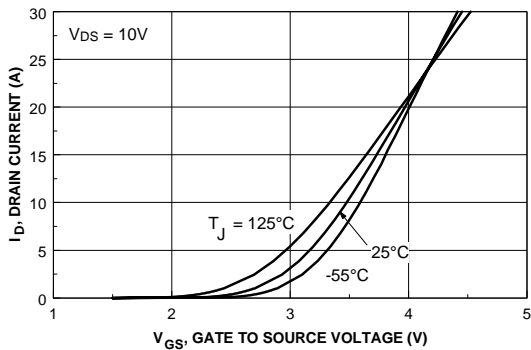


Figure 5. Transfer Characteristics.

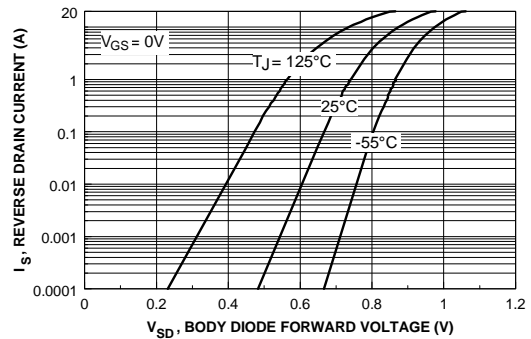


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics (continued)

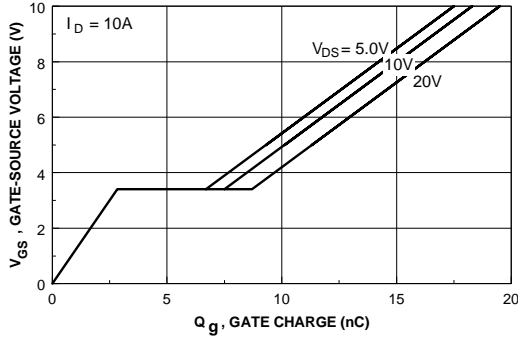


Figure 7. Gate-Charge Characteristics.

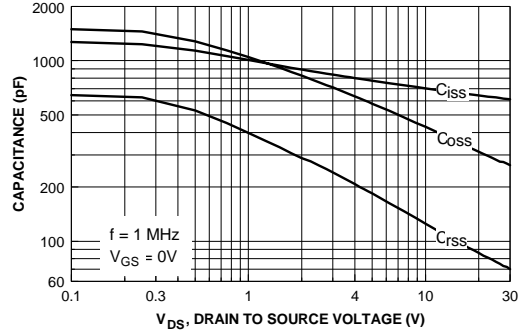


Figure 8. Capacitance Characteristics.

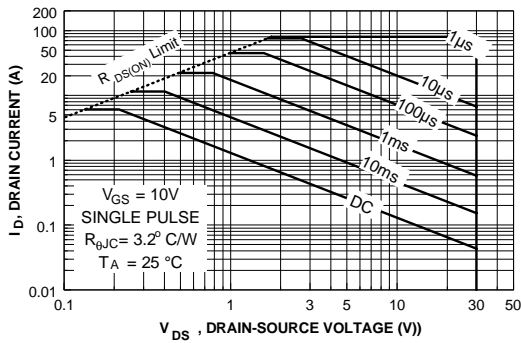


Figure 9. Maximum Safe Operating Area.

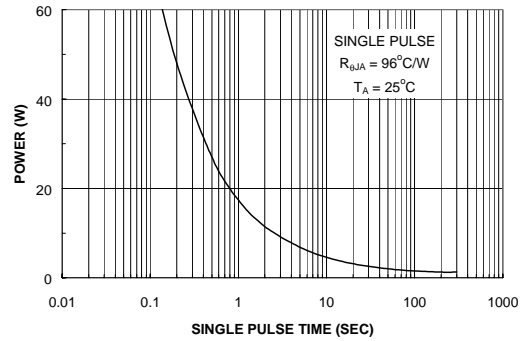


Figure 10. Single Pulse Maximum Power Dissipation.

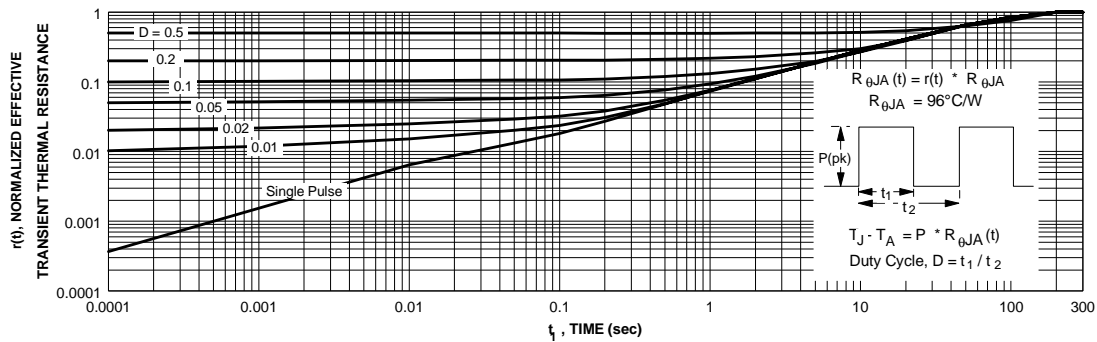


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b. Transient thermal response will change depending on the circuit board design.

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