

FDD6680

N-Channel Logic Level PWM Optimized PowerTrench™ MOSFET

General Description

This N-Channel Logic level MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers.

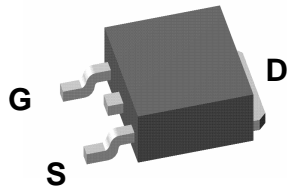
The MOSFET features faster switching and lower gate charge than other MOSFETs with comparable $R_{DS(on)}$ specifications. The result is a MOSFET that is easier to drive, even at very high frequencies, and DC/DC power supply designs with higher overall efficiency.

Features

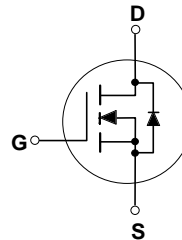
- 55 A, 30 V. $R_{DS(on)} = 0.010 \Omega @ V_{GS} = 10 \text{ V}$
 $R_{DS(on)} = 0.015 \Omega @ V_{GS} = 4.5 \text{ V}$.
- Optimized for use in high frequency DC/DC converters.
- Low gate charge (19nC typical).
- Very Fast switching.

Applications

- DC/DC converter
- Motor drives



TO-252



Absolute Maximum Ratings $T_C=25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain-Source Voltage	30	V
V_{GSS}	Gate-Source Voltage	± 20	V
I_D	Maximum Drain Current -Continuous (Note 1) (Note 1a)	55 14	A
	Maximum Drain Current -Pulsed	100	
P_D	Maximum Power Dissipation @ $T_C = 25^\circ\text{C}$ (Note 1)	60	W
	$T_A = 25^\circ\text{C}$ (Note 1a)	3.2	
	$T_A = 25^\circ\text{C}$ (Note 1b)	1.3	
T_J, T_{stg}	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction-to- Case (Note 1)	2.1	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to- Ambient (Note 1a) (Note 1b)	40	$^\circ\text{C}/\text{W}$
		96	$^\circ\text{C}/\text{W}$

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
FDD6680	FDD6680	13"	16mm	2500

Electrical Characteristics

$T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Drain-Source Avalanche ratings (Note 2)

W_{DSS}	Single Pulse Drain-Source Avalanche Energy	$V_{DD} = 15\text{ V}, I_L = 55\text{ A}$			170	mJ
I_{AR}	Maximum Drain-Source Avalanche Current				55	A

Off Characteristics

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C		18		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{ V}, V_{GS} = 0\text{ V}$			1	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$			100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -20\text{ V}, V_{DS} = 0\text{ V}$			-100	nA

On Characteristics (Note 2)

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	1	2	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C		-5.5		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 14\text{ A}$ $V_{GS} = 10\text{ V}, I_D = 14\text{ A}, T_J = 125^\circ\text{C}$ $V_{GS} = 4.5\text{ V}, I_D = 12\text{ A}$		0.008 0.013 0.012	0.010 0.017 0.015	Ω
$I_{D(on)}$	On-State Drain Current	$V_{GS} = 10\text{ V}, V_{DS} = 5\text{ V}$	50			A
g_{FS}	Forward Transconductance	$V_{DS} = 5\text{ V}, I_D = 14\text{ A}$		38		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 15\text{ V},$		2070		pF
C_{oss}	Output Capacitance	$V_{GS} = 0\text{ V},$		510		pF
C_{riss}	Reverse Transfer Capacitance	$f = 1.0\text{ MHz}$		235		pF

Switching Characteristics (Note 2)

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 15\text{ V}, I_D = 1\text{ A},$		15	28	ns
t_r	Turn-On Rise Time	$V_{GS} = 10\text{ V}, R_{GEN} = 6\ \Omega$		18	33	ns
$t_{d(off)}$	Turn-Off Delay Time			40	64	ns
t_f	Turn-Off Fall Time			18	33	ns
Q_g	Total Gate Charge	$V_{DS} = 15\text{ V}, I_D = 14\text{ A},$		19	27	nC
Q_{gs}	Gate-Source Charge	$V_{GS} = 5\text{ V},$		7		nC
Q_{gd}	Gate-Drain Charge			6		nC

Drain-Source Diode Characteristics and Maximum Ratings

I_S	Maximum Continuous Drain-Source Diode Forward Current				2.3	A
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 2.3\text{ A}$ (Note 2)		0.75	1.2	V

Notes:

- $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the drain tab. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



■ a) $R_{\theta JA} = 40^\circ\text{C/W}$ when mounted on a 1 in^2 pad of 2oz copper.



■ b) $R_{\theta JA} = 96^\circ\text{C/W}$ on a minimum mounting pad.

Scale 1 : 1 on letter size paper

- Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2.0\%$

Typical Characteristics

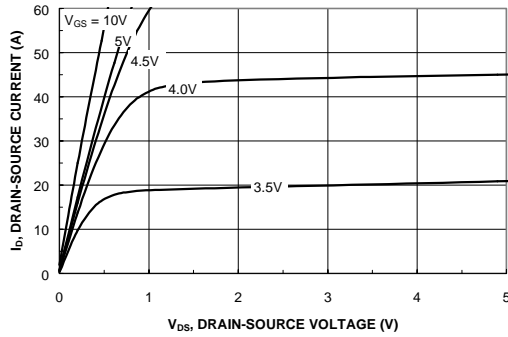


Figure 1. On-Region Characteristics.

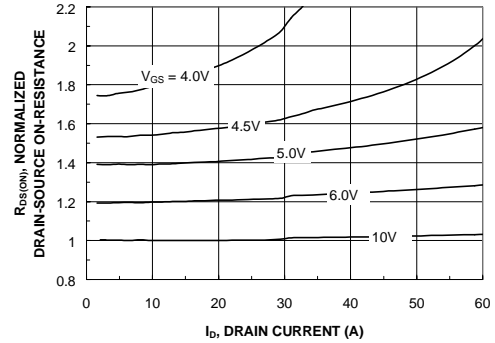


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

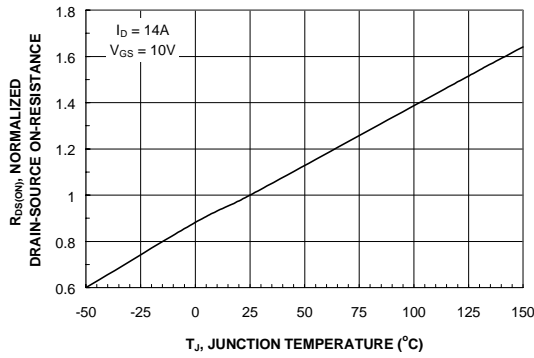


Figure 3. On-Resistance Variation with Temperature.

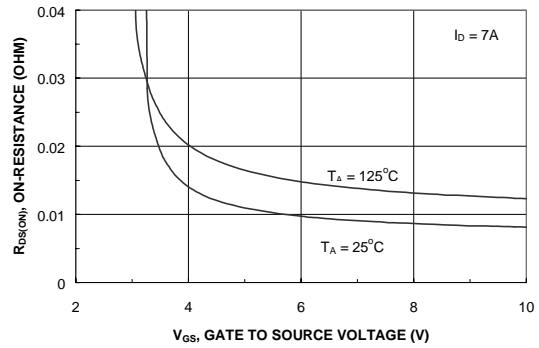


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

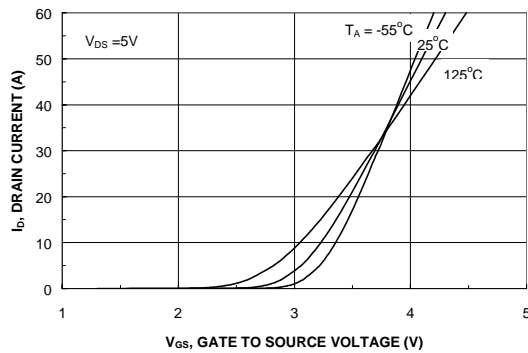


Figure 5. Transfer Characteristics.

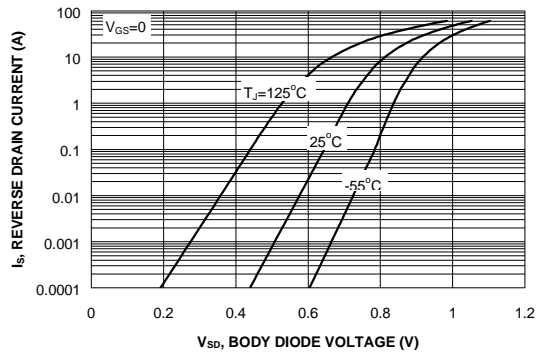


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics (continued)

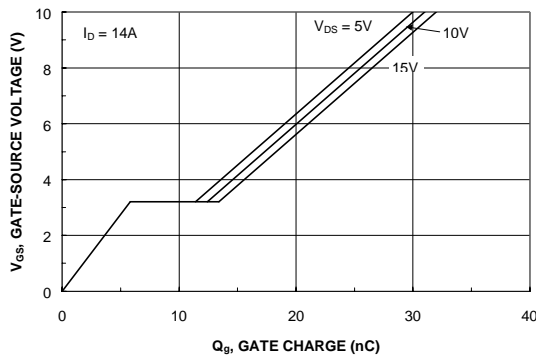


Figure 7. Gate-Charge Characteristics.

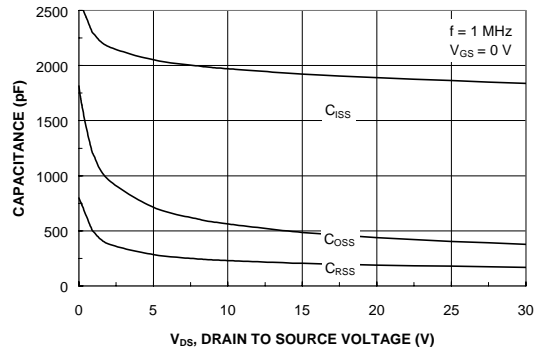


Figure 8. Capacitance Characteristics.

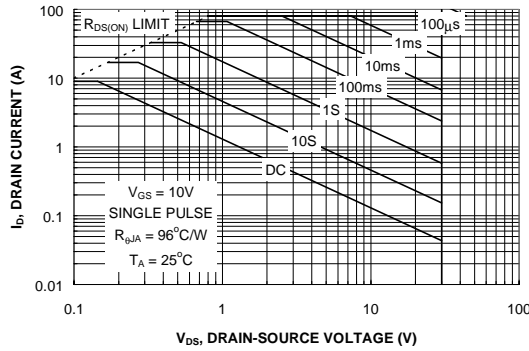


Figure 9. Maximum Safe Operating Area.

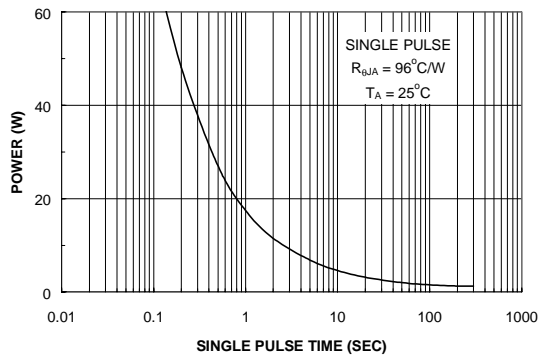


Figure 10. Single Pulse Maximum Power Dissipation.

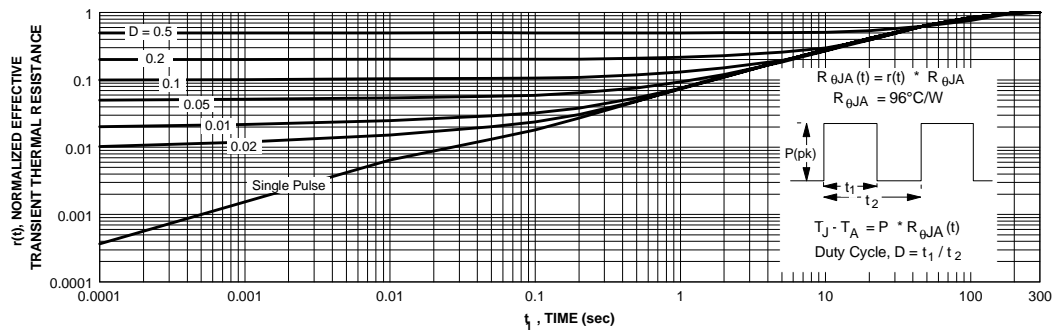


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b. Transient thermal response will change depending on the circuit board design.

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