

# DATA SHEET

## **GTL2010**

10-bit GTL processor voltage clamp

Product specification  
Supersedes data of 1999 Apr 05

2000 Aug 30

## 10-bit GTL processor voltage clamp

## GTL2010

## FEATURES

- Direct interface with TTL level
- 6.5Ω ON-state connection between port  $S_n$  and  $D_n$

## DESCRIPTION

The GTL2010 is a high speed 10-bit voltage clamp. The low ON-state resistance of the clamp allows connections to be made with minimal propagation delay.

The device is organized as one 10-bit voltage clamp. When S or D is low, the clamp is in the ON-state and a low resistance connection exists between the S and D ports. When S port and D port are high, the clamp is in the OFF-state and a very high impedance exists between the S and D ports. When port D is high, the voltage on the S port is clamped to the applied reference voltage on the GREF port.

## FUNCTION TABLE

$G_{REF}^1$	$D_{REF}^1$	$S_{REF}^2$	Switch	Driven Input	Output of Driven Input
H	H	0 V	off	X	0 V
H	H	$V_{TT}$	on	H	$V_{TT}$
H	H	$V_{TT}$	on	L	L
L	L	$V_{TT}$	off	X	0 V

H = High voltage level

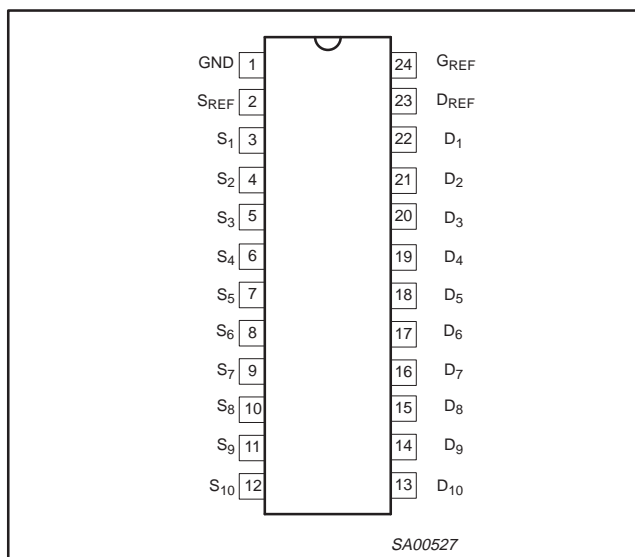
L = Low voltage level

X = Don't Care

## NOTES:

1.  $G_{REF}$  and  $D_{REF}$  are connected together and tied high through a resistor.
2.  $G_{REF}$  must be at least 1.5 V higher than  $S_{REF}$  for proper switch operation.

## PIN CONFIGURATION



## QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
		$T_{amb} = 25^{\circ}\text{C}; GND = 0V$		
$t_{PLH}$	Propagation delay Sn to Dn	$V_{DD1} = 3.3V; V_{DD2} = 2.5V;$ $V_{REF} = 1.5V; \text{unloaded}$	1.5	ns
$C_{OFF}$	Channel capacitance (OFF-state)	$V_S = 1.5V$	7.5	pF

## ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DWG NUMBER
24-Pin Plastic TSSOP Type II	0°C to +85°C	GTL2010 PW	SOT355-1

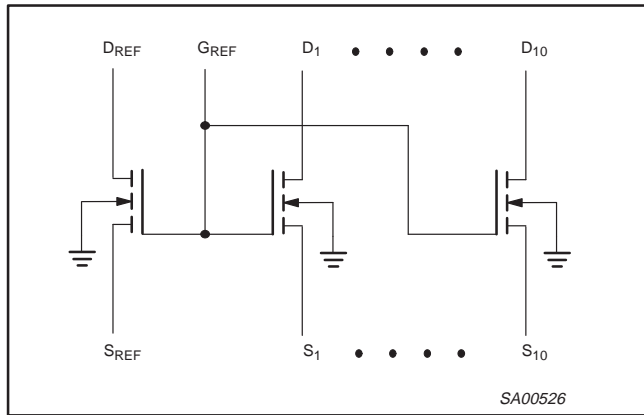
## PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	GND	Ground (0V)
2	$S_{REF}$	Source of reference transistor
3 – 12	$S_n$	Port $S_1$ to Port $S_{10}$
13 – 22	$D_n$	Port $D_1$ to Port $D_{10}$
23	$D_{REF}$	Drain of reference transistor
24	$G_{REF}$	Gate of reference transistor

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## CLAMP SCHEMATIC



## ABSOLUTE MAXIMUM RATINGS<sup>1, 2, 3</sup>

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V <sub>S_REF</sub>	DC source reference voltage		-0.5 to +7.0	V
V <sub>D_REF</sub>	DC drain reference voltage		-0.5 to +7.0	V
V <sub>G_REF</sub>	DC gate reference voltage		-0.5 to +7.0	V
V <sub>S<sub>n</sub></sub>	DC voltage Port S <sub>n</sub>		-0.5 to +7.0	V
V <sub>D<sub>n</sub></sub>	DC voltage Port D <sub>n</sub>		-0.5 to +7.0	V
I <sub>REFK</sub>	DC reference diode current	V <sub>I</sub> < 0	-50	mA
I <sub>SK</sub>	DC diode current Port S <sub>n</sub>	V <sub>I</sub> < 0	-50	mA
I <sub>DK</sub>	DC diode current Port D <sub>n</sub>	V <sub>I</sub> < 0	-50	mA
I <sub>MAX</sub>	DC clamp current per channel	Channel in ON-state	±35	mA
T <sub>stg</sub>	Storage temperature range		-65 to +150	°C

### NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
- The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			Min	Max	
V <sub>S_REF</sub>	DC source reference voltage		1.0	4.4	V
V <sub>D_REF</sub>	DC drain reference voltage		V <sub>S_REF</sub> + 0.6	5	V
V <sub>G_REF</sub>	DC gate reference voltage		V <sub>S_REF</sub> + 0.6	5	V
V <sub>S<sub>n</sub></sub>	DC voltage Port S <sub>n</sub> (OFF-state)		V <sub>S_REF</sub>	5	V
V <sub>S<sub>n</sub></sub>	DC voltage Port S <sub>n</sub> (ON-state)		0	0.2	V
V <sub>D<sub>n</sub></sub>	DC voltage Port D <sub>n</sub> (OFF-state)		V <sub>S_REF</sub>	5	V
V <sub>D<sub>n</sub></sub>	DC voltage Port D <sub>n</sub> (ON-state)		0	0.4	V
I <sub>S</sub>	Switch input leakage current (OFF-state) for S <sub>n</sub> and D <sub>n</sub> I/O	V <sub>S</sub> , V <sub>D</sub> = 5V		15	μA
I <sub>I</sub>	G <sub>REF</sub> input leakage current	V <sub>G</sub> = 5V		2.5	μA
T <sub>amb</sub>	Operating ambient temperature range	In free air	0	+85	°C

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## DC CHARACTERISTICS for $V_{DD1} = 3.0$ to $3.6V$ ; $V_{DD2} = 2.36$ to $2.64V$ ; $V_{REF} = 1.365$ to $1.635V$ range

Over recommended operating conditions. Voltage are referenced to GND (ground = 0V). Refer to the Test Circuit diagram.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			$T_{amb} = 0^{\circ}C$ to $+85^{\circ}C$			
			Min	Typ <sup>1</sup>	Max	
$V_{OL}$	LOW level output voltage	$V_S = 0.175V$ ; $I_{CLAMP} = 15.2mA$		260	350	mV

**NOTE:**

1. All typical values are measured at  $V_{DD1} = 3.3V$ ,  $V_{DD2} = 2.5V$ ,  $V_{REF} = 1.5V$  and  $T_{amb} = 25^{\circ}C$ .

## AC CHARACTERISTICS for $V_{DD1} = 3.0$ to $3.6V$ ; $V_{DD2} = 2.36$ to $2.64V$ ; $V_{REF} = 1.365$ to $1.635V$ range

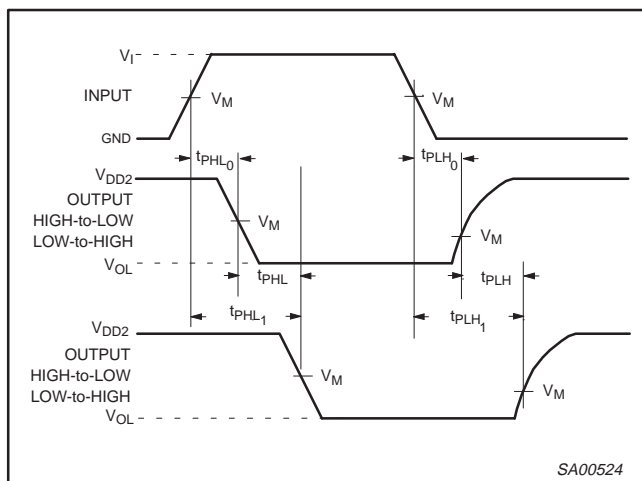
$GND = 0V$ ;  $t_r = t_f \leq 3.0ns$ . Refer to the Test Circuit diagram.

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			$T_{amb} = 0$ to $+85^{\circ}C$			
			MIN	TYP <sup>1</sup>	MAX	
$t_{PLH}^2$	Propagation delay Sn to Dn; Dn to Sn		0.5	1.5	5.5	ns

**NOTES:**

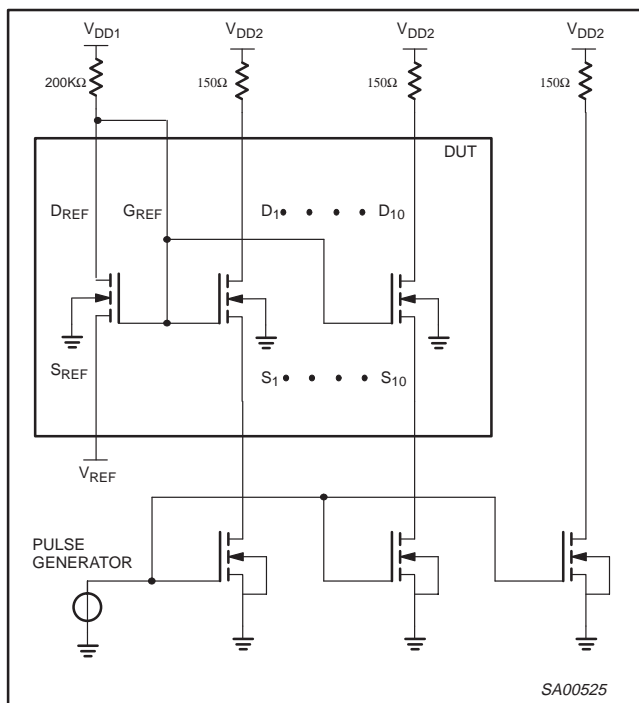
- All typical values are measured at  $V_{DD1} = 3.3V$ ,  $V_{DD2} = 2.5V$ ,  $V_{REF} = 1.5V$  and  $T_{amb} = 25^{\circ}C$ .
- Propagation delay guaranteed by characterization.
- $C_{ON,MAX}$  of 30pF and a  $C_{OFF,MAX}$  of 15pF is guaranteed by design.

### AC WAVEFORMS



Waveform 1. The Input ( $S_n$ ) to Output ( $D_n$ ) Propagation Delays

### TEST CIRCUIT



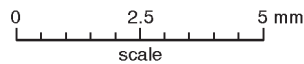
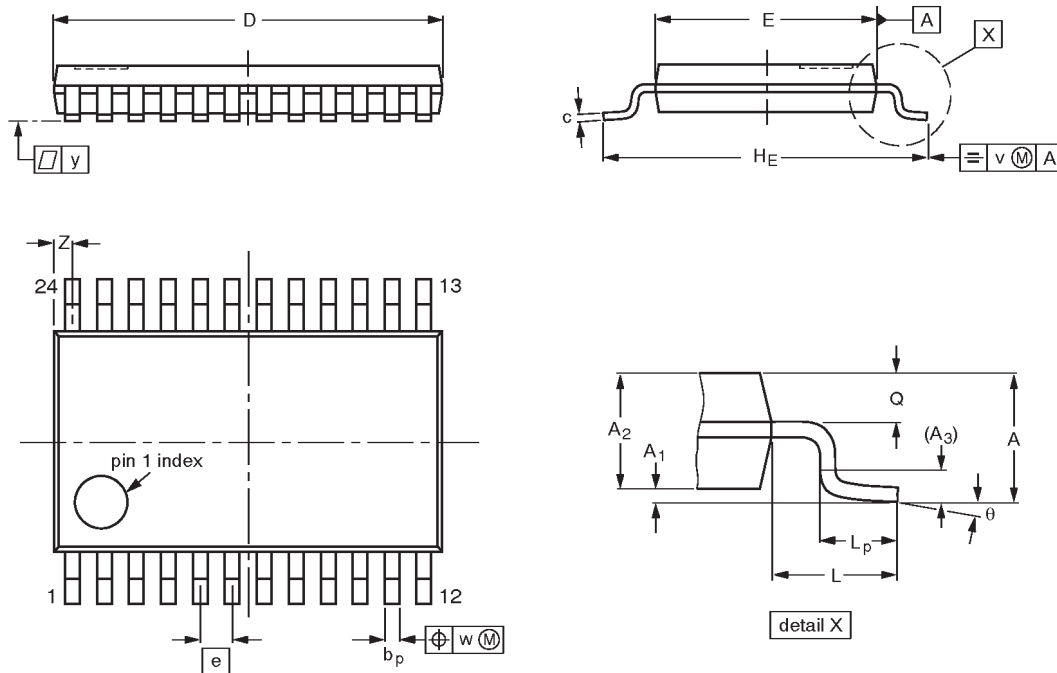
Waveform 2. Load circuit

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**TSSOP24:** plastic thin shrink small outline package; 24 leads; body width 4.4 mm

**SOT355-1**



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	7.9 7.7	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT355-1		MO-153AD				93-06-16 95-02-04

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## Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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Date of release: 08-00

Document order number:

9397 750 07462

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