



Improved, 8-Channel/Dual 4-Channel, CMOS Analog Multiplexers

DG408/DG409

General Description

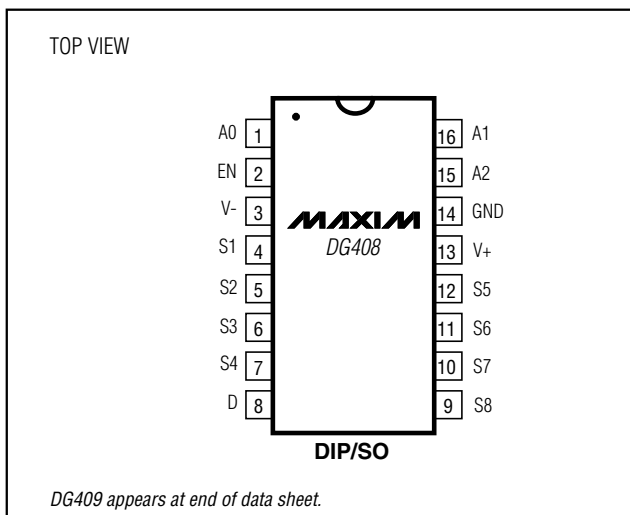
Maxim's redesigned DG408 and DG409 CMOS analog multiplexers now feature guaranteed matching between channels (8Ω max) and flatness over the specified signal range (9Ω max). These low on-resistance muxes (100Ω max) conduct equally well in either direction and feature guaranteed low charge injection (15pC max). In addition, these new muxes offer low input off-leakage current over temperature—less than 5nA at +85°C.

The DG408 is a 1-of-8 multiplexer/demultiplexer and the DG409 is a dual 4-channel multiplexer/demultiplexer. Both muxes operate with a +4.5V to +30V single supply and with ±4.5V to ±20V dual supplies. ESD protection is guaranteed to be greater than 2000V per Method 3015.7 of MIL-STD-883. These improved muxes are pin-compatible plug-in upgrades for the industry standard DG408 and DG409.

Applications

- Sample-and-Hold Circuits
- Test Equipment
- Guidance and Control Systems
- Communications Systems
- Data-Acquisition Systems
- Audio Signal Routing

Pin Configurations



Features

- ◆ Pin-Compatible Plug-In Upgrades for Industry Standard DG408/DG409
- ◆ Guaranteed Matching Between Channels, 8Ω Max
- ◆ Guaranteed On-Resistance Flatness, 9Ω Max
- ◆ Guaranteed Low Charge Injection, 15pC Max
- ◆ Low On-Resistance, 100Ω Max
- ◆ Input Leakage, 5nA Max at +85°C
- ◆ Low Power Consumption, 1.25mW Max
- ◆ Rail-to-Rail Signal Handling
- ◆ Digital Input Controls TTL/CMOS Compatible
- ◆ ESD Protection >2000V per Method 3015.7

Ordering Information

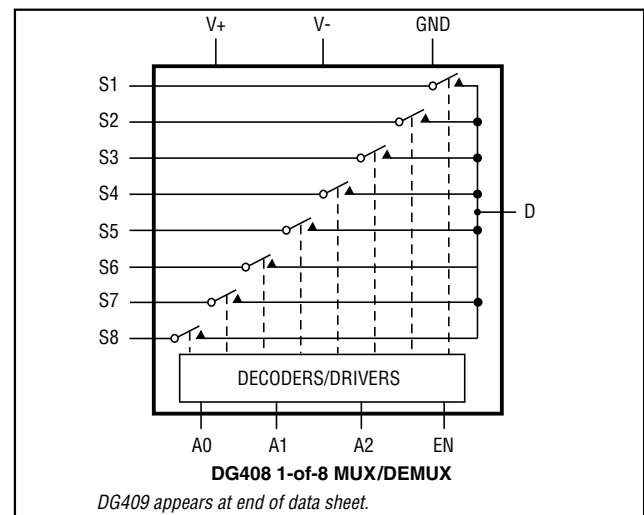
PART	TEMP. RANGE	PIN-PACKAGE
DG408CJ	0°C to +70°C	16 Plastic DIP
DG408CY	0°C to +70°C	16 Narrow SO
DG408C/D	0°C to +70°C	Dice*
DG408DJ	-40°C to +85°C	16 Plastic DIP
DG408DY	-40°C to +85°C	16 Narrow SO
DG408DK	-40°C to +85°C	16 CERDIP
DG408AK	-55°C to +125°C	16 CERDIP**

Ordering Information continued at end of data sheet.

* Contact factory for dice specifications.

** Contact factory for availability.

Functional Diagrams



Improved, 8-Channel/Dual 4-Channel, CMOS Analog Multiplexers

ABSOLUTE MAXIMUM RATINGS

Voltage Referenced to V-

V+-0.3V, 44V

GND-0.3V, 25V

Digital Inputs, S, D (Note 1).....(V- - 2V) to (V+ + 2V) or 30mA, (whichever occurs first)

Continuous Current (any terminal).....30mA

Peak Current, S, D (pulsed at 1ms, 10% duty cycle max)100mA

Continuous Power Dissipation (TA = +70°C)

Plastic DIP (derate 10.53mW/°C above +70°C)842mW

Narrow SO (derate 8.70mW/°C above +70°C)696mW

CERDIP (derate 10.00mW/°C above +70°C)800mW

Operating Temperature Ranges

DG408/DG409C_0°C to +70°C

DG408/DG409D_-40°C to +85°C

DG408/DG409AK-55°C to +125°C

Storage Temperature Range-65°C to +150°C

Lead Temperature (soldering, 10sec)+300°C

Note 1: Signals on S-, D-, EN, A0, A1, or A2 exceeding V+ or V- are clamped by internal diodes. Limit forward current to maximum current ratings.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Dual Supplies

(V+ = 15V, V- = -15V, GND = 0V, VAH = +2.4V, VAL = +0.8V, TA = TMIN to TMAX, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS		
SWITCH									
Analog Signal Range	VANALOG	(Note 3)		-15		15	V		
Drain-Source On-Resistance	rDS(ON)	IS = -1.0mA, VD = ±10V	TA = +25°C		60	100	Ω		
			TA = TMIN to TMAX			125			
On-Resistance Matching Between Channels	ΔrDS(ON)	IS = -1.0mA, VD = ±10V (Note 4)	TA = +25°C		1.5	8	Ω		
			TA = TMIN to TMAX			10			
On-Resistance Flatness	rFLAT	IS = -1.0mA, VD = ±5V or 0V	TA = +25°C		1.8	9	Ω		
			TA = TMIN to TMAX			12			
Source-Off Leakage Current (Note 5)	IS(OFF)	VD = +10V, VS = ±10V, VEN = 0V	TA = +25°C		-0.5	0.01	0.5	nA	
			TA = TMIN to TMAX	C, D		-5			5
				A		-50			50
Drain-Off Leakage Current (Note 5)	ID(OFF)	VD = ±10V, VS = +10V, VEN = 0V	DG408	TA = +25°C		-1	0.02	1	nA
				TA = TMIN to TMAX	C, D		-10		
			A			-100		100	
		DG409	TA = +25°C		-1	0.02	1		
			TA = TMIN to TMAX	C, D		-5		5	
				A		-50		50	
Drain-On Leakage Current (Note 5)	ID(ON)	VD = ±10V, VS = ±10V, sequence each switch on	DG408	TA = +25°C		-1	0.02	1	nA
				TA = TMIN to TMAX	C, D		-20		
			A			-100		100	
		DG409	TA = +25°C		-1	0.02	1		
			TA = TMIN to TMAX	C, D		-10		10	
				A		-50		50	

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ELECTRICAL CHARACTERISTICS—Dual Supplies (continued)

(V₊ = 15V, V₋ = -15V, GND = 0V, V_{AH} = +2.4V, V_{AL} = +0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
INPUT							
Input Current with Input Voltage High	I _{AH}	V _A = 2.4V or 15V		-1.0		1.0	μA
Input Current with Input Voltage Low	I _{AL}	V _{EN} = 0V or 2.4V, V _A = 0V		-1.0		1.0	μA
SUPPLY							
Power-Supply Range				±4.5		±20	V
Positive Supply Current	I ₊	V _{EN} = V _A = 0V or 4.5V	T _A = +25°C		16	30	μA
			T _A = T _{MIN} to T _{MAX}			75	
		V _{EN} = 2.4V, V _{A(ALL)} = 0V or 2.4V	T _A = +25°C		0.075	0.5	mA
			T _A = T _{MIN} to T _{MAX}			2	
Negative Supply Current	I ₋	V _{EN} = 2.4V, V _{A(ALL)} = 0V or 2.4V	T _A = +25°C		-1	1	μA
			T _A = T _{MIN} to T _{MAX}			-10	
DYNAMIC							
Transition Time	t _{TRANS}	Figure 2	T _A = +25°C		85	175	ns
			T _A = T _{MIN} to T _{MAX}			250	
Break-Before-Make Interval	t _{OPEN}	Figure 4	T _A = +25°C		10	40	ns
Enable Turn-On Time	t _{ON(EN)}	Figure 3	T _A = +25°C		85	150	ns
			T _A = T _{MIN} to T _{MAX}			225	
Enable Turn-Off Time	t _{OFF(EN)}	Figure 3	T _A = +25°C			150	ns
			T _A = T _{MIN} to T _{MAX}			300	
Charge Injection (Note 3)	Q	C _L = 1.0nF, V _S = 0V, R _S = 0Ω, Figure 5	T _A = +25°C		2	15	pC
Off Isolation (Note 6)	V _{ISO}	V _{EN} = 0V, R _L = 1kΩ, f = 100kHz, Figure 6	T _A = +25°C		-75		dB
Crosstalk Between Input Channels	V _{CT}	V _{EN} = 2.4V, f = 100kHz, V _{GEN} = 1V _{P-P} , R _L = 1kΩ, Figure 7	T _A = +25°C		-92		dB
Logic Input Capacitance	C _{IN}	f = 1MHz	T _A = +25°C		8		pF
Source-Off Capacitance	C _{S(OFF)}	f = 1MHz, V _{EN} = V _S = 0V, Figure 8	T _A = +25°C		3		pF
Drain-Off Capacitance	C _{D(OFF)}	f = 1MHz, V _{EN} = 0.8V V _D = 0V, Figure 8	DG408	T _A = +25°C		26	pF
			DG409			14	
Drain-On Capacitance	C _{D(ON)} + C _{S(ON)}	f = 1MHz, V _{EN} = 2.4V V _D = 0V, Figure 8	DG408	T _A = +25°C		37	pF
			DG409			25	

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ELECTRICAL CHARACTERISTICS—Single Supply

(V+ = 12V, V- = 0V, GND = 0V, VAH = +2.4V, VAL = +0.8V, TA = TMIN to TMAX, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
SWITCH							
Analog Signal Range	VANALOG	(Note 3)		0		12	V
Drain-Source On-Resistance	rDS(ON)	IS = -1.0mA VD = 3V or 10V	TA = +25°C		120	175	Ω
DYNAMIC							
Transition Time (Note 3)	tTRANS	VS1 = 8V, VS8 = 0V, VA = 0V, Figure 2	TA = +25°C		115	450	ns
Enable Turn-On Time (Note 3)	tON(EN)	VAL = 0V, VS1 = 5V, Figure 3	TA = +25°C		100	600	ns
Enable Turn-Off Time (Note 3)	tOFF(EN)	VAL = 0V, VS1 = 5V, Figure 3	TA = +25°C		75	300	ns
Charge Injection	Q	CL = 1.0nF, VS = 0V, RS = 0Ω	TA = +25°C		2		pC

Note 2: The algebraic convention where the most negative value is a minimum and the most positive value a maximum is used in this data sheet.

Note 3: Guaranteed by design.

Note 4: $\Delta R_{ON} = R_{ON(MAX)} - R_{ON(MIN)}$. On-resistance match between channels and flatness are guaranteed only with specified voltages. Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured at the extremes of the specified analog signal range.

Note 5: Leakage parameters are 100% tested at the maximum rated hot temperature and guaranteed by correlation at +25°C.

Note 6: Off isolation = $20 \log V_D/V_S$, where V_D = output and V_S = input to off switch.

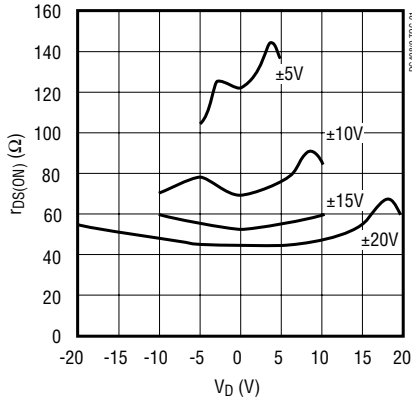
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Typical Operating Characteristics

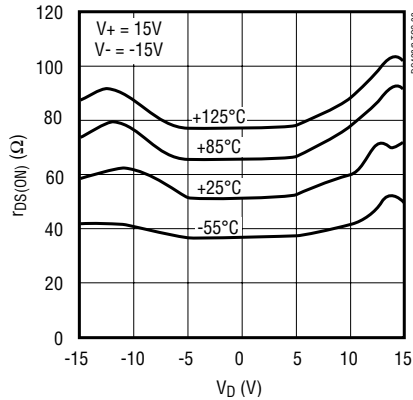
($T_A = +25^\circ\text{C}$, unless otherwise noted.)

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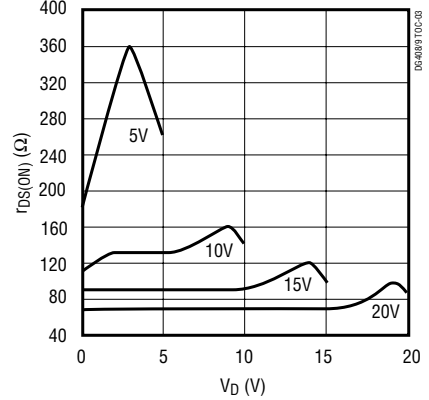
ON-RESISTANCE vs. V_D (DUAL SUPPLIES)



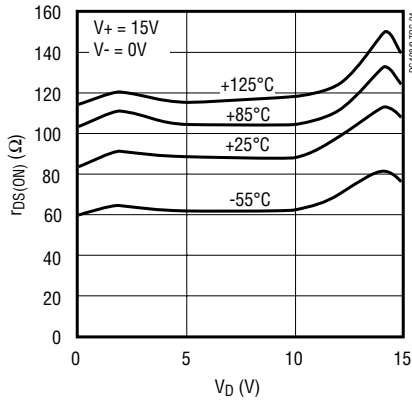
ON-RESISTANCE vs. V_D AND TEMPERATURE (DUAL SUPPLIES)



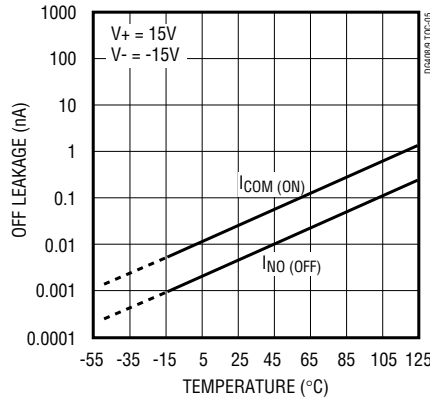
ON-RESISTANCE vs. V_D (SINGLE SUPPLY)



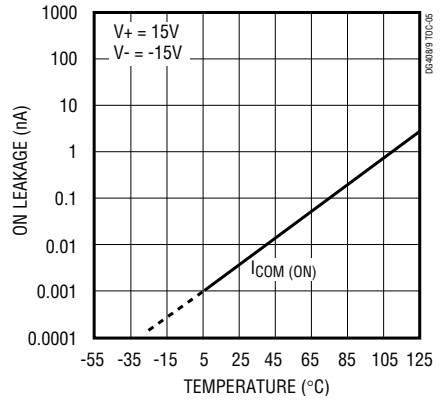
ON-RESISTANCE vs. V_D AND TEMPERATURE (SINGLE SUPPLY)



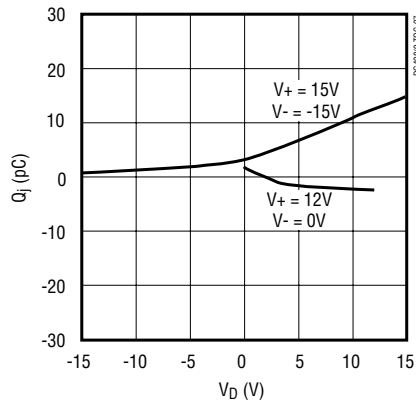
OFF LEAKAGE vs. TEMPERATURE



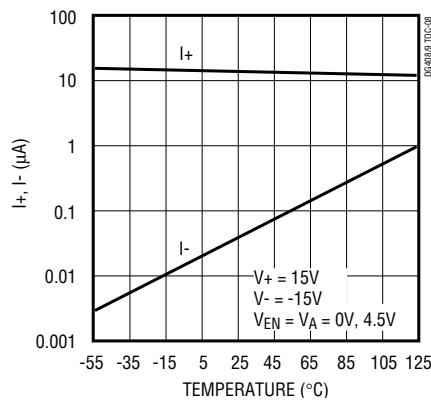
ON LEAKAGE vs. TEMPERATURE



CHARGE INJECTION vs. V_D



SUPPLY CURRENT vs. TEMPERATURE



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Pin Description

PIN		NAME	FUNCTION
DG408	DG409		
1, 15, 16	—	A0, A2, A1	Address Inputs
—	1, 16	A0, A1	Address Inputs
2	2	EN	Enable Input
3	3	V-	Negative Supply Voltage Input
4–7	—	S1–S4	Bidirectional Analog Inputs
—	4–7	S1A–S4A	Bidirectional Analog Inputs
8	—	D	Bidirectional Analog Output
—	8, 9	DA, DB	Bidirectional Analog Outputs
9–12	—	S8–S5	Bidirectional Analog Inputs
—	10–13	S4B–S1B	Bidirectional Analog Inputs
13	14	V+	Positive Supply Voltage Input
14	15	GND	Ground

Applications Information

Operation with Supply Voltages Other than 15V

Using supply voltages less than $\pm 15\text{V}$ reduces the analog signal range. The DG408/DG409 switches operate with $\pm 4.5\text{V}$ to $\pm 20\text{V}$ bipolar supplies or with a $+4.5\text{V}$ to $+40\text{V}$ single supply. Connect V- to GND when operating with a single supply. Both device types can also operate with unbalanced supplies, such as $+24\text{V}$ and -5V . The *Typical Operating Characteristics* graphs show typical on-resistance with 20V, 15V, 10V, and 5V supplies. (Switching times increase by a factor of two or more for operation at 5V.)

Overvoltage Protection

Proper power-supply sequencing is recommended for all CMOS devices. Do not exceed the absolute maximum ratings, because stresses beyond the listed ratings may cause permanent damage to the devices. Always sequence V+ on first, then V-, followed by the logic inputs, S or D. If power-supply sequencing is not possible, add two small signal diodes in series with supply pins for overvoltage protection (Figure 1). Adding diodes reduces the analog signal range to 1V below V+ and 1V above V-, but does not affect the devices' low switch resistance and low leakage characteristics. Device operation is unchanged, and the difference between V+ and V- should not exceed $+44\text{V}$.

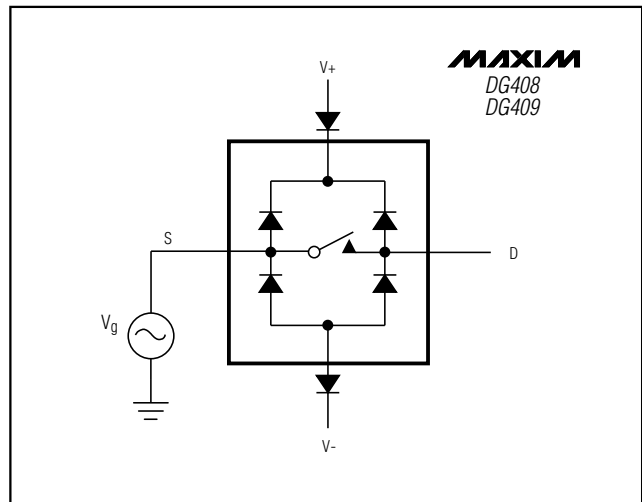


Figure 1. Overvoltage Protection Using External Blocking Diodes

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Test Circuits/Timing Diagrams

DG408/DG409

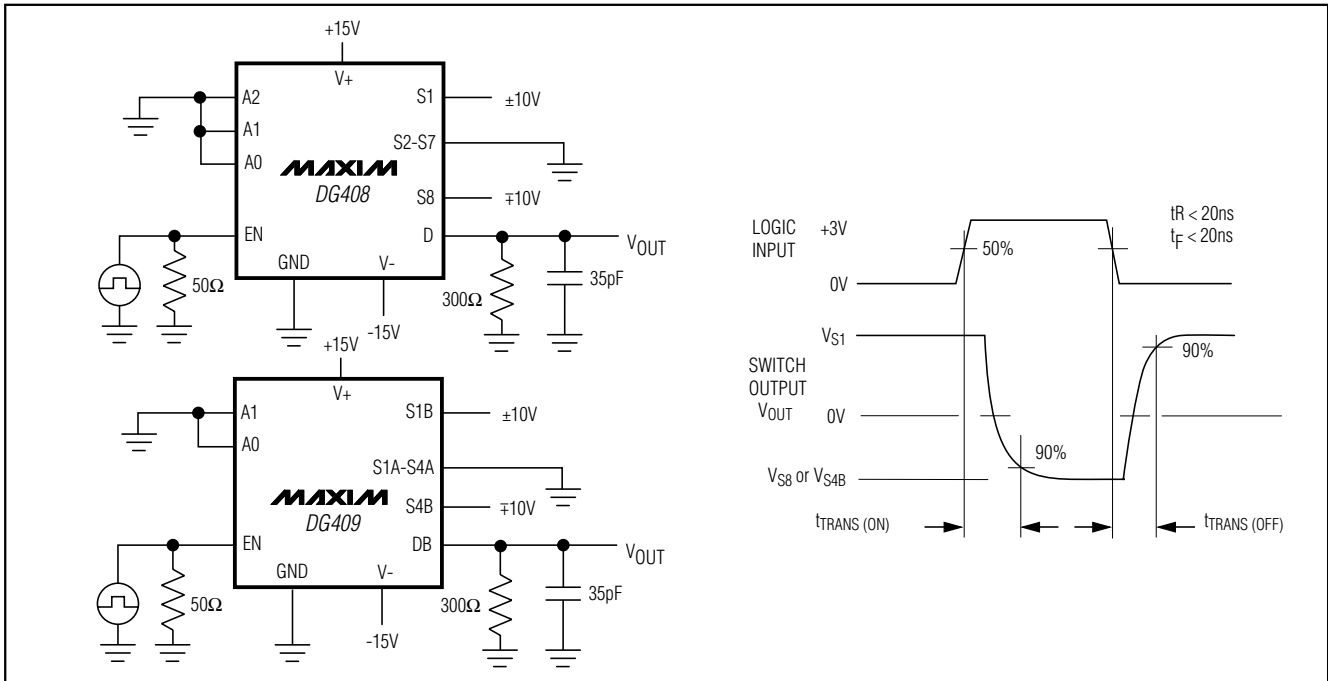


Figure 2. Transition Time

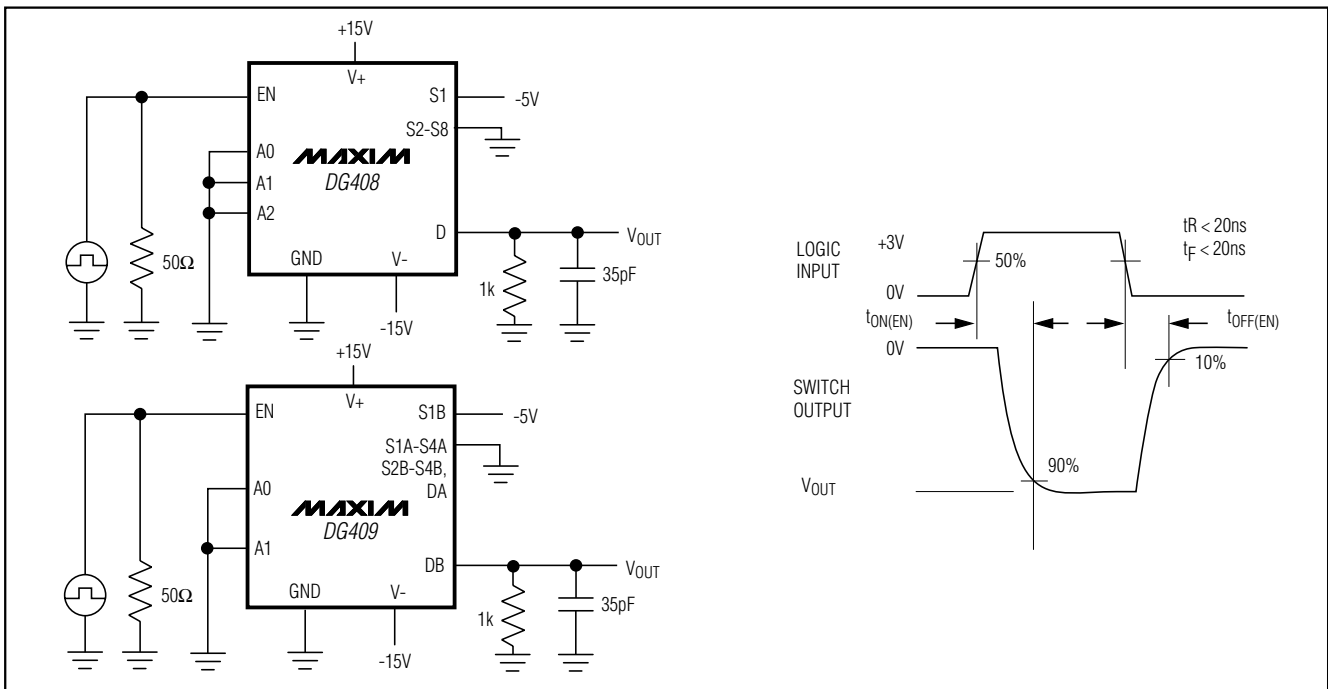


Figure 3. Enable Switching Time

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Test Circuits/Timing Diagrams (continued)

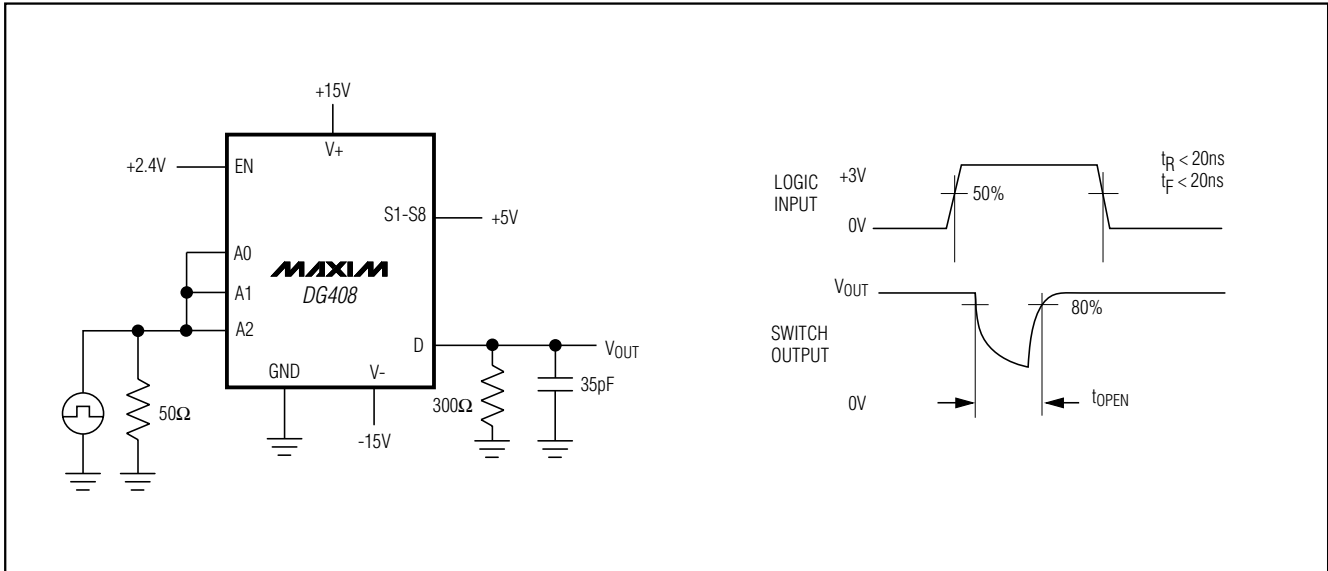


Figure 4. Break-Before-Make Interval

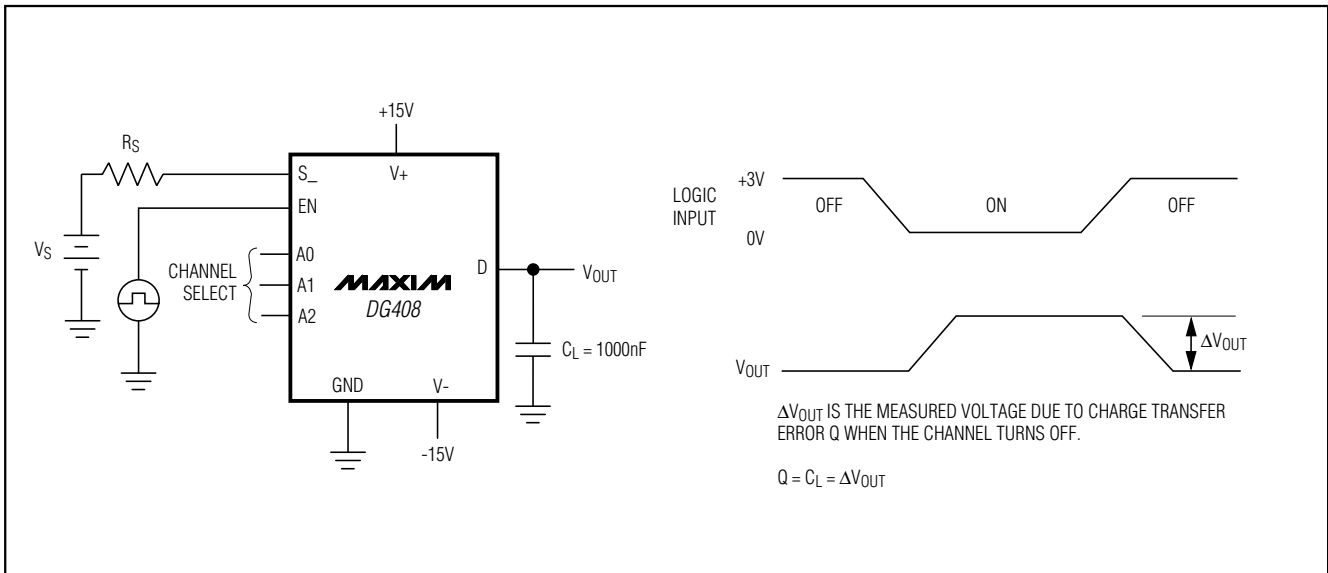


Figure 5. Charge Injection

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Test Circuits/Timing Diagrams (continued)

DG408/DG409

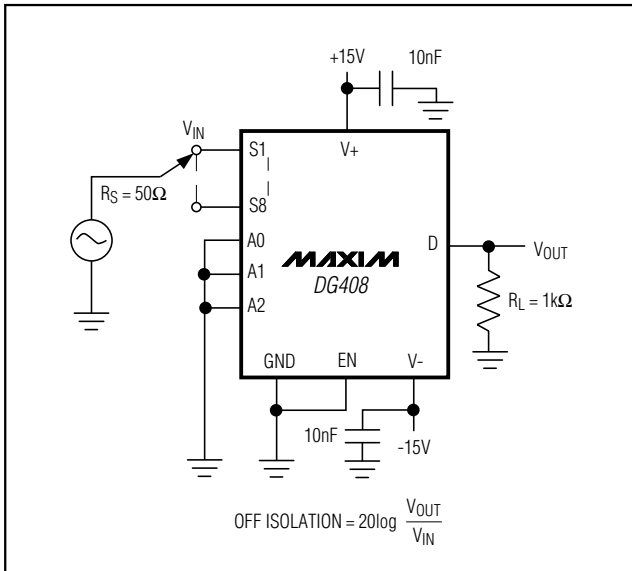


Figure 6. Off Isolation

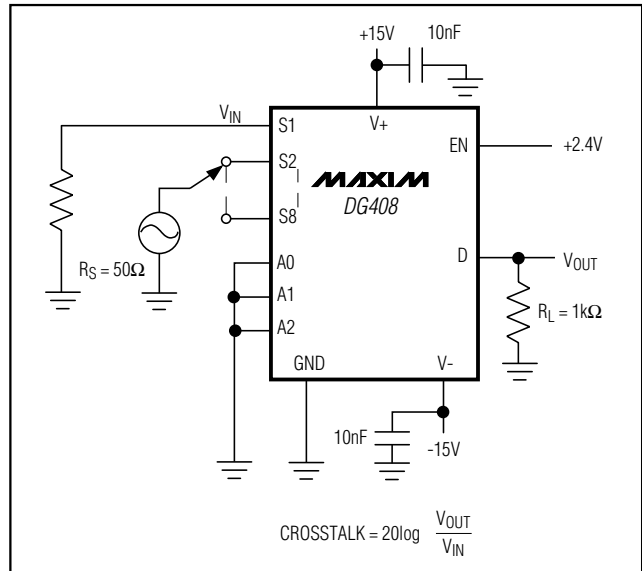


Figure 7. Crosstalk

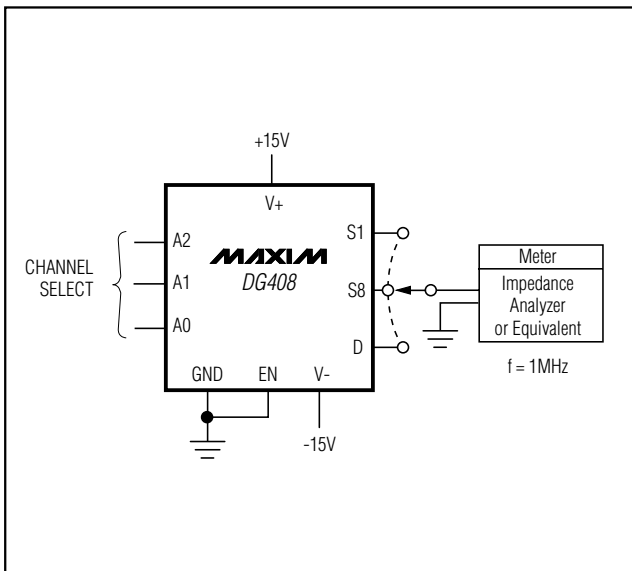
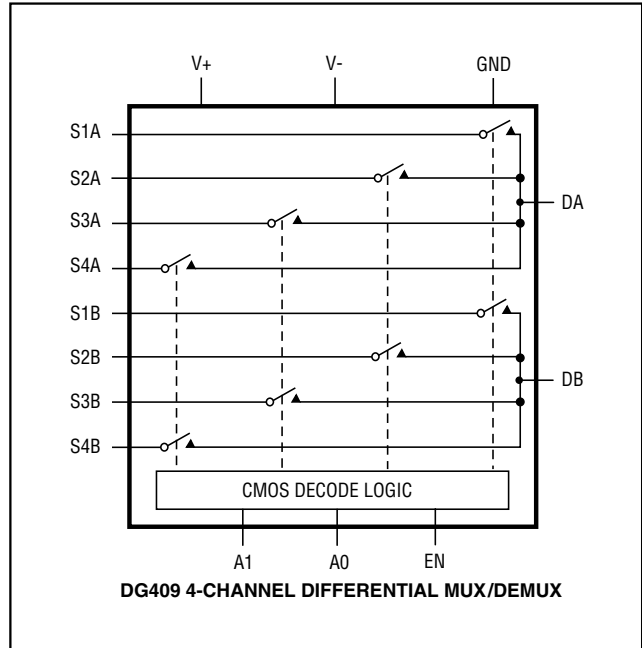
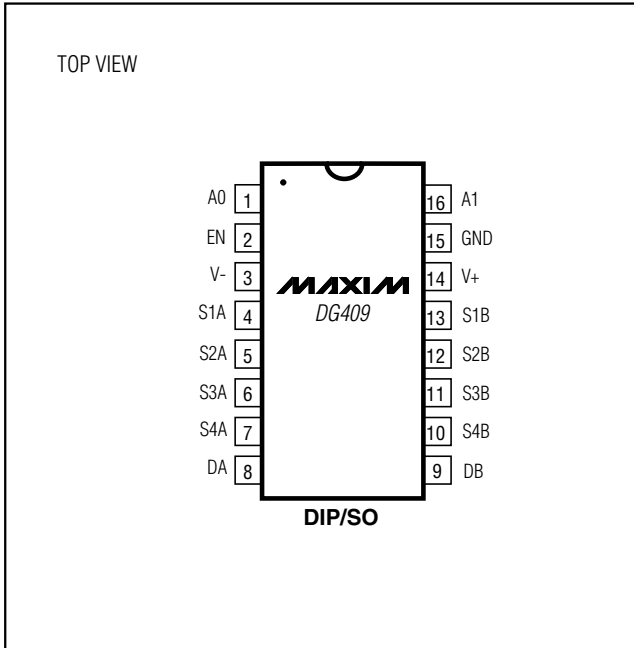


Figure 8. Source/Drain Capacitance

Improved, 8-Channel/Dual 4-Channel, CMOS Analog Multiplexers

Pin Configurations/Functional Diagrams/Truth Tables (continued)



A2	A1	A0	EN	ON SWITCH
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

DG408

LOGIC "0" $V_{AL} \leq 0.8V$, LOGIC "1" $V_{AH} \geq 2.4V$

A1	A0	EN	ON SWITCH
X	X	0	None
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

DG409

LOGIC "0" $V_{AL} \leq 0.8V$, LOGIC "1" $V_{AH} \geq 2.4V$

Improved, 8-Channel/Dual 4-Channel, CMOS Analog Multiplexers

DG408/DG409

_ Ordering Information (continued)

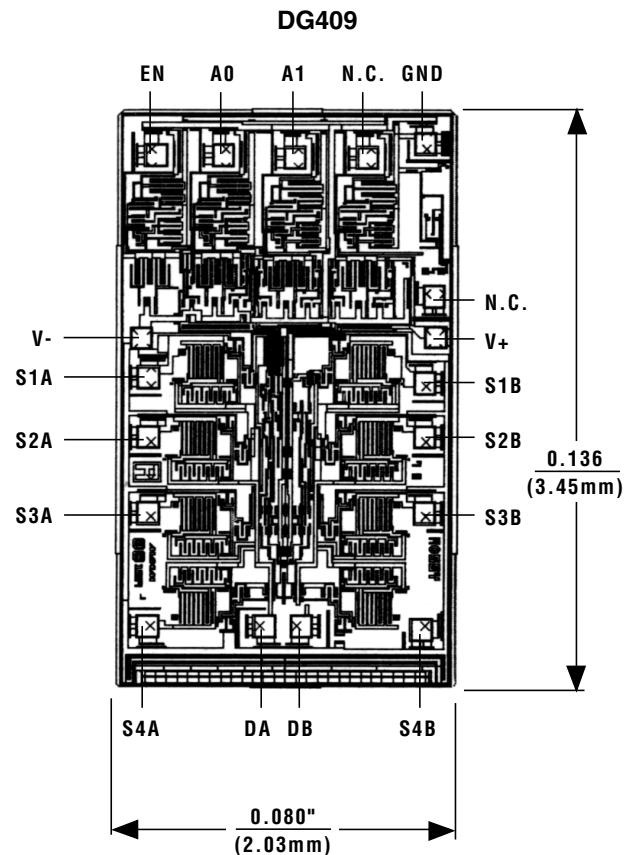
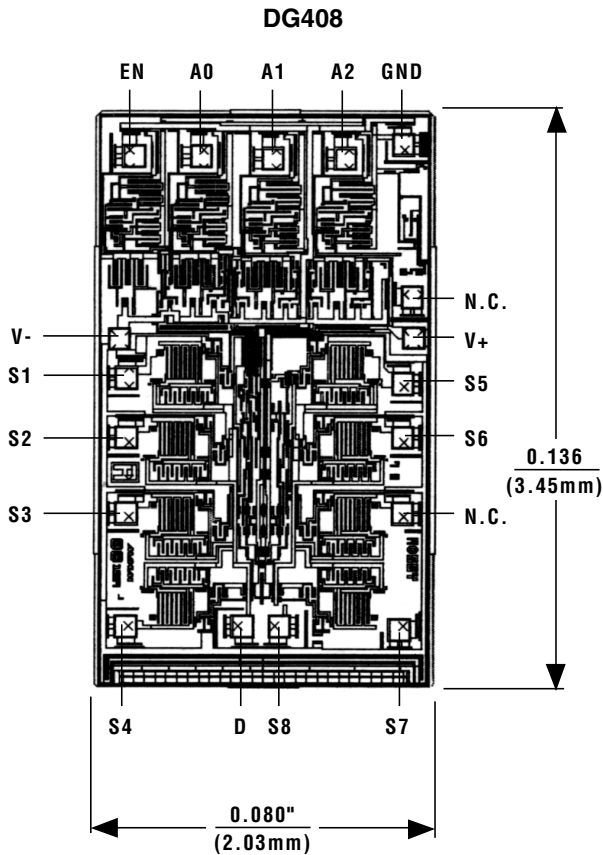
PART	TEMP. RANGE	PIN-PACKAGE
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DG409CY	0°C to +70°C	16 Narrow SO
DG409C/D	0°C to +70°C	Dice*
DG409DJ	-40°C to +85°C	16 Plastic DIP
DG409DY	-40°C to +85°C	16 Narrow SO
DG409DK	-40°C to +85°C	16 CERDIP
DG409AK	-55°C to +125°C	16 CERDIP**

* Contact factory for dice specifications.

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Improved, 8-Channel/Dual 4-Channel, CMOS Analog Multiplexers

Chip Topographies



N.C. = NO INTERNAL CONNECTION

TRANSISTOR COUNT: 122
SUBSTRATE CONNECTED TO V+

TRANSISTOR COUNT: 122
SUBSTRATE CONNECTED TO V+

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