HA13532NT

Three-Phase Stepping Motor Control IC

HITACHI

ADE-207-121A (Z)
2nd Edition
July 1996

Description

The HA13532NT is an IC for control a three-phase stepping motor.

Functions

- PWM current control
- Low-voltage inhibit (LVI)
- Three-bit D/A converter for current programming
- Motor on/off
- Selectable 2-phase or 2-3-phase exciting

Features

- Wide operating voltage range
- Few external components

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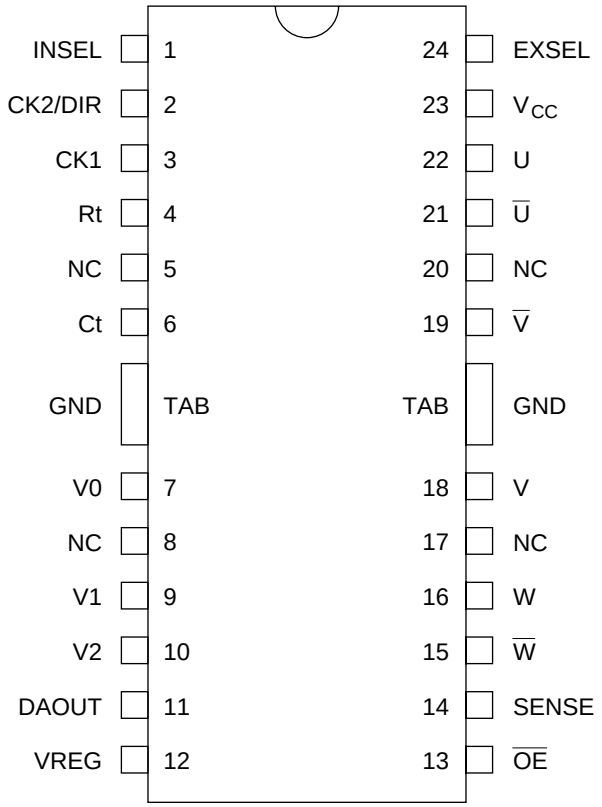
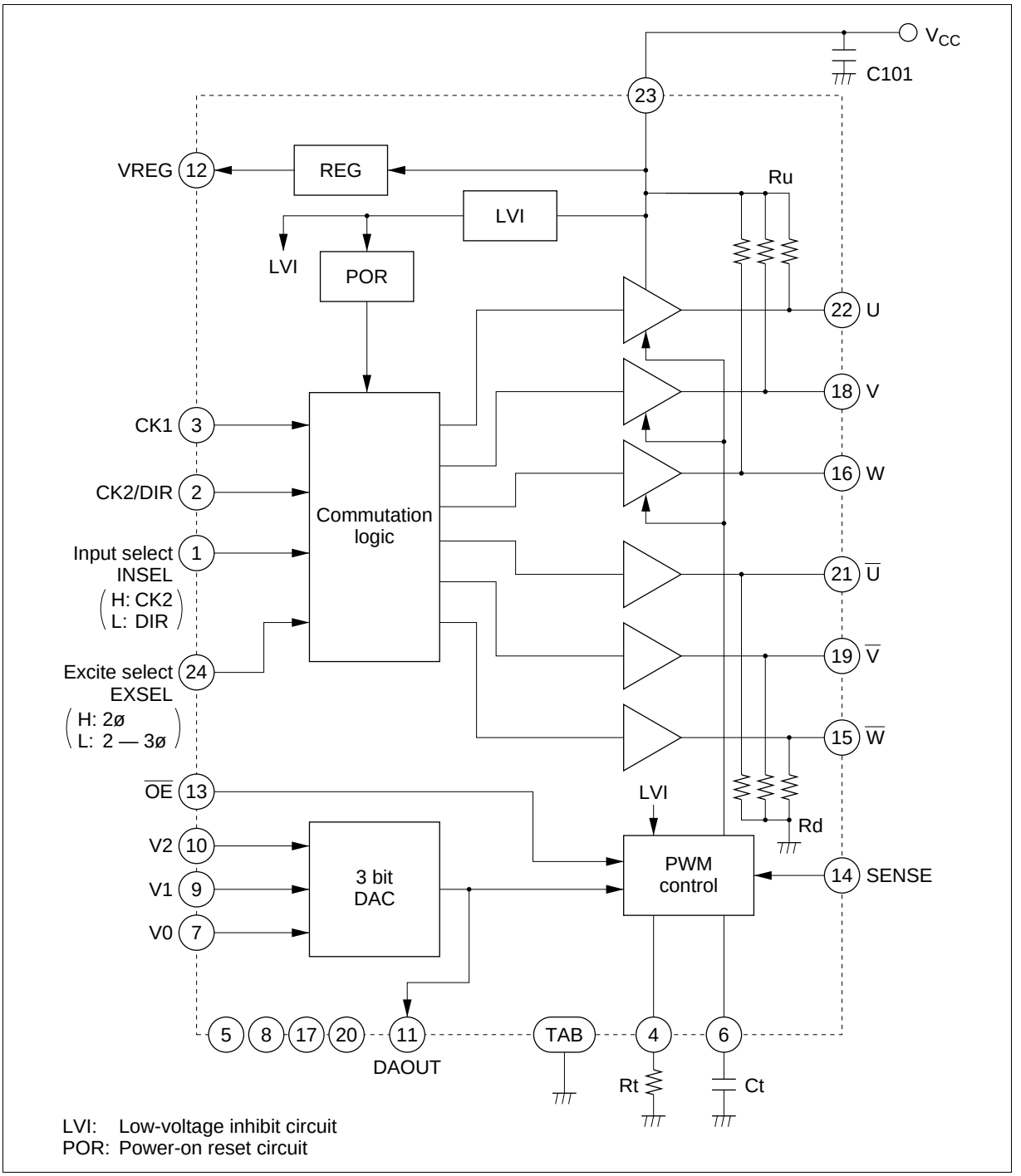
Pin Arrangement



(Top view)

Block Diagram

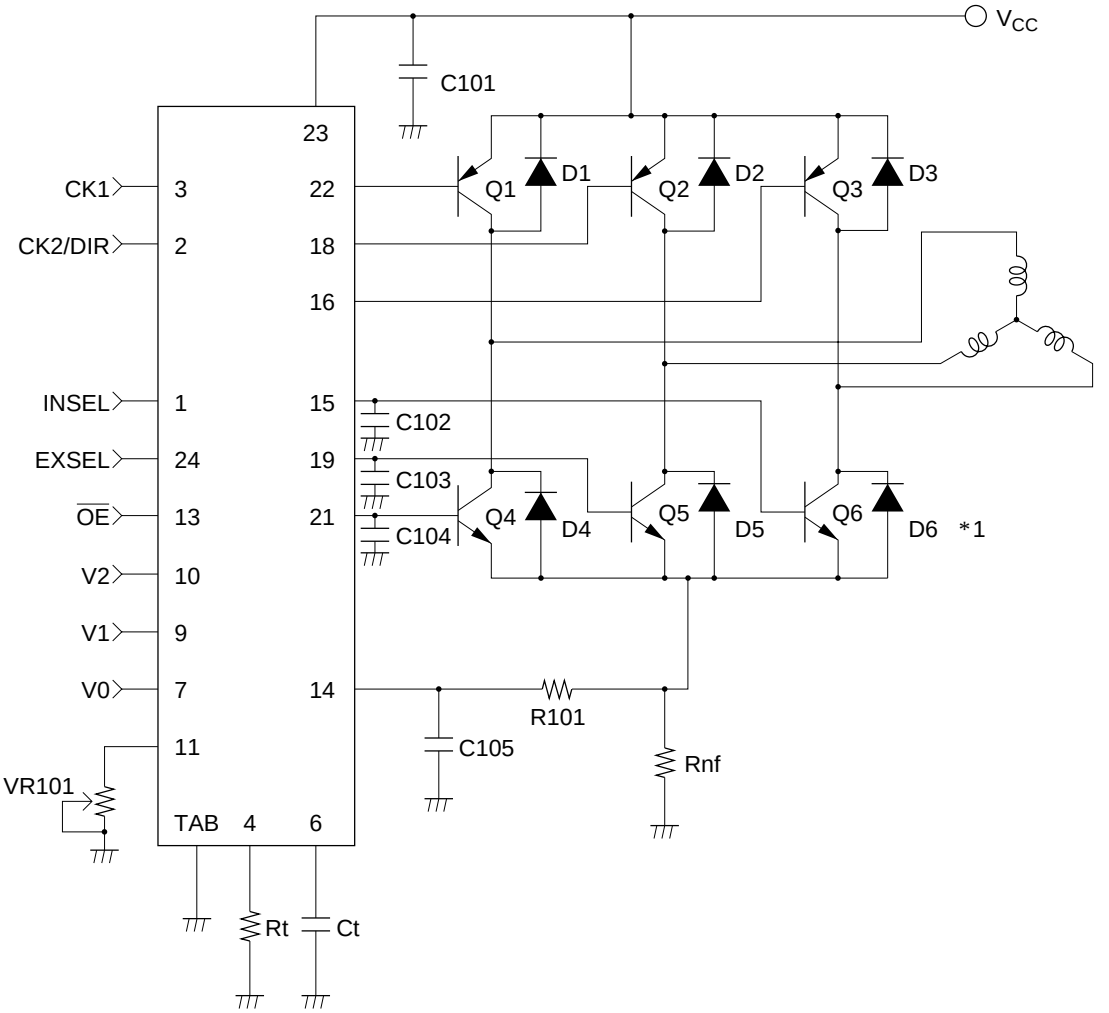


LVI: Low-voltage inhibit circuit
POR: Power-on reset circuit

Pin Description

Pin No.	Pin Name	Function	Pin Voltage
1	INSEL	Selects pin 2 input: CK2 if high; DIR if low (see timing diagrams)	V_{TH} = 2.5 V typ
2	CK2/DIR	CK2 or DIR input (see timing diagrams)	V_{TH} = 2.5 V typ
3	CK1	CK1 input (see timing diagrams)	V_{TH} = 2.5 V typ
4	Rt	Reference value for 3-phase output current and Ct charge/discharge current	4.8 V typ
5	NC	No connection	
6	Ct	Time constant for PWM carrier frequency	
7	V0	Voltage programming input to DAC (LSB)	V_{TH} = 2.5 V typ
8	NC	No connection	
9	V1	Voltage programming input to DAC	V_{TH} = 2.5 V typ
10	V2	Voltage programming input to DAC (MSB)	V_{TH} = 2.5 V typ
11	DAOUT	DAC output	
12	VREG	Regulated output	4.8 V typ (@I = 2 mA)
13	$\overline{OE}$	Output enable: low enables PWM output phases U, V, and W; high gives high impedance	V_{TH} = 2.5 V typ
14	SENSE	Current feedback	0 V min, 5.0 V max
15	$\overline{W}$	Phase-W lower-arm output	
16	W	Phase-W upper-arm output	
17	NC	No connection	
18	V	Phase-V upper-arm output	
19	$\overline{V}$	Phase-U lower-arm output	
$\overline{20}$	$\overline{NC}$	No connection	
21	$\overline{U}$	Phase-U lower-arm output	
22	U	Phase-U upper-arm output	
23	V_{CC}	Power supply	10 V min, 27.6 V max
24	EXSEL	Selects exciting mode: 2-phase if high; 2-3-phase if low (see timing diagrams)	V_{TH} = 2.5 V typ

Application Circuit



Notes: 1. Use high-speed diodes for D4, D5, and D6.

External Conponents

Symbol	Recommended Value	Purpose	Notes
Rnf	0.11 Ω ≤ Rnf ≤ 0.33 Ω	Current sensing	1
Rt	51 k Ω	Reference current programming	2
Ct	1000 pF	Time constant for PWM carrier frequency	3
C_{101}	≥ 0.1 µF	Power supply decoupling	
C_{102}, C_{103}, C_{104}	0.01 µF	Penetration current control	4
C_{105}	1000 pF	Current sensing filter	
R_{101}	750 Ω		
VR_{101}	100 kΩ	Motor current little adjustment	

Notes: 1. The maximum motor drive current is:

$$Imax \approx \pm \frac{Vdac + Voffs}{Rnf} \quad (1)$$

where, Vdac: DAC output voltage (see electrical characteristics)
Voffs: Offset voltage (see electrical characteristics)

2. The output sink current Iosnk, output source current Iosrc, and Ct charge/discharge currents Ict+ and Ict– are calculated as follows:
where, set Rt to be 2.5kΩ or higher.

$$Iosnk \approx \frac{50Vrt}{Rt} - \frac{Vbe}{Ru} \quad (2)$$

$$Iosrc \approx \frac{50Vrt}{Rt} - \frac{Vbe}{Rd} \quad (3)$$

$$Ict+, Ict- \approx \frac{Vrt}{Rt} \quad (4)$$

where, Vrt: Rt voltage (see electrical characteristics)
Ru: pull-up resistance (see electrical characteristics)
Rd: pull-down resistance (see electrical characteristics)
Vbe: base-emitter voltage of driven transistor

3. The PWM carrier frequency fc is calculated as follows:

$$fc \approx \frac{Ict}{2Ct\,(Vcth - Vctl)} \quad (5)$$

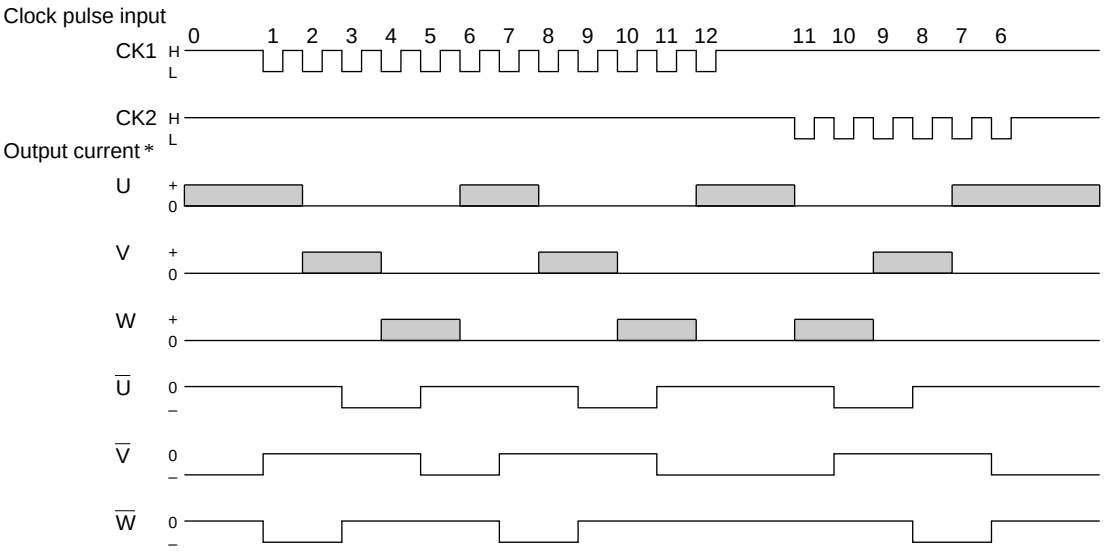
$$\approx \frac{Vrt}{2CtRt\,(Vcth - Vctl)} \quad (6)$$

where, Vcth: Ct high voltage (see electrical characteristics)
Vctl: Ct low voltage (see electrical characteristics)

4. Values of C_{102}, C_{103}, C_{104}, C_{105}, R_{101} are different from using power transistor

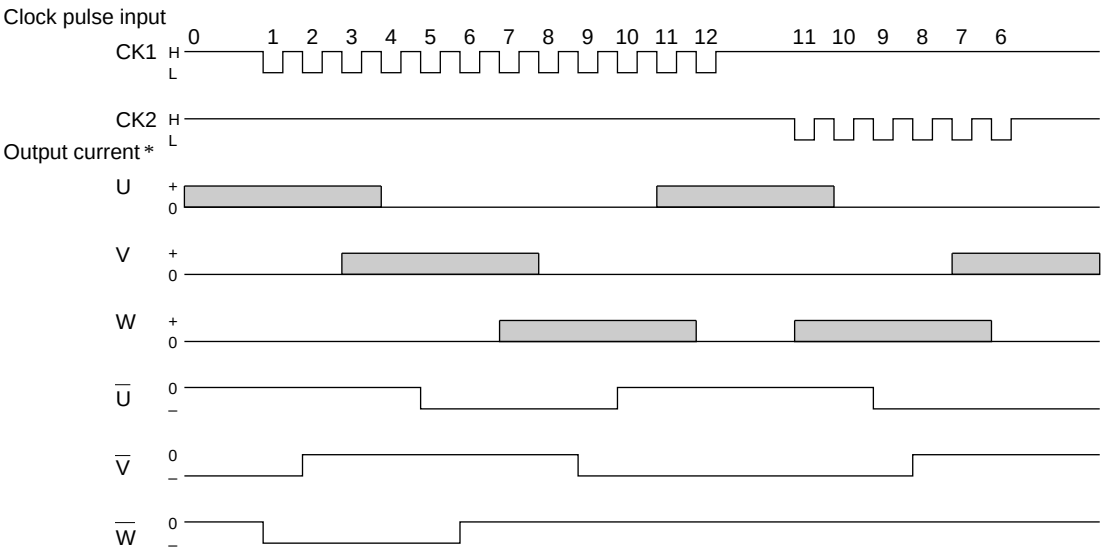
Timing Waveforms

Two Clock Pulse Inputs, Two-Phase Exciting (INSEL High, EXSEL High)



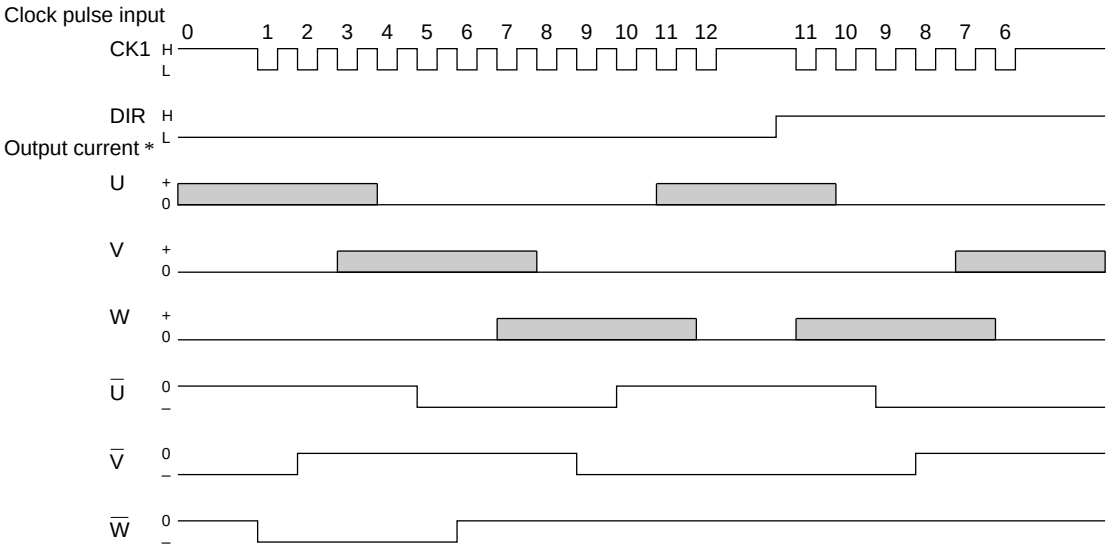
Note: * Initialized with U and $\overline{V}$ on at power-up.

Two Clock Pulse Inputs, Two-Three-Phase Exciting (INSEL High, EXSEL Low)



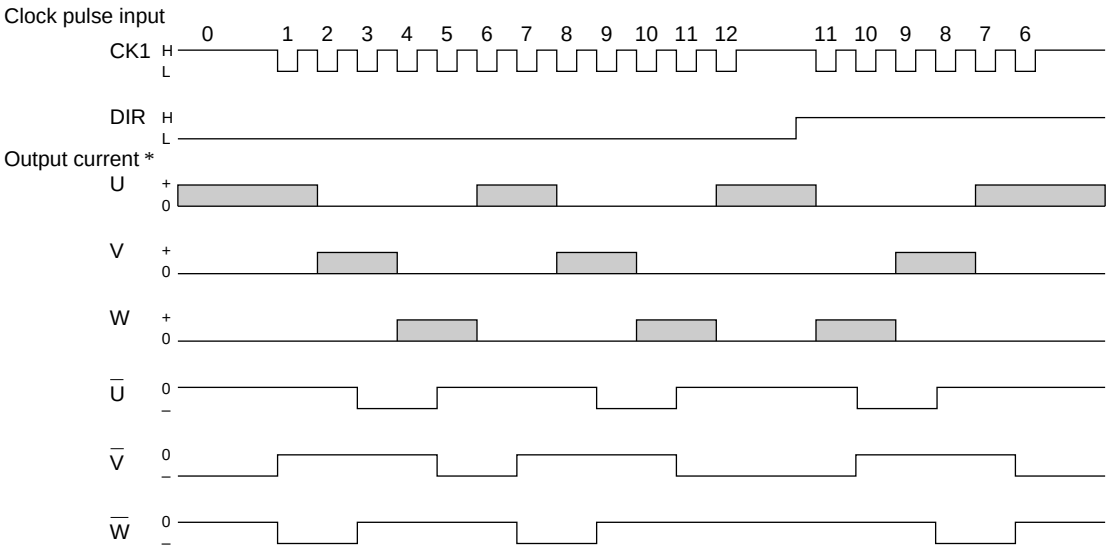
Note: * Initialized with U and $\overline{V}$ on at power-up.

One Clock Pulse Input, Two-Three-Phase Exciting (INSEL Low, EXSEL Low)



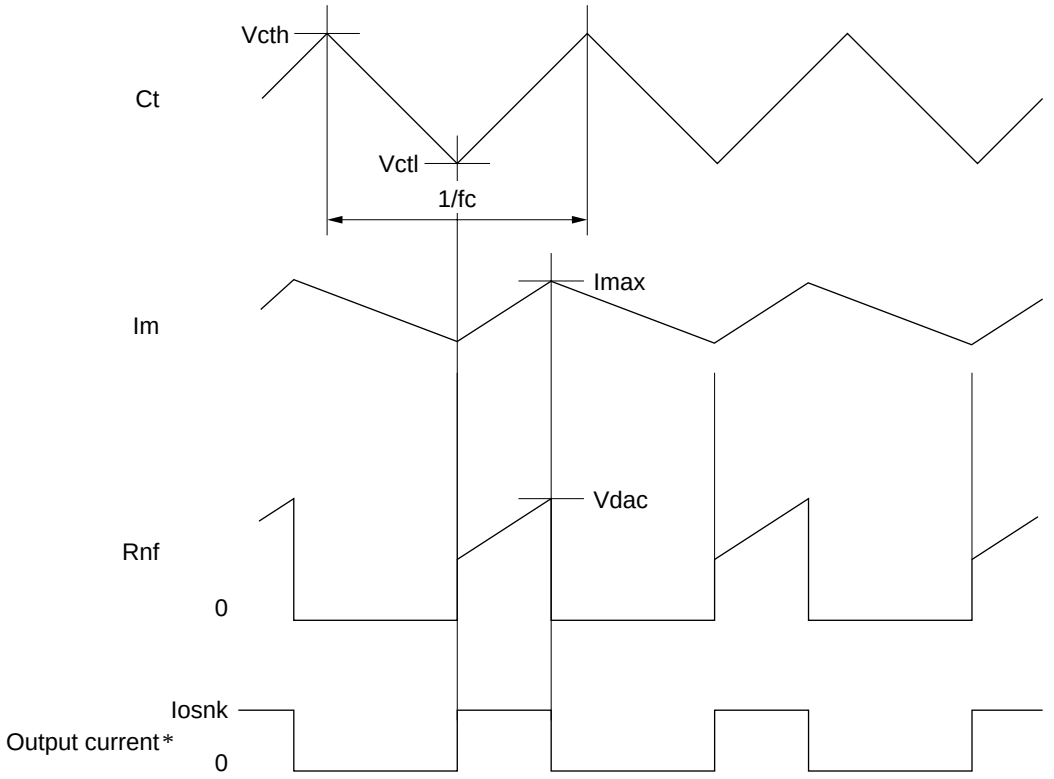
Note: * Initialized with U and $\overline{V}$ on at power-up.

One Clock Pulse Input, Two-Phase Exciting (INSEL Low, EXSEL High)



Note: * Initialized with U and $\overline{V}$ on at power-up.

PWM Control



Note: * Only phase U is shown.

Absolute Maximum Ratings

Item	Symbol	Rating	Unit	Notes
Power supply voltage	V_{CC}	30	V	1
Input voltage	Vin	7	V	2
Power dissipation	P_T	910	mW	3
Operating temperature	Topr	–10 to +70	°C	
Storage temperature	Tstg	–55 to +125	°C	
Output current	Ireg	2	mA	

Notes: 1. The operating power supply voltage range is V_{CC} = 10 V to 27.6 V.
2. Applies to logic and DAC input pins.
3. Permitted at Ta = 70°C, if thermal resistance is as below:
$\theta j - a \leq 60°C/W$ (glass-epoxy board)

Electrical Characteristics (Ta = 25°C, V_{CC} = 24 V)

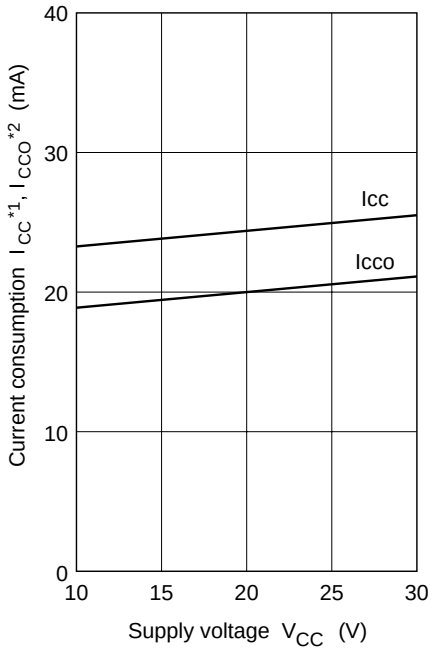
Item		Symbol	Min	Typ	Max	Unit	Test Conditions	Pins	Notes
Current consumption		I_{CCO}	—	—	33	mA	V_{CC} = 30 V, $\overline{OE}$ = H	23	1
		I_{CC}	—	—	41	mA	V_{CC} = 30 V, $\overline{OE}$ = L		
REG	Output voltage	Vreg	4.4	4.8	5.2	V	Ireg = 2 mA	12	
	Load regulation	ΔVreg	—	—	±0.1	V	Ireg = 0 mA to 2 mA		
Logic	Input current	Iin	–10	—	1	µA	Vin = 0 V to 7 V	1, 2, 3, 13, 24	
			–1	—	10	µA		7, 9, 10	
	Low voltage level	Vil	—	—	1.35	V		1, 2, 3, 7, 9, 10, 13,	
	High voltage level	Vih	3.65	—	—	V		24	
DAC	Outout voltage	Vdac	200	230	260	mV	(V2, V1, V0) = (H, L, L)	11	
			116	146	176	mV	(V2, V1, V0) = (L, H, L)		
			75	105	135	mV	(V2, V1, V0) = (L, L, H)		
			33	63	93	mV	(V2, V1, V0) = (L, L, L)		
PWM control	Input current	Isens	—	—	±2	µA	Vsens = 0 V to 5 V	14	
	Offset voltage	Voffs	—	—	±10	mV			2
	Rt voltage	Vrt	4.4	4.8	5.2	V	Rt = 51 kΩ	4	
	Ct change current	Ict+	84	94	104	µA	Rt = 51 kΩ, Vct = 3.75 V	6	
	Ct discharge current	Ict–	84	94	104	µA	Rt = 51 kΩ, Vct = 3.75 V		

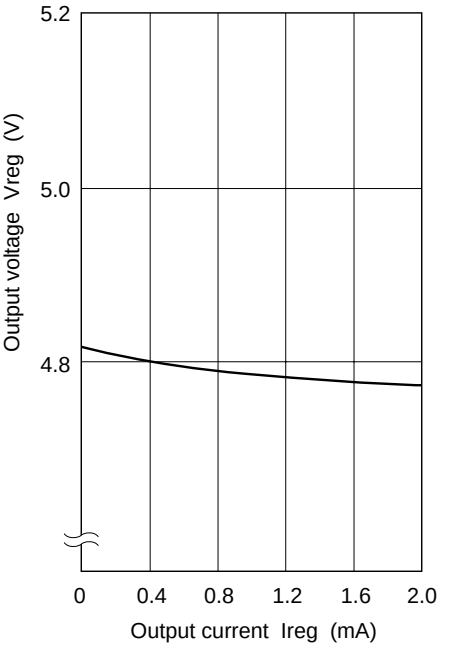
Electrical Characteristics (Ta = 25°C, V_{CC} = 24 V) (Cont)

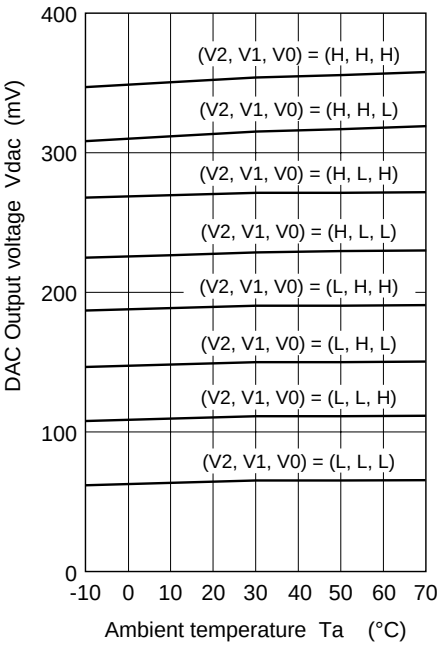
Item		Symbol	Min	Typ	Max	Unit	Test Conditions	Pins	Notes
PWM control	Ct high voltage	Vcth	4.3	4.8	5.3	V		6	3
	Ct low voltage	Vctl	2.3	2.78	3.3	V			
	Carrier frequency	fc	18.6	23.3	28.0	kHz	Rt = 51 kΩ, Ct = 1000 pF		
3-pahse output	Output sink current	Iosnk	2.0	3.1	4.2	mA	$V_O = V_{CC} – 1.5$ V, Rt = 51 kΩ	16, 18, 22	
	Output source current	Iosrc	2.0	3.1	4.2	mA	V_O = 1.5 V, Rt = 51 kΩ	15, 19, 21	
	Output leakage current	Ioff	—	—	±10	µA	V_{CC} = 30 V, $V_O = V_{CC}$	16, 18, 22	
			—	—	±10	µA	V_{CC} = 30 V, V_O = 0 V	15, 19, 21	
	Pull-up resistance	Ru	700	950	1200	Ω		16, 18, 22	
	Pull-down resistance	Rd	700	950	1200	Ω		15, 19, 21	
	Transient response time	t_{phl}	—	—	6.0	µs		15, 16, 18, 19, 21, 22	
		t_{plh}	—	—	6.0	µs			
LVI	Operating voltage	Vlvi	8.0	—	10	V		23	
	Hysteresis	Vhys	—	0.3	—	V			

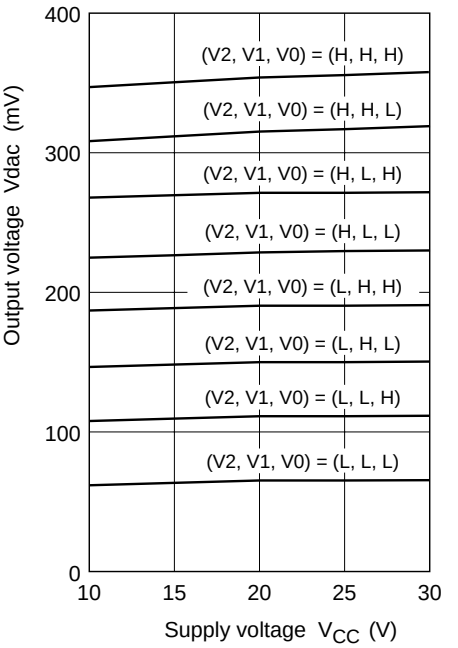
Notes: 1. Measured with pins 12, 15, 16, 18, 19, 21, and 22 open.
2. Offset between pins 11 and 14.
3. See timing diagrams.

Reference Data

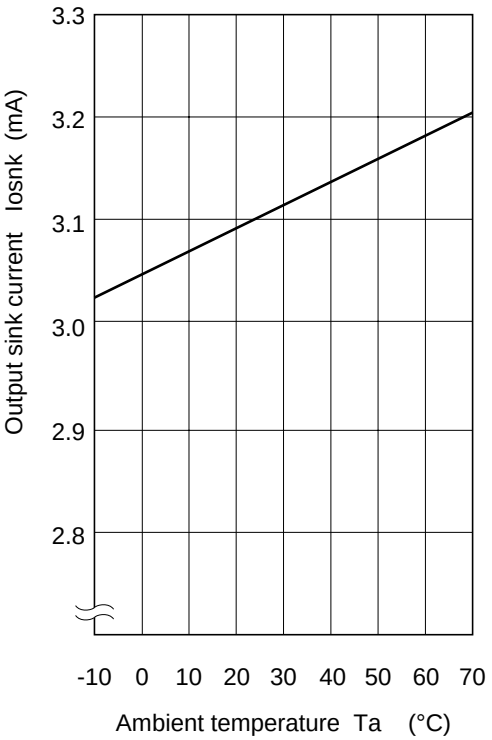


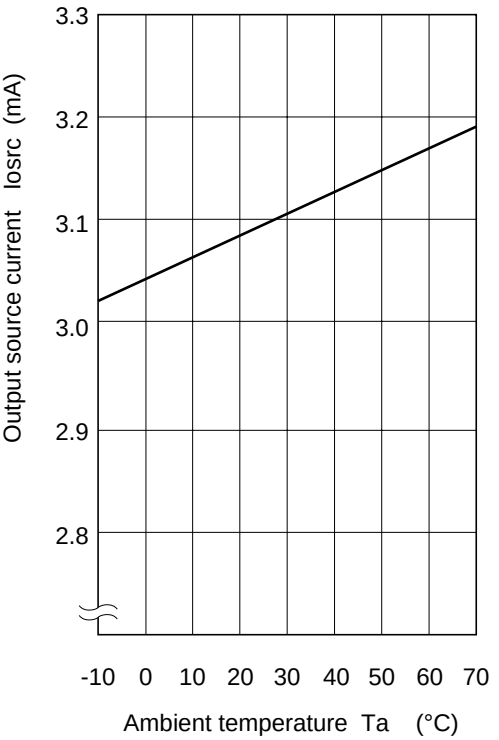




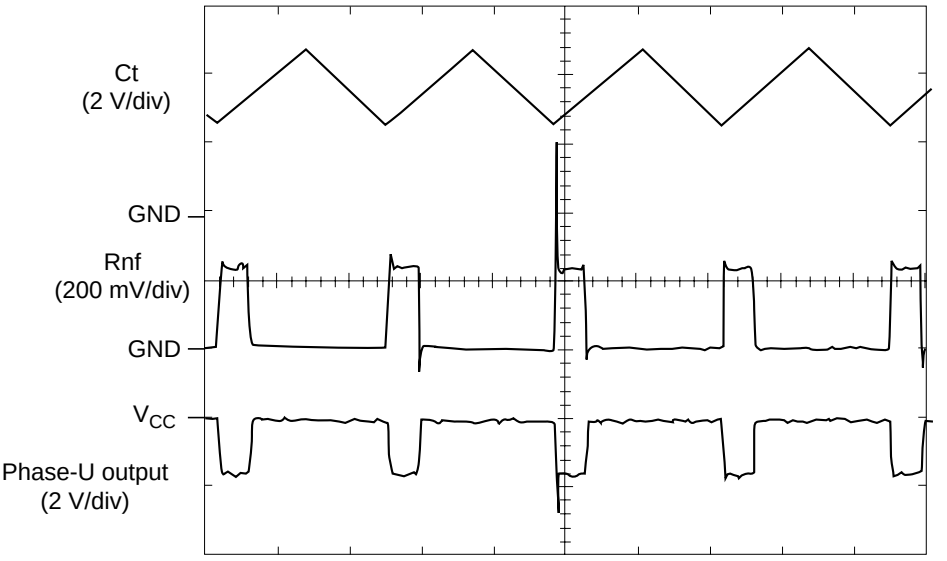


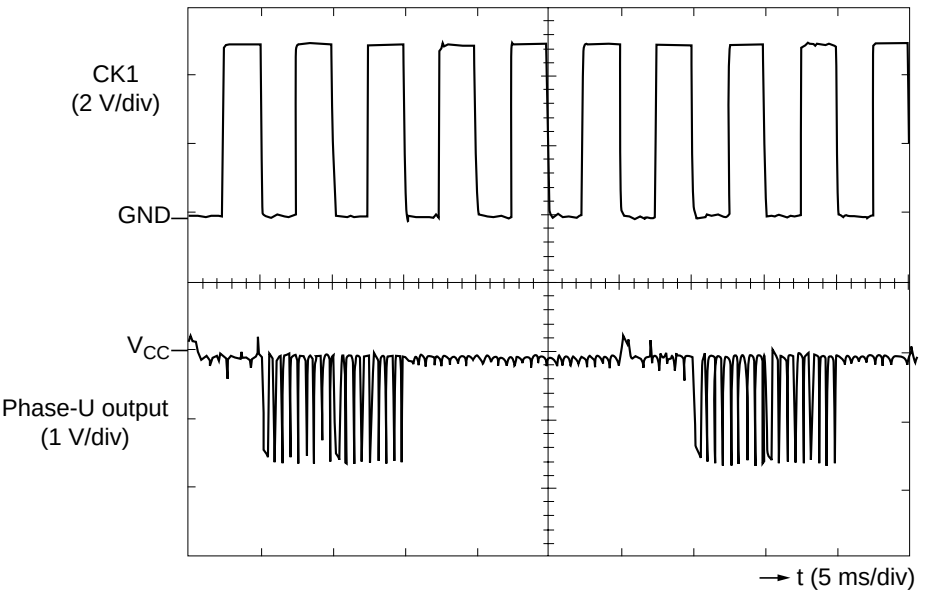
Notes: 1. Iosnk + Iosrc is the current during three-channel output.
2. Iosnk is the current during two-channel output.


Output sink current Iosnk (mA)
3.3
3.2
3.1
3.0
2.9
2.8
-10 0 10 20 30 40 50 60 70
Ambient temperature Ta (°C)


Output source current Iosrc (mA)
3.3
3.2
3.1
3.0
2.9
2.8
-10 0 10 20 30 40 50 60 70
Ambient temperature Ta (°C)

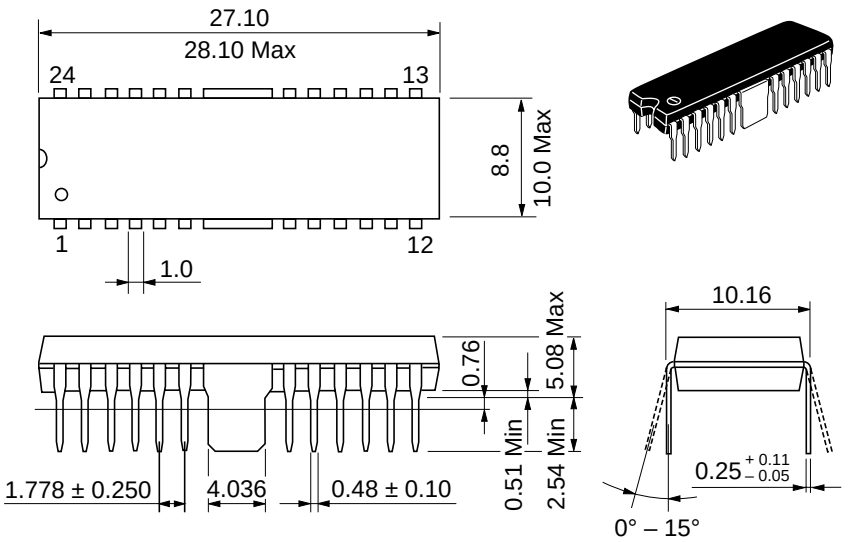
In-Circuit Waweform Characteristics





Package Dimensions

Unit: mm



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