
HA16107P/FP, HA16108P/FP

PWM Switching Regulator for High-performance Voltage Mode Control

HITACHI

ADE-204-012B (Z)

Rev. 2

Dec. 2000

Description

The IC products in this series are primary control switching regulator control IC's appropriate for obtaining stabilized DC voltages from commercial AC power.

These IC's can directly drive power MOS FET's, they have a timer function built in to the secondary overcurrent protection, and they can perform intermittent operation or delayed latched shutdown as protection operations in unusual conditions. They can be used to implement switching power supplies with a high level of safety due to the wide range of built-in functionality.

Functions

- 6.45 V reference voltage
- Triangle wave generator
- Error amplifier
- Under voltage lockout protector
- PWM comparator
- Pulse-by-pulse current limiting
- Timer-latch current limiting (HA16107)
- ON/OFF timer function (HA16108)
- Soft start and quick shutdown
- Output circuit for power MOS FET driving

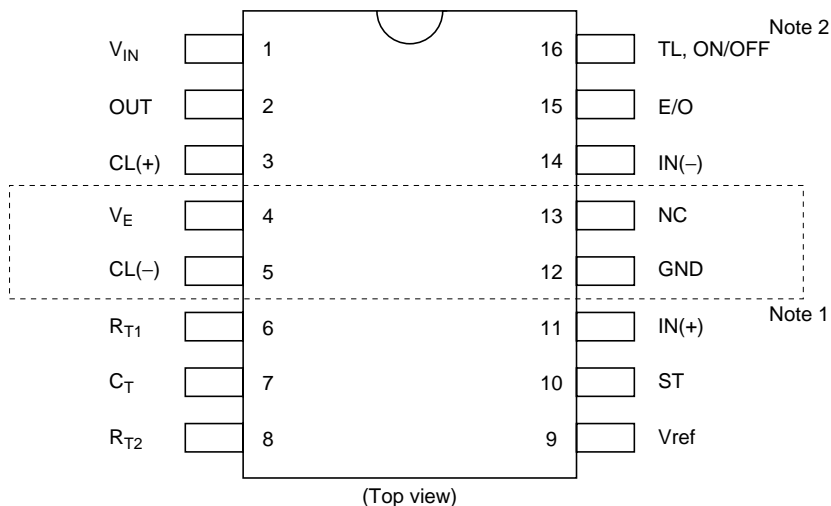
Features

- Operating frequencies up to a high 600 kHz
- Built-in pre-driver circuit for driving power MOS FET
- Built-in timer latch over-current protection function (HA16107)
- The OCL enables intermittent operation by an ON/OFF timer for prevention of secondary overcurrent. (HA16108)
- The UVL function (under voltage lockout) is applied to both V_{in} and V_{ref} .
- ON/OFF reset: an auto-reset function which is based on the time constant of an external capacitor and observation of drops in V_{in} .
- Since the over-voltage protection function OVP (the TL pin) only observes voltage drops in V_{in} , it is possible to use the OVP and ON/OFF pin for independent purposes.
- Built-in 34 V Zener diode between V_{in} and ground.

Ordering Information

Product	Typical Threshold Voltage		Notes	Package
	UVL1	OVP		
HA16107P	Hi: 16.2 V	7.0 V	Timer latch protection	DP-16
HA16107FP	Lo: 9.5 V			FP-16DA
HA16108P	Hi: 16.2 V	Hi: 7.0 V	On-off timer protection (intermittent operation possible)	DP-16
HA16108FP	Lo: 9.5 V	Lo: 1.3 V		FP-16DA

Pin Arrangement



- Notes: 1. In the SOP package models (HA16107FP and HA16108FP) pins 4, 5, and 13 are connected inside the IC. However, all must be connected to the system ground.
 2. Pin 16 is TL (HA16107), ON/OFF (HA16108).

Pin Functions

- HA16107P, HA16108P

Pin No.	Symbol	Pin Functions
1	V_{IN}	Input voltage
2	OUT	Pulse output
3	CL (+)	Current limiter
4	V_E	Output ground
5	CL (-)	Current limiter
6	R_{T1}	Timing resistor (rising time)
7	C_T	Timing capacitor
8	R_{T2}	Timing resistor (falling time)
9	Vref	Reference voltage output
10	ST	Soft start
11	IN (+)	Error amp (+) input
12	GND	Ground
13	NC	NC
14	IN (-)	Error amp (-) input
15	E/O	Error output
16	TL, ON/OFF	Timer latch (HA16107), ON/OFF (HA16108)

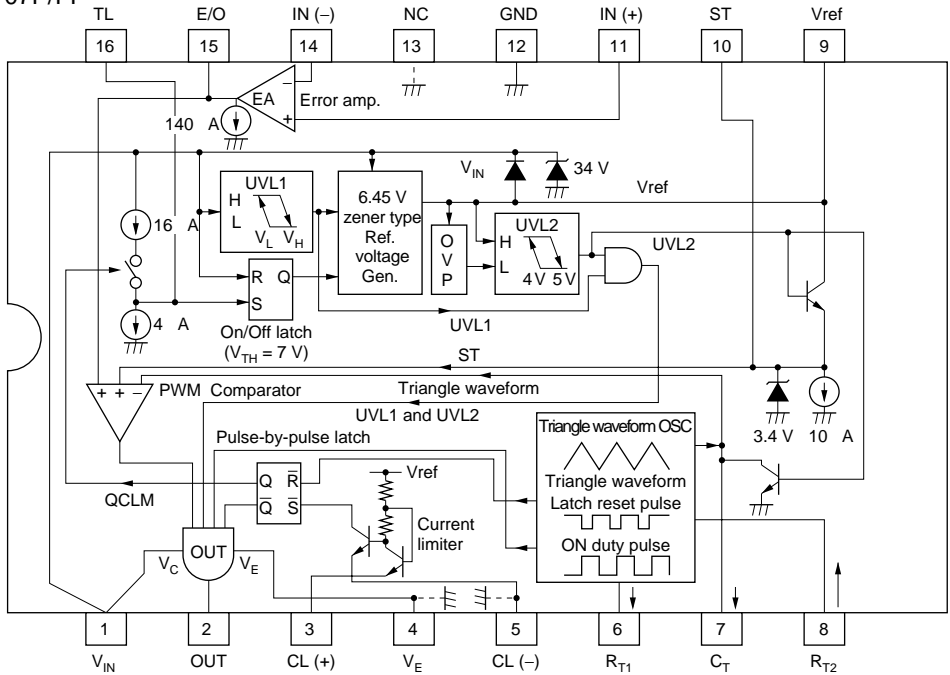
HA16107P/FP, HA16108P/FP

- HA16107FP, HA16108FP

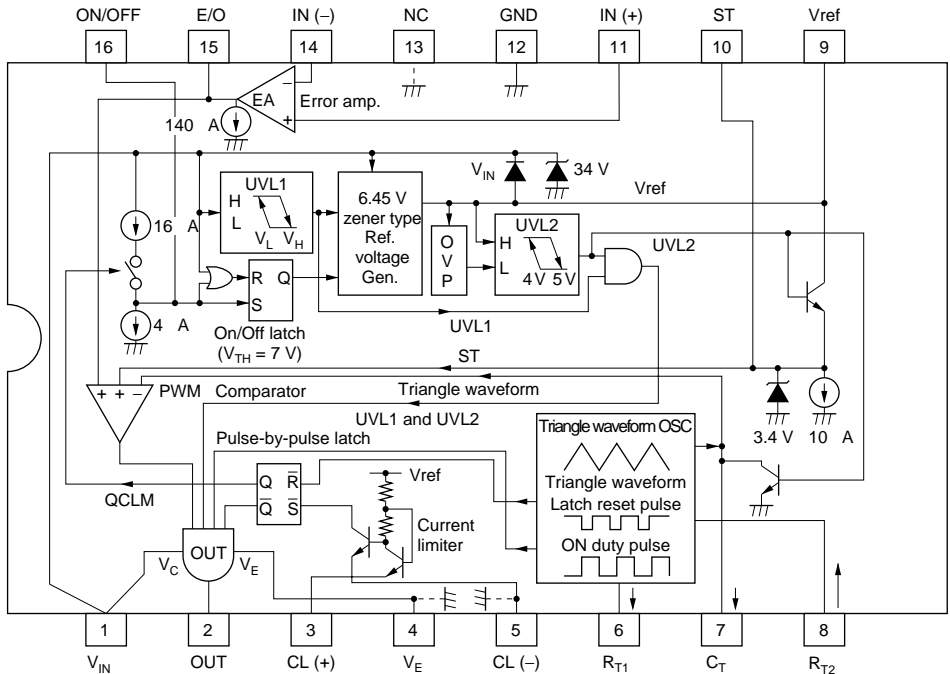
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7	C_T	Timing capacitor
8	R_{T2}	Timing resistor (falling time)
9	Vref	Reference voltage output
10	ST	Soft start
11	IN (+)	Error amp (+) input
12	GND	Ground
13	GND	Ground
14	IN (-)	Error amp (-) input
15	E/O	Error output
16	TL, ON/OFF	Timer latch (HA16107), ON/OFF (HA16108)

Block Diagram

• HA16107P/FP



• HA16108P/FP

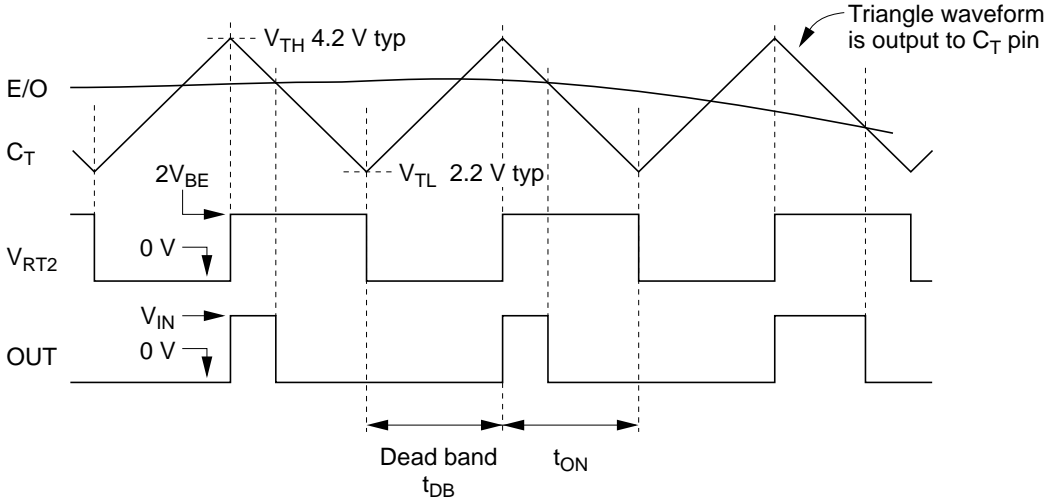


Note: Dotted lines apply to the SOP package model (pins 4, 5, and 13: ground)

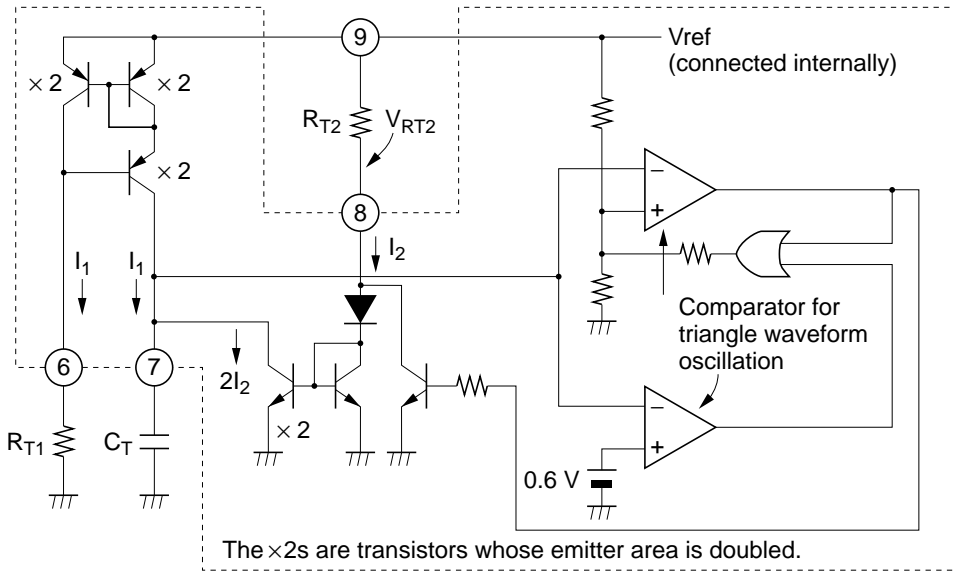
Function and Timing Chart

Triangle Waveform and PWM Output

- Timing chart (during normal operation)



- Oscillator equivalent circuit



$$I_1 = \frac{V_{ref} - 2V_{BE}}{R_{T1}}$$

$$I_2 = \frac{V_{ref} - 2V_{BE}}{R_{T2}}$$

$$t_{DB} = \frac{C_T \times R_{T1} \times 2V}{V_{ref} - 2V_{BE}} \approx 0.4 \times C_T \times R_{T1} \text{ (s)}$$

$$t_{ON} = t_{DB} \frac{R_{T2}}{2R_{T1} - R_{T2}} \text{ (s)}$$

$$D_{u \text{ max}} = \frac{R_{T2}}{2R_{T1}}$$

$$f_{OSC} \approx \frac{1 - D_{u \text{ max}}}{t_{DB}} \text{ (Hz)}$$

Note: When f_{OSC} is high, the actual value will differ from that given by the formula due to the delay time. Determine the correct constants after constructing a test circuit.

1. Timing in Normal Operation

Timing in these ICs is based on a triangular voltage waveform. The rising edge (leading edge) defines the deadband time t_{DB} . The falling edge (trailing edge) defines the ON-duty control band t_{ON} . PWM output is on in the area within t_{ON} that is bounded above by the triangle wave V_{CT} and error output $V_{E/O}$. The following pin outputs are related to PWM control:

- C_T (pin 7): triangle-wave voltage output
- E/O (pin 15): error output voltage
- R_{T2} (pin 8): ON-duty pulse output voltage
- OUT (pin 2): PWM pulse output (for driving the gate of a power MOS FET)

2. Triangle Oscillator, Waveform and Frequency

The triangle oscillator in these ICs generates a triangular waveform by charging and discharging timing capacitor C_T with a constant current, as shown in the equivalent circuit. The C_T charge current is:

$$I(C_{T\text{chg}}) = I_1 = \frac{V_{REF} - 2V_{BE}}{R_{T1}}$$

The discharge current is:

$$I(C_{T\text{dischg}}) = 2I_2 - I_1, \text{ where } I_2 = \frac{V_{REF} - 2V_{BE}}{R_{T2}}$$

In these equations V_{ref} (reference voltage) is typically 6.45 V, and V_{BE} (base-emitter voltage of internal transistors) is about 0.7 V.

The deadband time is:

$$\begin{aligned} t_{DB} &= \frac{C_T \times R_{T1} \times 2V}{V_{REF} - 2V_{BE}} + 0.8 \mu\text{s} \\ &\approx 0.4 \times C_T \times R_{T1} + 0.8 \mu\text{s} \end{aligned}$$

The ON-duty time is:

$$t_{ON} = t_{DB} \times \frac{R_{T2}}{2R_{T1} - R_{T2}}$$

The 0.8 μs in these equations is a correction term for internal circuit delays.

The maximum ON-duty is

$$Du \text{ max} = \frac{R_{T2}}{2R_{T1}}$$

The oscillating frequency is:

$$\begin{aligned} f_{OSC} &= \frac{1}{\frac{t_{DB}}{1 - Du \text{ max}} + 0.8 \mu\text{s}} \\ &= \frac{1}{\frac{0.8 \times C_T \times R_{T1}^2}{2R_{T1} - R_{T2}} + 0.8 \mu\text{s}} \text{ (Hz)} \end{aligned}$$

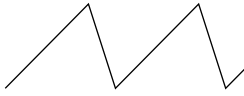
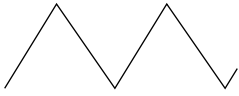

When $R_{T1} = R_{T2}$, the maximum ON-duty is 50%, and:

$$f_{OSC} \approx \frac{1}{0.8 C_T R_{T1} + 0.8 \mu\text{s}} \text{ (Hz)}$$

This approximation is fairly close, but it should be checked in-circuit.

3. Programming of Maximum ON-Duty (Du Max)

The preceding equations should be used to program the deadband or maximum ON-duty. The following table gives a summary.

Condition	$R_{T1} > R_{T2}$	$R_{T1} = R_{T2}$	$R_{T1} < R_{T2}$
Triangle waveform			
Du max	Less than 50%	50%	Greater than 50%*

Note: In a primary-control switching regulator, Du Max > 50% is dangerous because the transformer will saturate.

Soft Start and Quick Shutdown

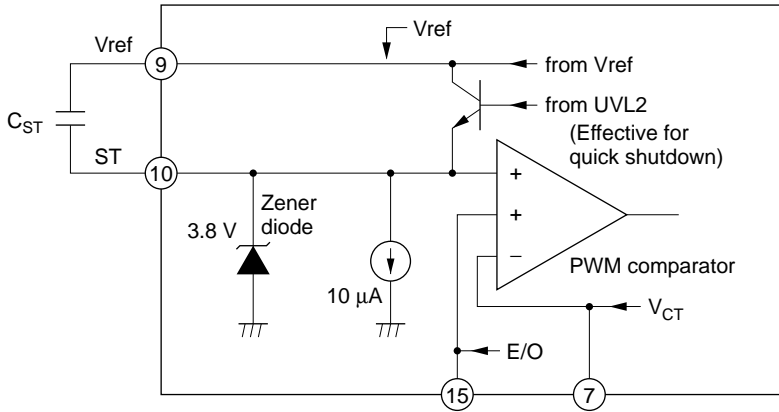
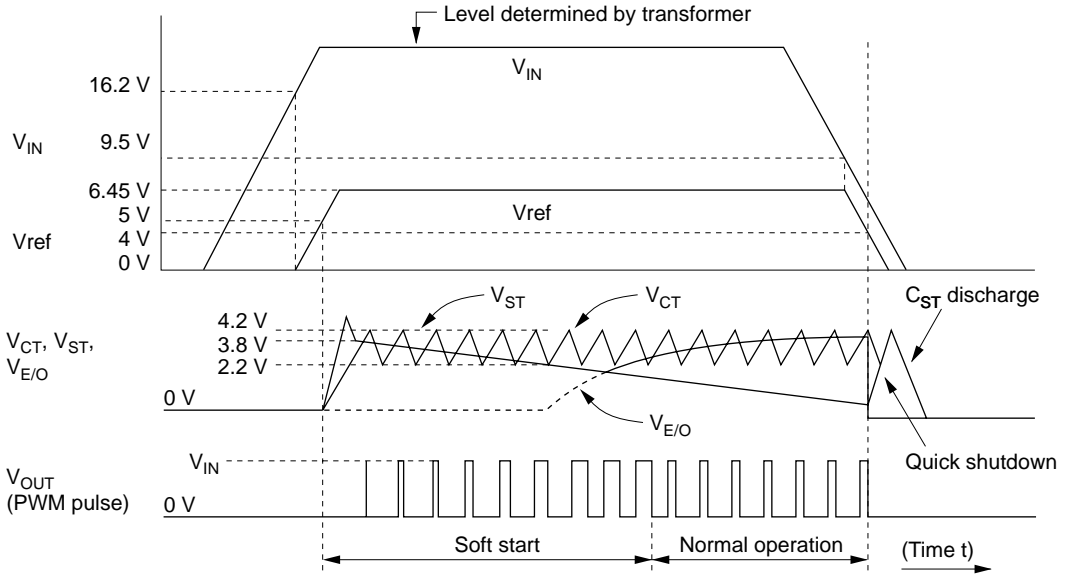
One purpose of the soft-start function is to protect the switching controller and power MOSFET from surges at power-up. Another purpose is to let the secondary-side DC voltage rise smoothly.

When power goes off, the quick-shutdown function rapidly discharges the capacitor in the soft-start circuit (and at the same time switches the PWM output off) to prepare for the next power-on.

The soft-start function in these ICs lets the PWM output develop smoothly from zero to the designated pulse width at power-up. The soft-start voltage is the 3.8 V voltage value of an internal Zener diode, so the PWM output is able to start widening gradually as soon as the soft-start function starts operating. The soft-start function will start promptly even if C_{ST} is large.

The soft-start and quick-shutdown modes are selected automatically in the IC, under control of the UVL signal.

• Timing waveforms

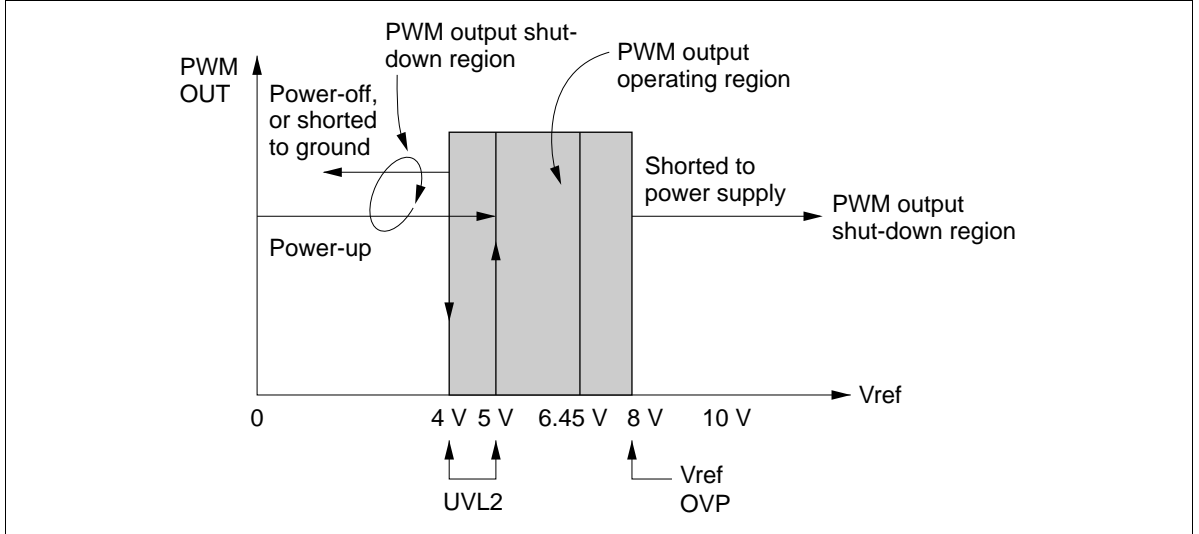


Note: The soft-start time constant is determined by C_{ST} and the constant-current value (typically 10 μ A).

Vref Protection Functions: Overvoltage and Undervoltage

Vref overvoltage and undervoltage conditions are detected by the overvoltage detection circuit and UVL2 circuit. PWM output shuts down when $V_{ref} \geq 8\text{ V}$. UVL2 detects undervoltage with hysteresis between approximately 4 V and 5 V. PWM output also shuts down below these voltages. It follows that PWM output will shut off whenever the Vref pin is shorted to the power supply (V_{IN}) or ground (GND). PWM output also shuts off when V_{IN} is turned on or off.

The following diagram shows how these protection functions operate when power comes on and goes off ($V_{ref} < 6.45\text{ V}$), and when a high external voltage is applied to the Vref pin ($V_{ref} > 6.45\text{ V}$).



1. Current-Limiter Circuit

The current limiter pin (CL) is connected to the emitter of an npn transistor, as shown in the block diagram. The threshold voltage is 240 mV typ. The switching speed of this circuit is approximately 100 ns from detection of overcurrent to shut-down of PWM output. Switching speed increases with the strength of the signal input to the CL pin.

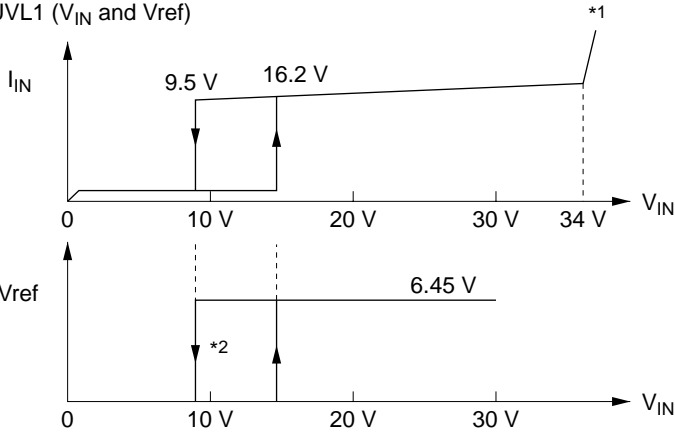
Instead of simple pulse-by-pulse current limiting, in these ICs the current limiting circuit is linked to the timer-and-latch or ON/OFF timer circuit, and also detects the degree of overcurrent. The overcurrent value is determined from the point at which current limiting is triggered in the ON-duty cycle. With a large overcurrent (causing current limiting to operate even at a small ON-duty), the IC automatically shortens the timer time.

Undervoltage Lockout and PWM Output

The undervoltage lockout function turns off the PWM pulse output when the controller's supply voltage goes below a designated value. These ICs have two undervoltage lockout circuits. The UVL1 circuit senses the supply voltage V_{IN} . The UVL2 circuit senses the V_{ref} voltage. A feature of these ICs is that PWM output is turned on only when both voltages are above designated values. Otherwise, the IC operates in standby mode.

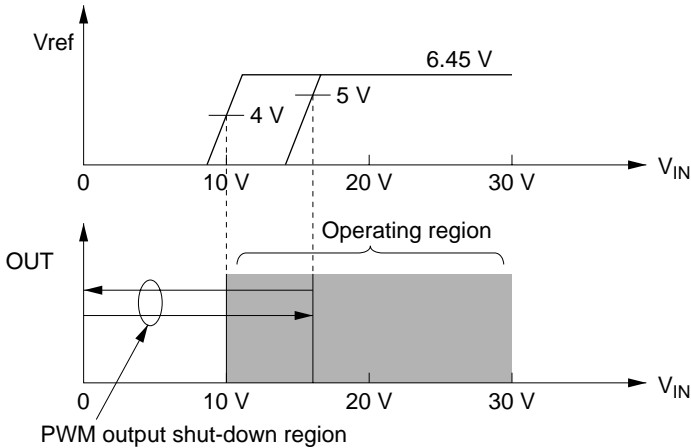
The two built-in undervoltage lockout circuits make it possible to configure an extremely safe power supply system. PWM output will shut down under a variety of abnormal conditions, such as if V_{ref} is shorted to ground while V_{IN} is applied.

• UVL1 (V_{IN} and V_{ref})



- Notes: 1. Breakdown voltage of the internal Zener diode ($V_z = 34\text{ V typ}$).
 2. Hysteresis characteristic.

• UVL2 (V_{ref} and PWM output)



• UVL1 and UVL2

V_{IN} (UVL1)	L	H	H	L
V_{ref} (UVL2)	L	L	H	H
PWM OUT	L	L	OUT	L
Standby mode	⊙	⊙	—	⊙

Note: Double circles indicate standby mode.

Timer Latch and ON/OFF Timer

The HA16107 has a built-in timer-latch function. The HA16108 has a built-in ON/OFF timer function.

The timer-latch function is an overvoltage protection function that combines latched shutdown of PWM output with a timer function to vary the time until latched shutdown occurs according to the overcurrent value. A dedicated voltage detection pin is provided in addition to V_{ref} overvoltage protection.

The ON/OFF timer function is equivalent to the above timer-latch function without the latch. If overcurrent is detected continuously, PWM output shuts down temporarily, then normal operation resumes. This process repeats, temporary shutdown alternating with normal operation.

Both the timer-latch function in the HA16107 and the ON/OFF function in the HA16108 wait for an interval after overcurrent detection before shutting down PWM output. The interval is determined by capacitor C_{TM} and the value of the charge/discharge current supplied internally from the IC. Normal operation therefore continues if a single overcurrent spike is detected, while if continuous overcurrent is detected, the current and voltage droop curves for the secondary-side output have sharp characteristics.

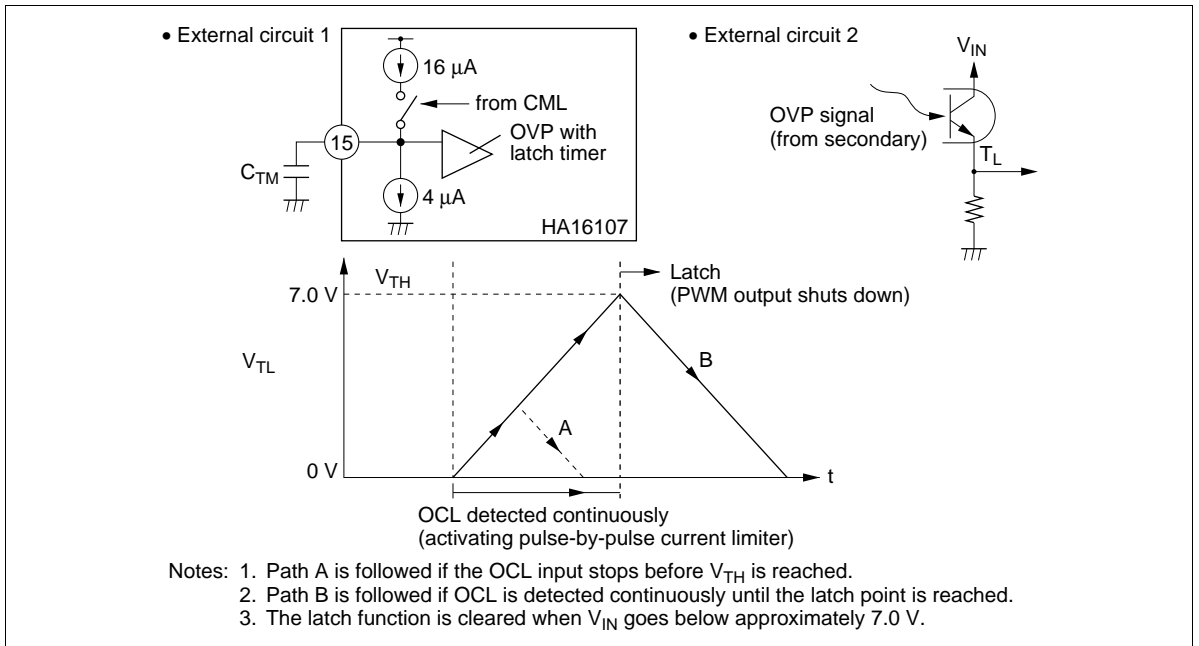
1. Use of Timer-Latch Pin (HA16107)

• Timer-Latch Usage

See external circuit 1 in the following diagram. Under continuous overcurrent, the CML switch turns on, charging C_{TM} with $12\ \mu\text{A}$. PWM output shuts down when the voltage at pin 15 exceeds $7\ \text{V}$.

• Overvoltage Protection Usage

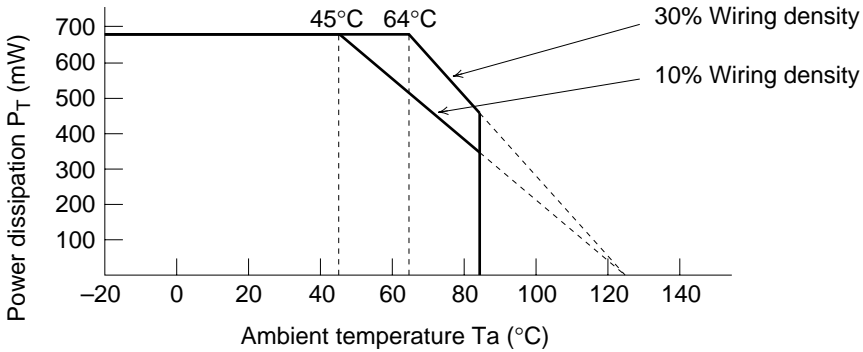
See external circuit 2 in the diagram. This configuration is suitable when overvoltage is detected by an OVP signal received through an optocoupler from the DC output on the secondary side of an AC/DC converter. PWM output shuts down when the OVP signal allows the voltage at the TL pin to exceed $7\ \text{V}$. The shutdown is latched. V_{IN} must go below approximately $6.5\ \text{V}$ (V_{INR2}) to release the latched state.



Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Rating Value	Units	Notes
Supply voltage	V _{IN}	30	V	
Output current (DC)	I _O	±0.2	A	
Output current (peak)	I _{opeak}	±2	A	
Current limiter voltage	V _{CL}	+4, -1	V	
Error amp input voltage	V _{IEA}	V _{ref}	V	
E/O output voltage	V _{IE/O}	V _{ref}	V	
R _{T1} pin current	I _{RT1}	500	μA	
R _{T2} pin current	I _{RT2}	5	mA	
Power dissipation	P _T	680	mW	1, 2
Operating temperature range	Topr	-20 to +85	°C	
Storage temperature range	Tstg	-55 to +125	°C	

- Notes:
1. For the "FP" products (SOP package), this value is when mounted on a 40 by 40 by 1.6 mm glass epoxy substrate. However, this value must be derated by 8.3 mW/°C from Ta = 45°C. When the wiring density is 10%, and 11.1 mW/°C from Ta = 64°C when the wiring density is 30%.
 2. For the "P" products (DIP package), this value is valid up to 45°C, and must be derated by 8.3 mW/°C above 45°C.
 3. In the case of SOP, use center 4 pins, (4), (5), (12), (13) for solder-mounting and connect the wide ground pattern, because these pins are available for heat sink of this IC.



Electrical Characteristics ($T_a = 25^\circ\text{C}$, $V_{IN} = 18\text{ V}$, $f_{OSC} = 100\text{ kHz}$)

Section	Item	Symbol	Min	Typ	Max	Unit	Test Conditions	Note
Reference voltage	Output voltage	Vref	6.10	6.45	6.80	V		
	Line regulation	Line	—	30	60	mV	$12\text{ V} \leq V_{IN} \leq 30\text{ V}$	
	Load regulation	Load	—	30	60	mV	$0\text{ mA} \leq I_o \leq 10\text{ mA}$	
	Temperature stability	$\Delta V_{ref}/\Delta T_a$	—	40	—	ppm/ °C		
	Short circuit current	I_{OS}	30	50	—	mA	Vref = 0 V	
	Over voltage protection (Vref OVP voltage)	Vrovpp	7.4	8.0	9.0	V		
Triangle wave generator	Maximum frequency	fmax	600	—	—	kHz		
	Minimum frequency	fmin	—	—	1	kHz		
	Voltage stability	$\Delta f/f_{o_1}$	—	± 1	± 3	%	$12\text{ V} \leq V_{IN} \leq 30\text{ V}$ $f_{o_1} = (f_{max} + f_{min})/2$	
	Temperature stability	$\Delta f/f_{o_2}$	—	± 1	—	%	$-20^\circ\text{C} \leq T_a \leq +85^\circ\text{C}$ $f_{o_2} = (f_{max} + f_{min})/2$	
	Frequency accuracy	f_{OSC}	270	300	330	kHz	$R_{T1} = R_{T2} = 27\text{ k}\Omega$ $C_T = 120\text{ pF}$	
PWM comparator	Minimum deadband pulse width	t_{DB}	—	—	1.0	μs		
	Low level threshold voltage	V_{TL}	1.9	2.2	2.5	V		
	High level threshold	V_{TH}	3.8	4.2	4.6	V		
	Differential threshold	ΔV_{TH}	1.7	2.0	2.3	V		
	Deadband width initial accuracy	$\Delta DB1$	—	± 1	± 3	%	$R_{T1} = R_{T2} = 27\text{ k}\Omega$ $C_T = 470\text{ pF}$	
	Deadband width voltage stability	$\Delta DB2$	—	± 0.2	± 2.0	%	$12\text{ V} \leq V_{IN} \leq 30\text{ V}$ $(D_{max} - D_{min})/2$	
	Deadband width temperature stability	$\Delta DB3$	—	± 1	—	%	$-20^\circ\text{C} \leq T_a \leq +85^\circ\text{C}$ $(D_{max} - D_{min})/2$	
Error amp	Input offset voltage	V_{IO}	—	2	10	mV		
	Input bias current	I_{IB}	—	0.8	2.0	μA		
	Input sink current	I_{osink}	80	140	—	μA	$V_o = 2\text{ V}$	
	Output source current	$I_{osource}$	80	140	—	μA	$V_o = 5\text{ V}$	

HA16107P/FP, HA16108P/FP

Electrical Characteristics (Ta = 25°C, V_{IN} = 18 V, f_{OSC} = 100 kHz) (cont.)

Section	Item	Symbol	Min	Typ	Max	Unit	Test Conditions	Note
Error amp (cont.)	High level output voltage	V _{OH}	V _{ref} – 1.5	—	—	V	I _O = 10 μA	
	Low level output voltage	V _{OL}	—	—	0.5	V	I _O = 10 μA	
	Voltage gain	G _V	—	55	—	dB	f = 10 kHz	
	Band width	BW	—	15	—	MHz		
	(–) Common mode voltage	V _{CM–}	1.2	—	—	V		
	(+) Common mode voltage	V _{CM+}	—	—	V _{ref} – 1.5	V		
Over-current detector	(+) Threshold voltage	V _{TH+}	0.216	0.240	0.264	V		
	(+) Bias current	I _{B+}	—	180	250	μA	V _{CL+} = 0 V	
	(–) Threshold voltage	V _{TH–}	–0.264	–0.240	–0.216	V		1, 2
	(–) Bias current	I _{B–}	—	950	1350	μA	V _{CL} = –0.3 V	1, 2
	Response time	t _{off}	—	100	—	ns	CL; open V _{CL} = +0.35 V	
Soft start	High level voltage	V _{STH}	3.2	3.8	4.4	V	I _{sink} = 1 mA	
	Sink current	I _{sink}	7	10	13	μA	V _{ST} = 2.0 V	
Under voltage lockout 1	V _{IN} high level threshold voltage	V _{INTH}	14.7	16.2	17.7	V		
	V _{IN} low level threshold voltage	V _{INTL}	8.5	9.5	10.5	V		
	Threshold differential voltage	ΔV _{TH}	5.2	6.2	7.2	V	(V _{INTH} – V _{INTL})	
Under voltage lockout 2	V _{ref} high level threshold voltage	V _{rTH}	4.5	5.0	5.5	V		
	V _{ref} low level threshold voltage	V _{rTL}	3.5	4.0	4.5	V		

- Notes: 1. Only applies to the HA16107P, HA16108P
 2. The terminal should not be applied under –1.0 V.

Electrical Characteristics ($T_a = 25^\circ\text{C}$, $V_{IN} = 18\text{ V}$, $f_{OSC} = 100\text{ kHz}$) (cont.)

Section	Item	Symbol	Min	Typ	Max	Unit	Test Conditions	Note
Timer latch, ON/OFF timer*2	Latch threshold voltage	V_{THH}	6.5	7.0	7.5	V		
	V_{IN} reset voltage	V_{INR2}	6.0	6.5	7.0	V		
	Reset voltage	V_{THL2}	1.0	1.3	1.6	V		1
	Differential threshold to UVL low voltage	ΔV	2.0	3.0	—	V	$(V_{INTL} - V_{INR2})$	
	Source current (OCL mode)	I_{source}	8	12	16	μA	Over current detection mode	
	Sink current (latch mode)	I_{sink}	2.5	4	5.5	μA	TL(ON/OFF) terminal = 4 V	
Output	Low voltage	V_{OL1}	—	1.7	2.2	V	$I_{osink} = 0.2\text{ A}$	
	High voltage	V_{OH}	$V_{IN} - 2.2$	—	—	V	$I_{osource} = 0.2\text{ A}$	
	Low voltage (standby mode)	V_{OL2}	—	—	0.5	V	$I_{osink} = 1\text{ mA}$	
	Rising time	t_r	—	40	—	ns	$C_L = 1000\text{ pF}$	
	Falling time	t_f	—	60	—	ns	$C_L = 1000\text{ pF}$	
Total	Standby current	I_{st}	—	160	250	μA	$V_{IN} = 14\text{ V}$	
	Operation current	I_{IN1}	—	16	20	mA	$V_{IN} = 30\text{ V}$, $C_L = 1000\text{ pF}$, $f = 100\text{ kHz}$	
	Operation current	I_{IN2}	—	12	16	mA	$V_{IN} = 30\text{ V}$, $f = 100\text{ kHz}$, Output open	
	ON/OFF latch current	I_{IN3}	—	350	460	μA	$V_{IN} = 14\text{ V}$	
	$V_{IN} - \text{GND}$ Zener voltage	V_Z	30	34	—	V		

Notes: 1. Only applies to the HA16108P/FP.

2. Timer latch: HA16107P/FP.

ON/OFF timer: HA16108P/FP.

Note on Standby Current

In the test circuit shown in figure 1, the operating current at the start of PWM pulse output is the standby current.

If the resistance connected externally to the Vref pin (including R_{T2}) is smaller than that of the test circuit, the apparent standby current will increase.

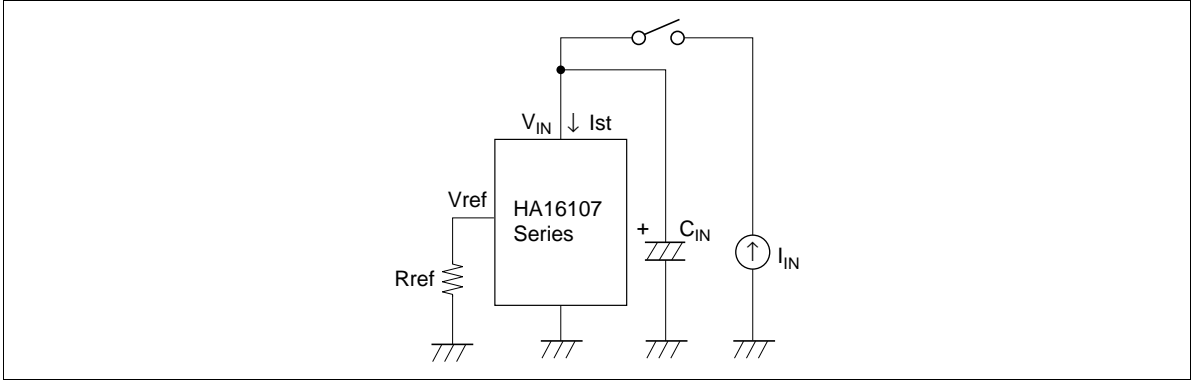


Figure 1 Standby Current Test Circuit

Application Note

- Case:

When DC power is applied directly as the power supply of the HA16107/HA16108, without using the transformer backup coil.

- Phenomenon:

The IC may not be activated in the case of a circuit in which V_{IN} rises quickly (10 V/100 μ s or faster), such as that shown in figure 2.

- Reason:

Because of the IC circuit configuration, the timer latch block operates first.

- Remedy (counter measure):

Take remedial action such as configuring a time constant circuit as shown in figure 3, to keep the V_{IN} rise speed below 10 V/100 μ s.

If the IC power supply consists of an activation resistance and backup coil, as in an AC/DC converter, The V_{IN} rise speed is usually around 1 V/100 μ s, and there is no risk of this phenomenon occurring.

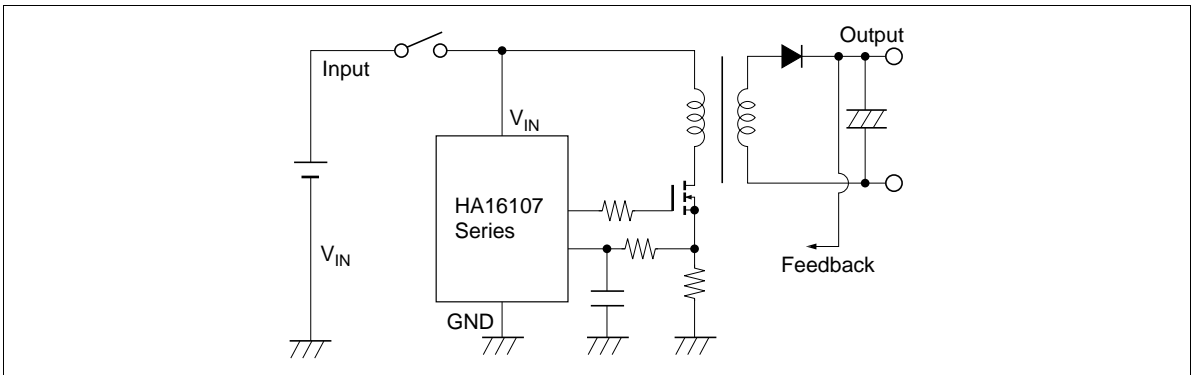


Figure 2 Example of Circuit with Fast V_{IN} Rise Time

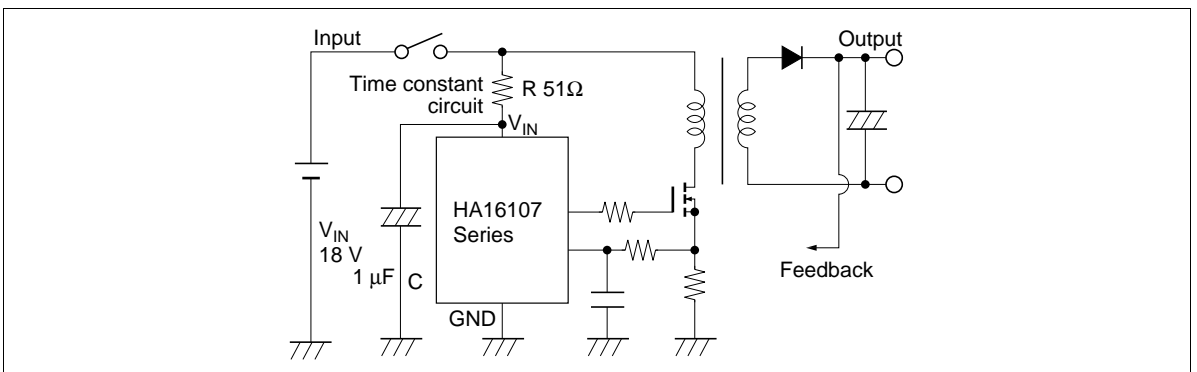
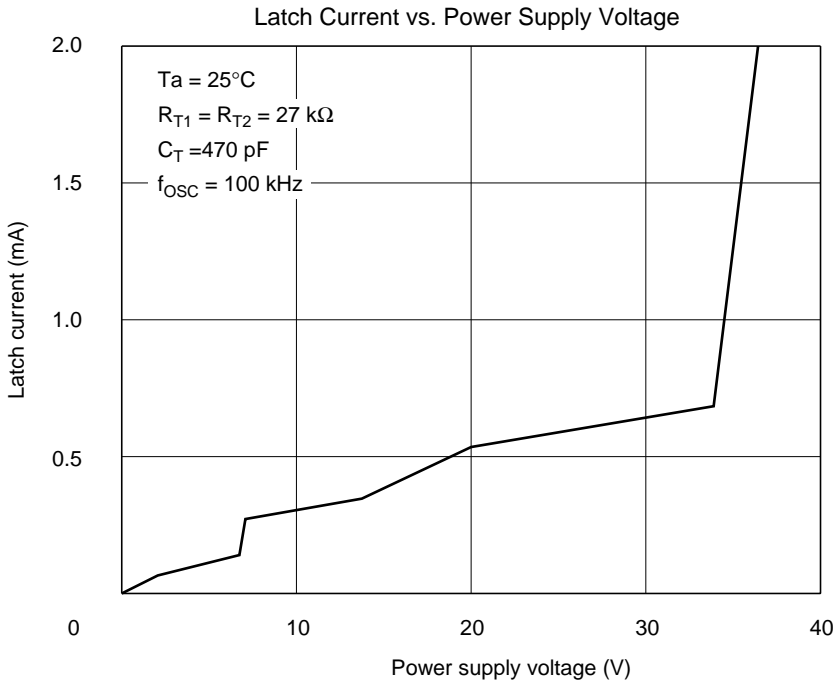
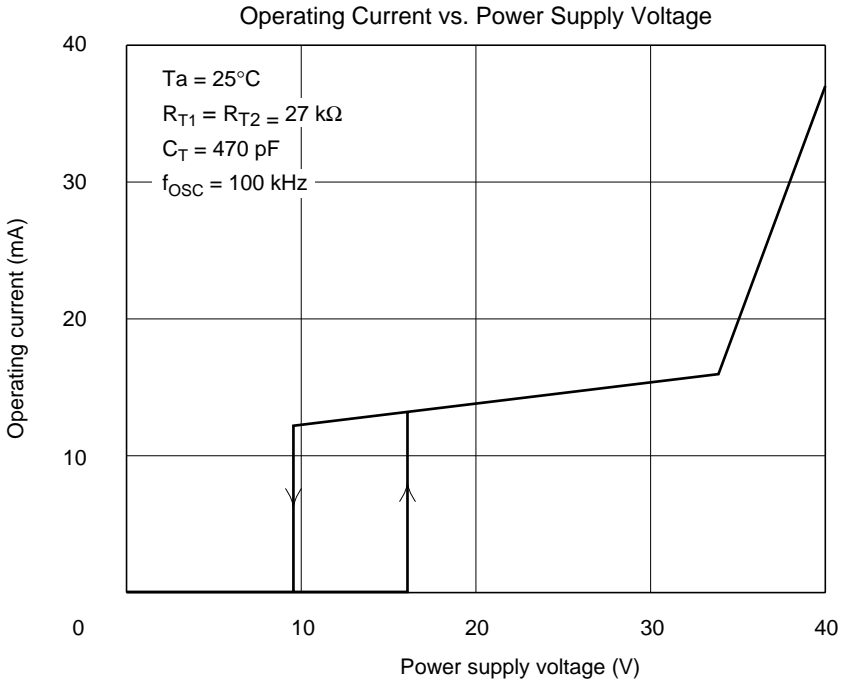
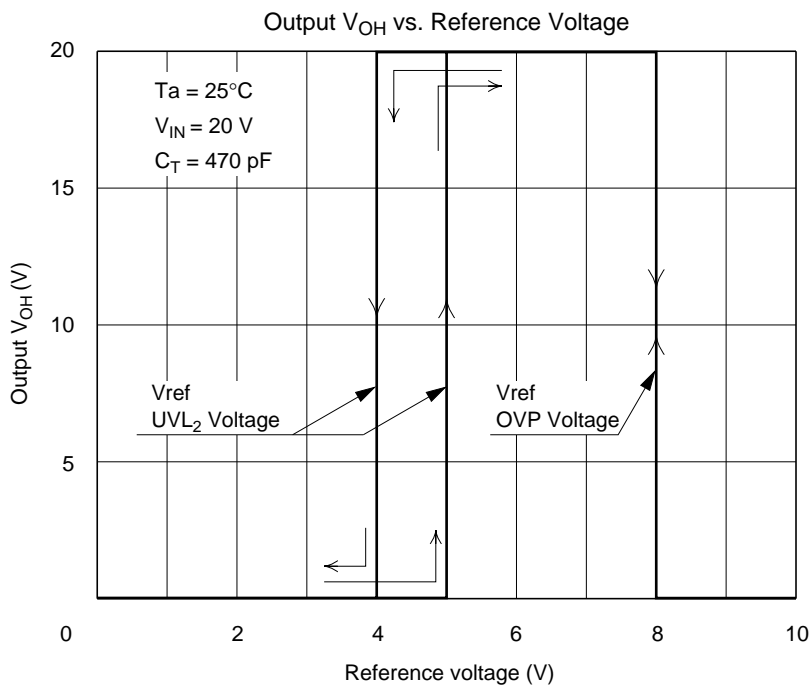
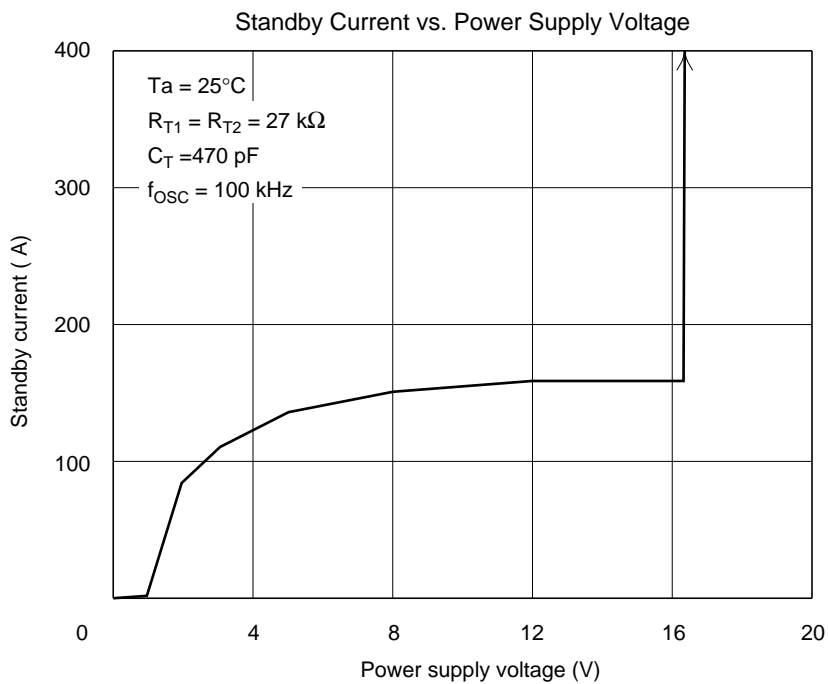
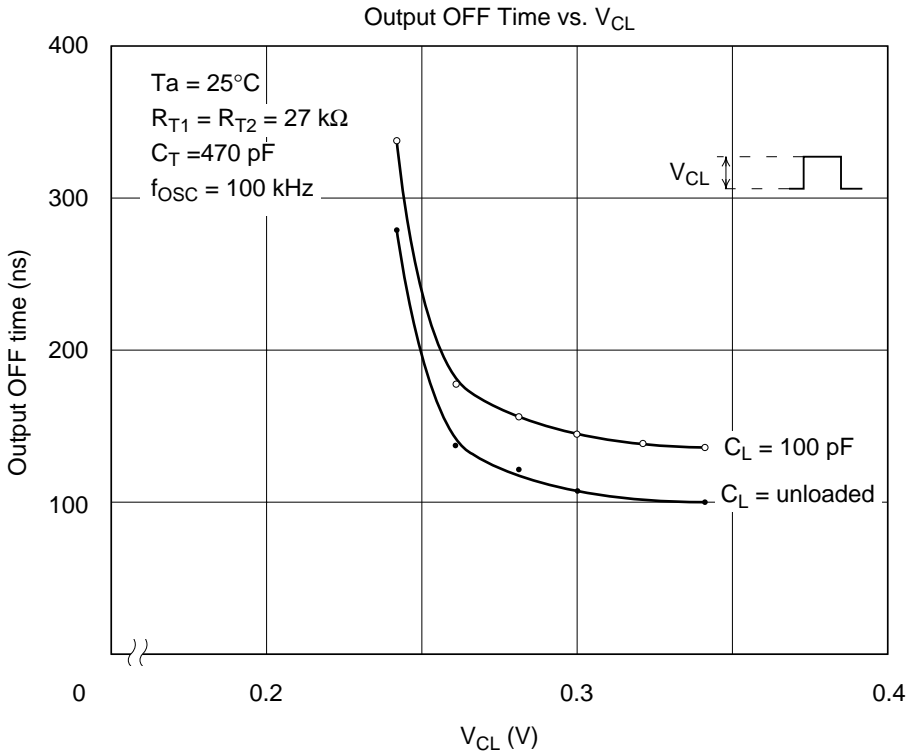
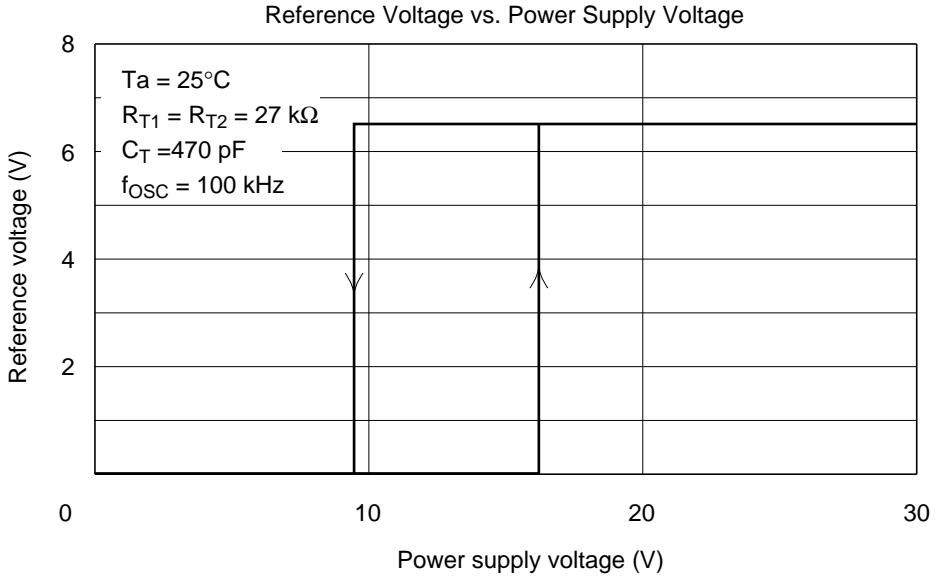


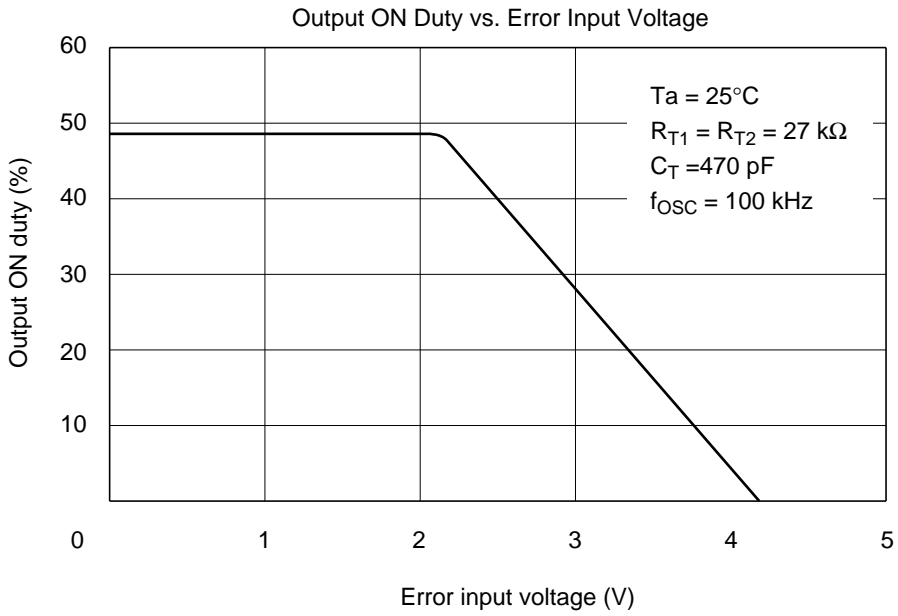
Figure 3 Sample Remedial Circuit

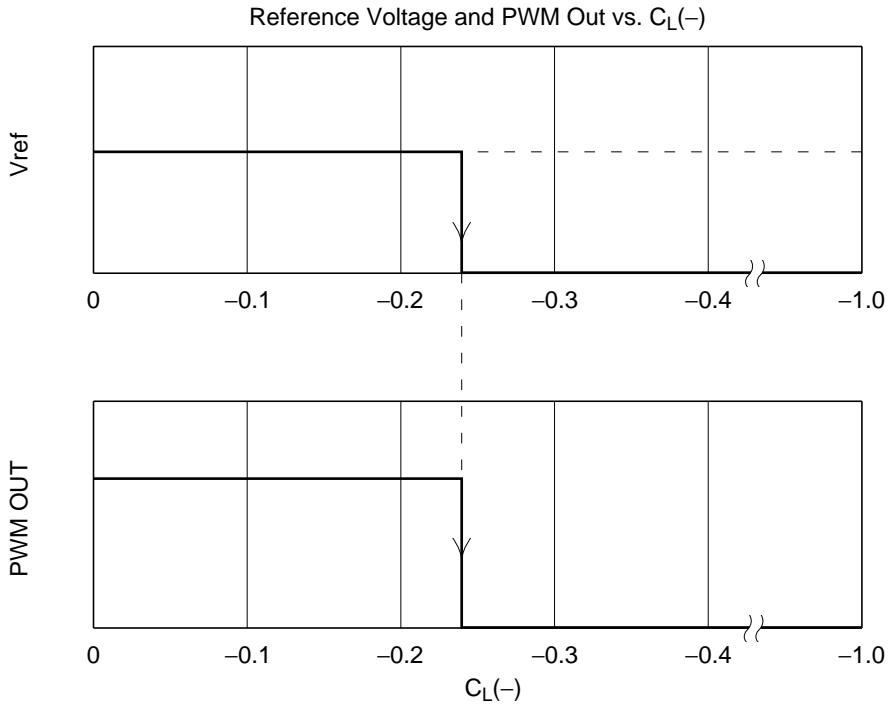
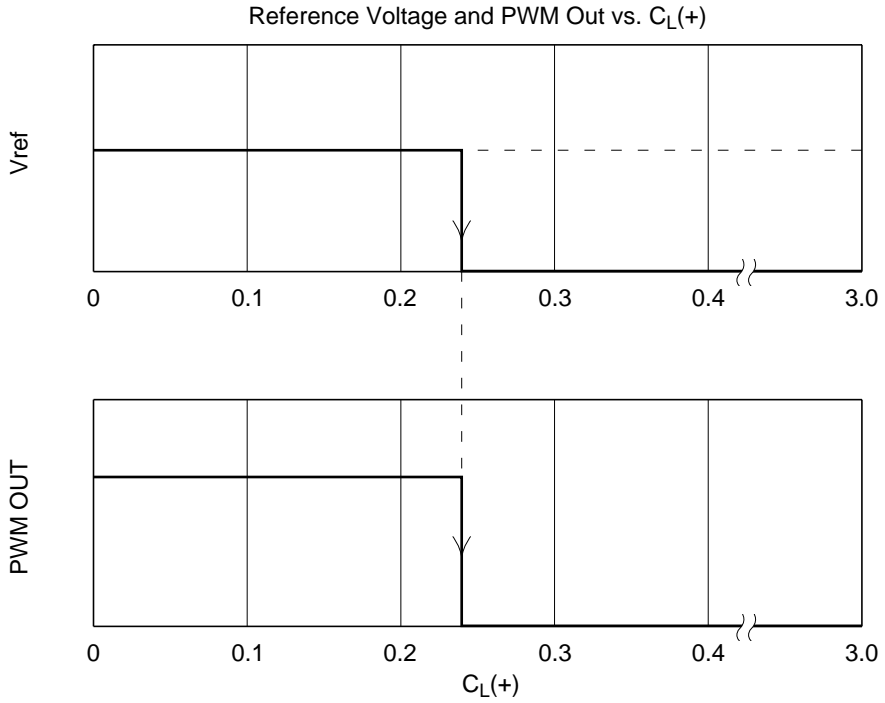
Characteristic Curves

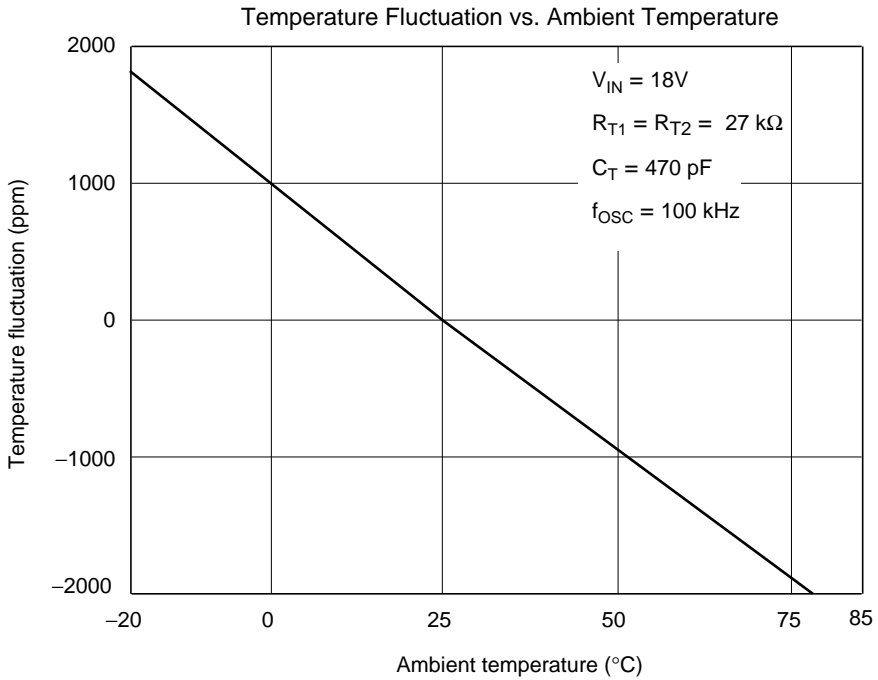
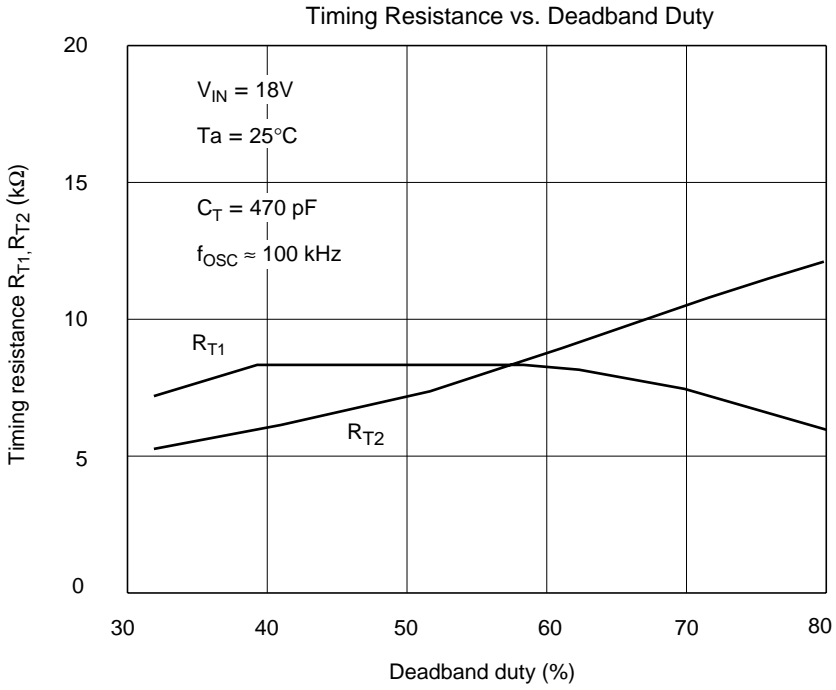


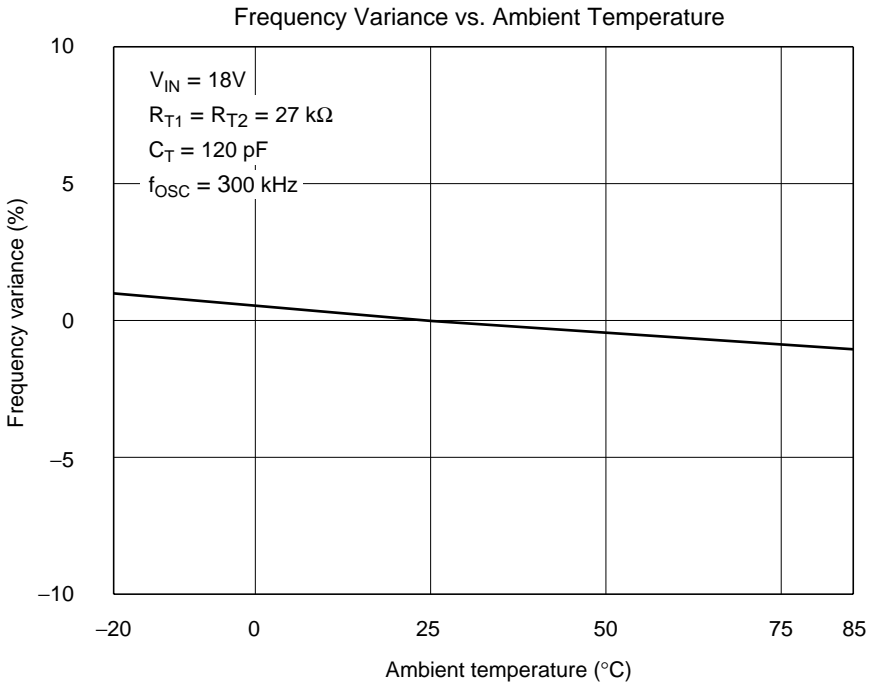
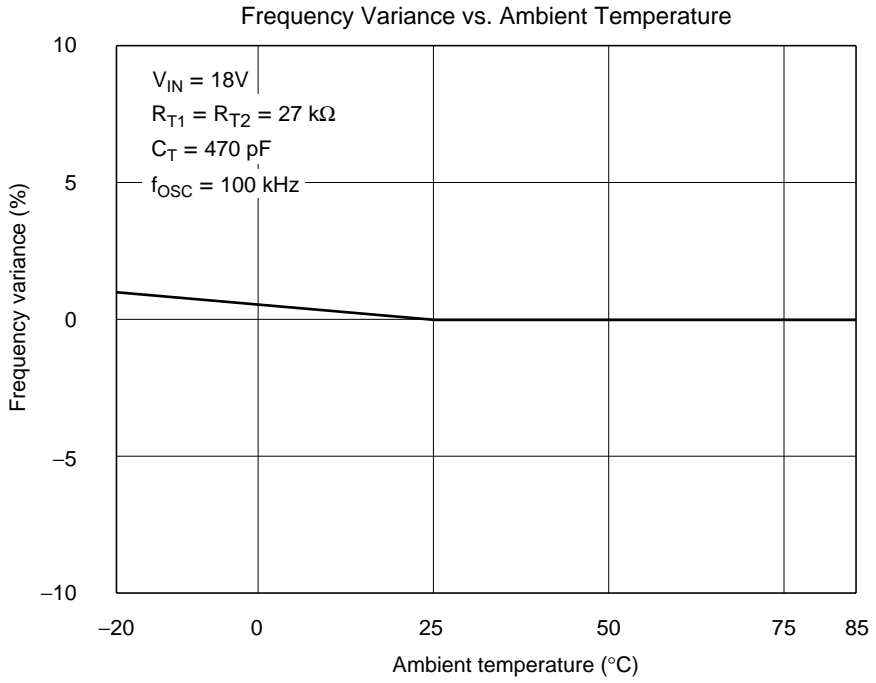




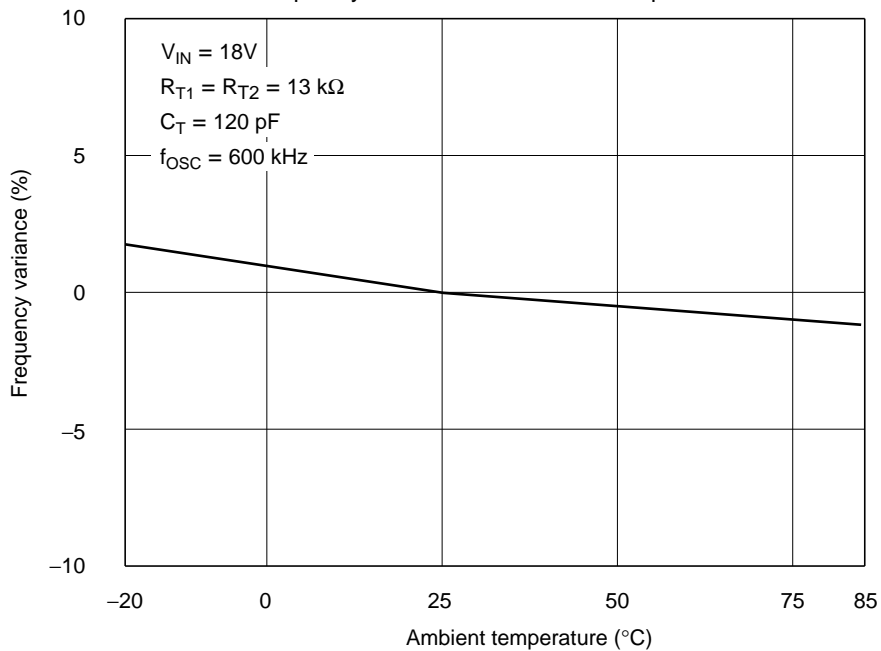




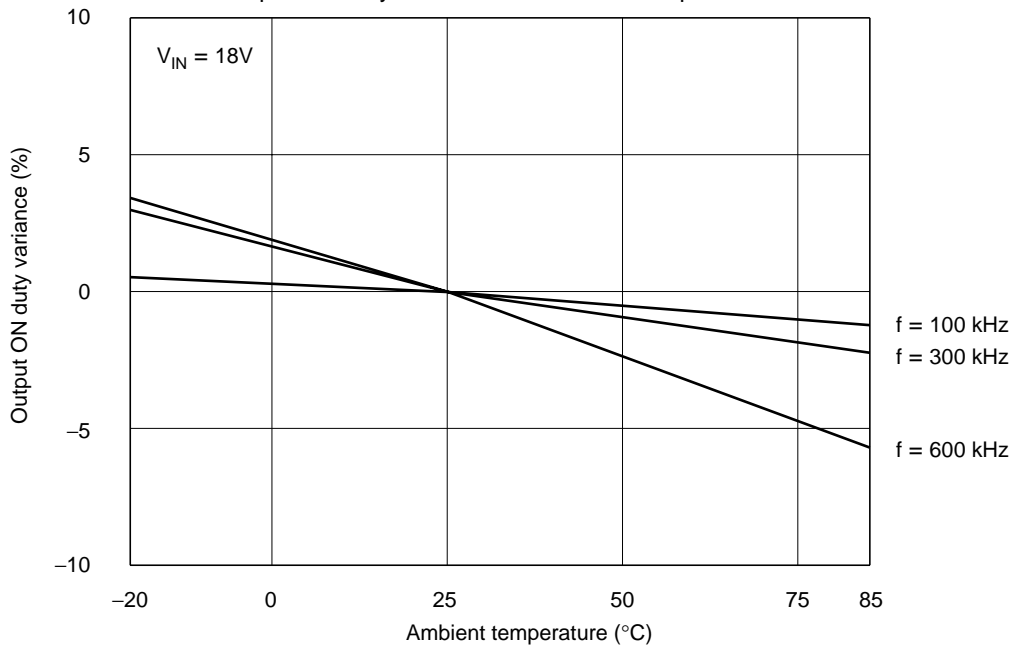


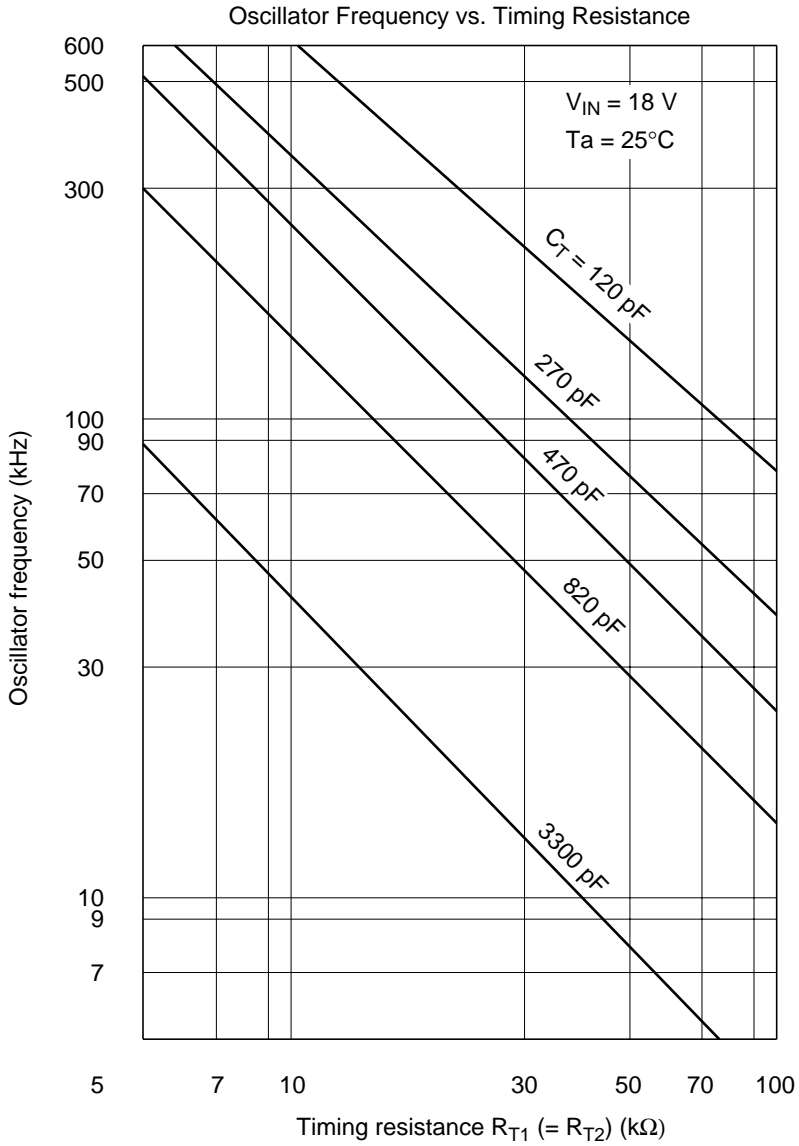


Frequency Variance vs. Ambient Temperature

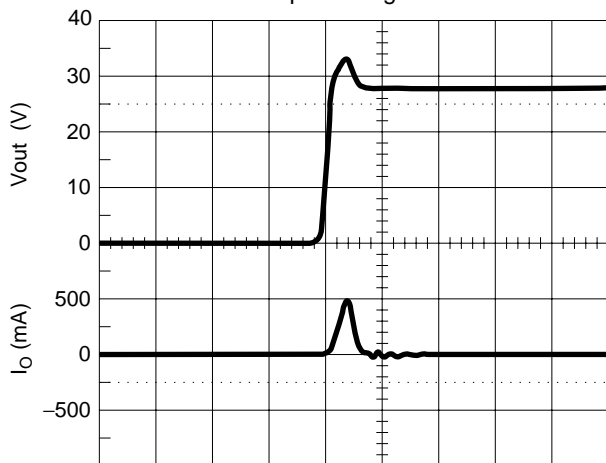


Output ON Duty Variance vs. Ambient Temperature





Vout Output Rising Waveform



→ 200 ns/div

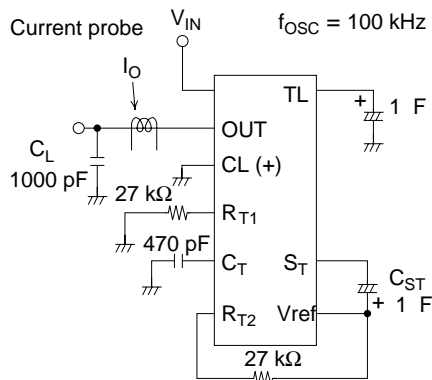
Test circuit

Ta = 25°C

$R_{T1} = R_{T2} = 27\text{ k}\Omega$

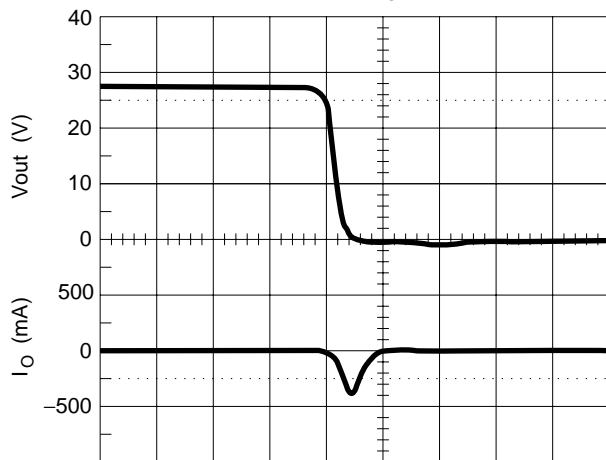
$C_T = 470\text{ pF}$

$f_{OSC} = 100\text{ kHz}$



* Current probe: Tektronix AM503

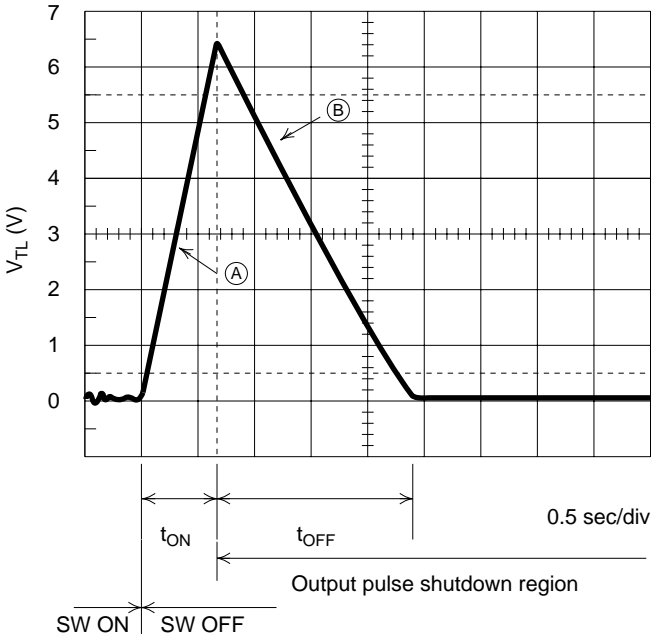
Vout Output Falling Waveform



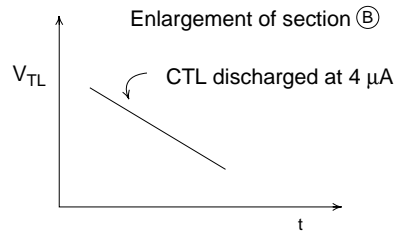
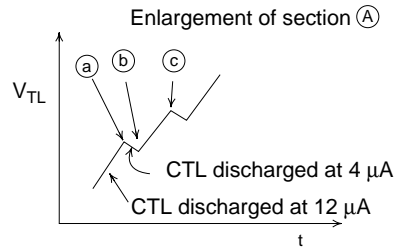
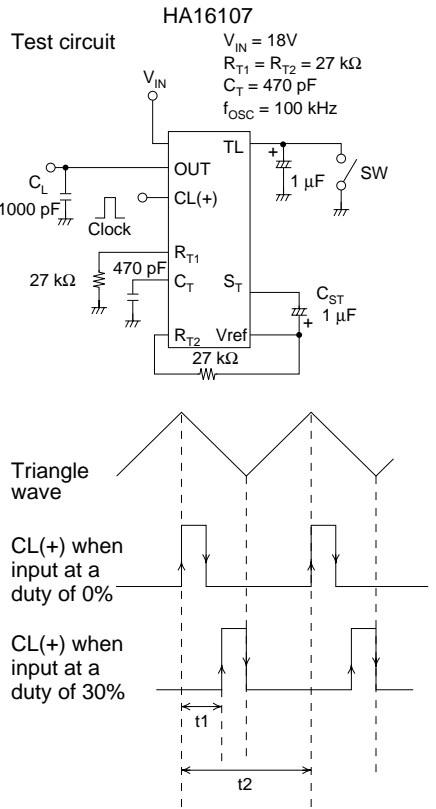
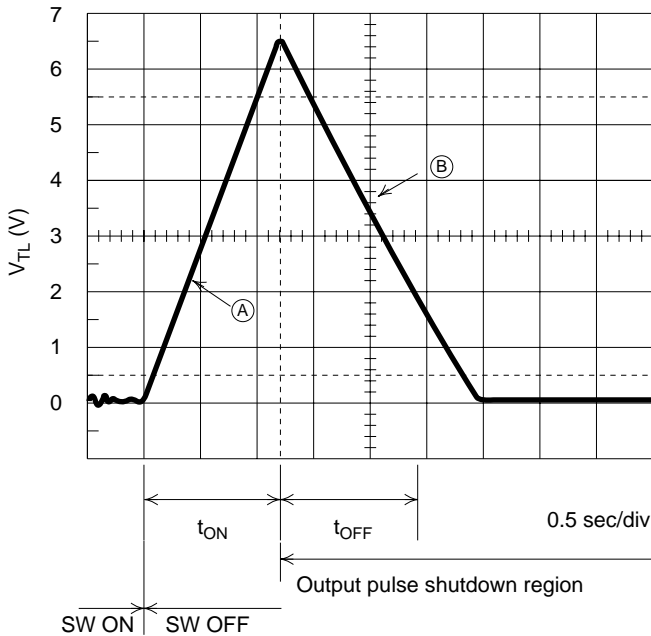
→ 200 ns/div

Operating waveform at the TL pin

When overcurrent is input at the point where the duty cycle is 0%.



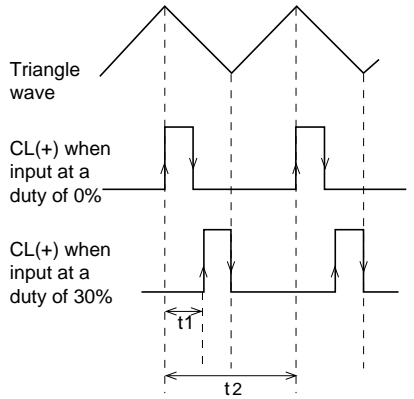
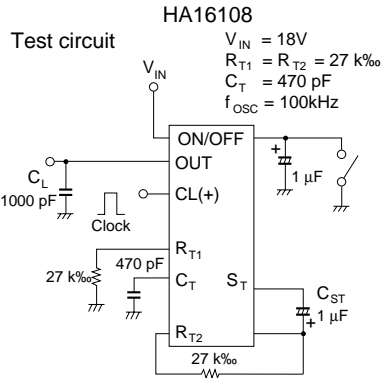
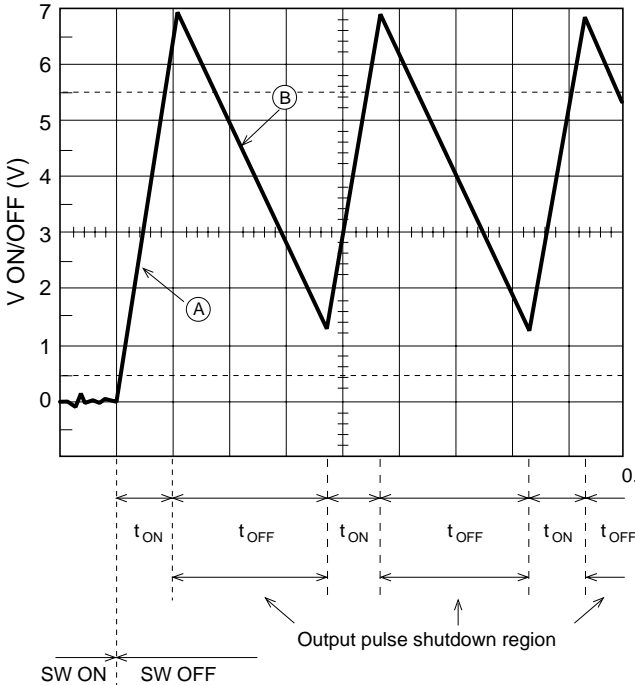
When overcurrent is input at the point where the duty cycle is 30%.



- ① a to ② b : PWM pulse output is High
- ② b : The point where overcurrent is detected
- ② b to ③ c : PWM pulse output is Low.

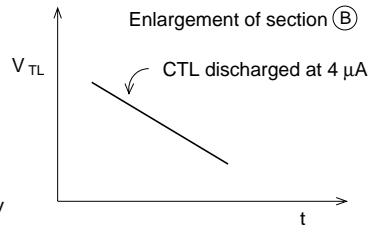
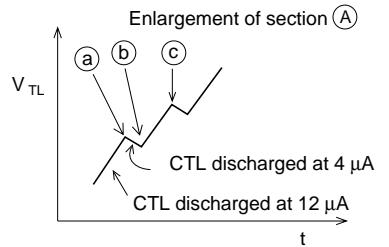
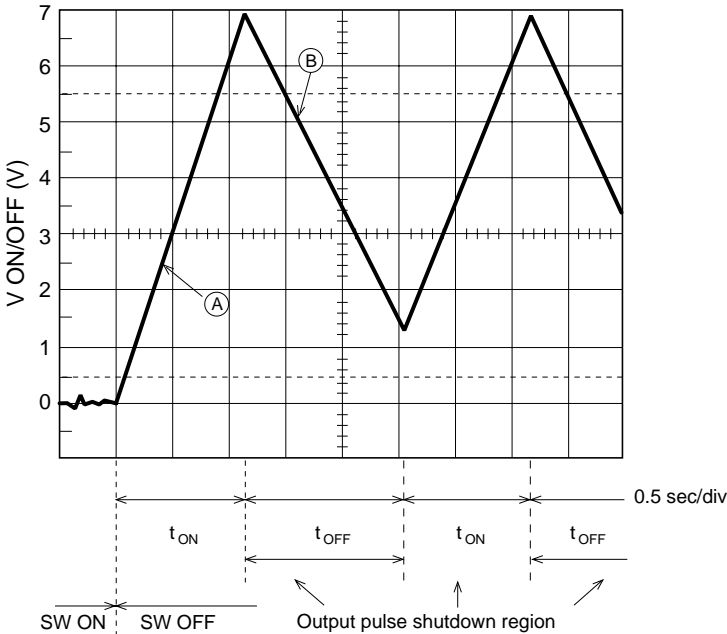
Operating waveform at the ON/OFF pin

When overcurrent is input at the point where the duty cycle is 0%.



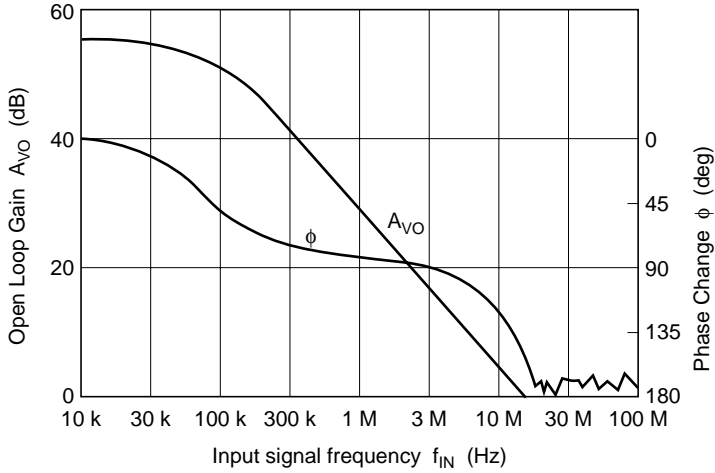
$$Du = \frac{t_1}{t_2} \times 100 (\%)$$

When overcurrent is input at the point where the duty cycle is 30%.

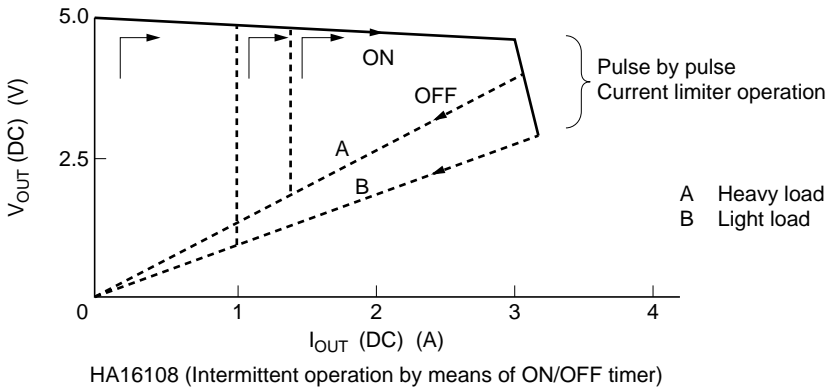
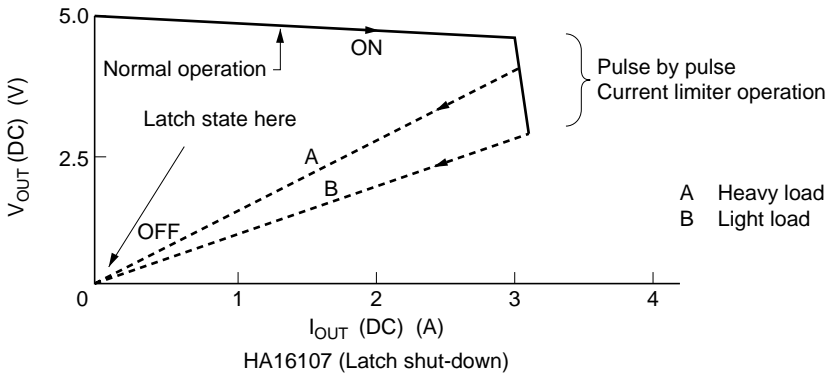


- (a) to (b) : PWM pulse output is High.
- (b) : The point where overcurrent is detected.
- (b) to (c) : PWM pulse output is Low.

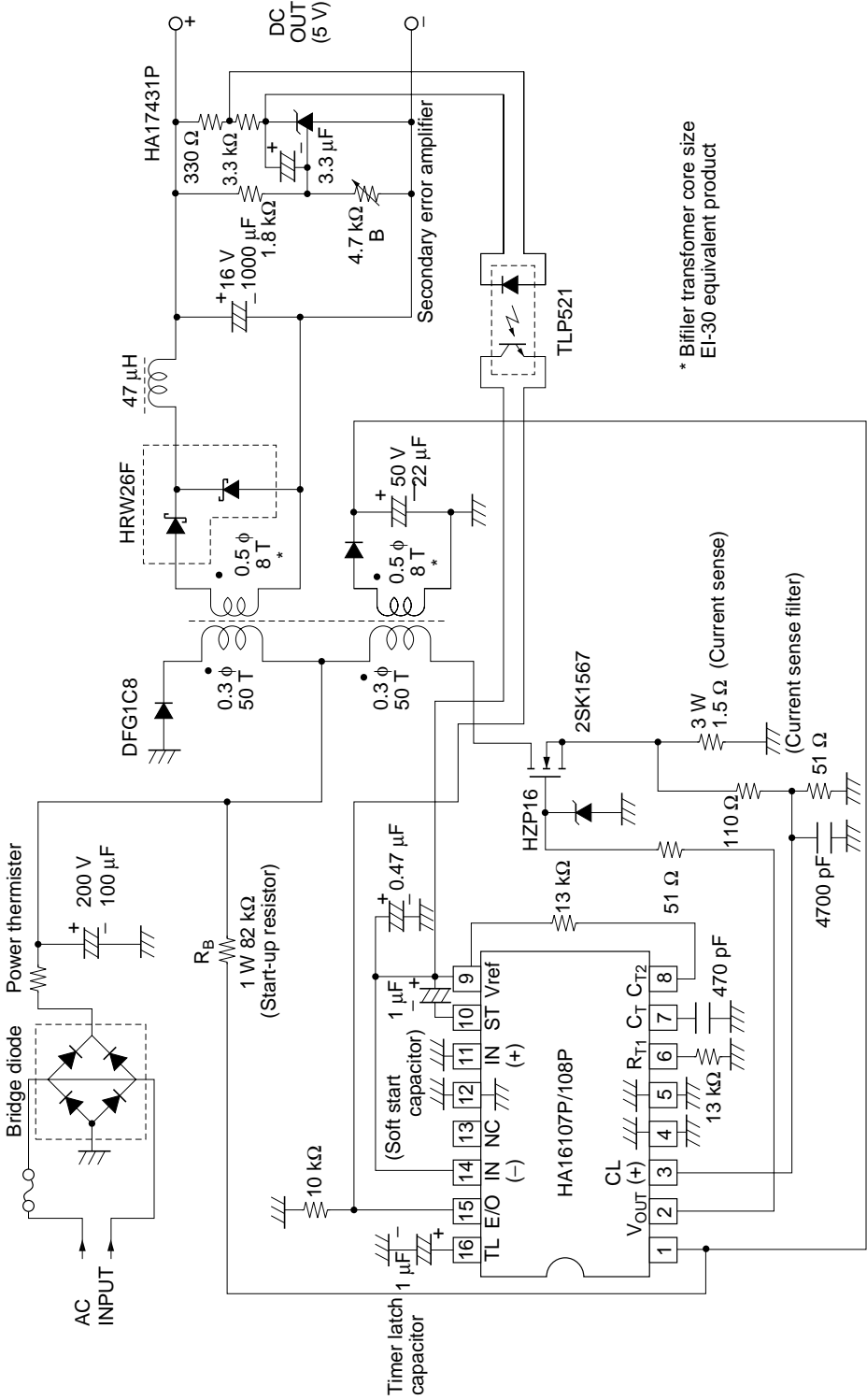
Error Amplifier Characteristic



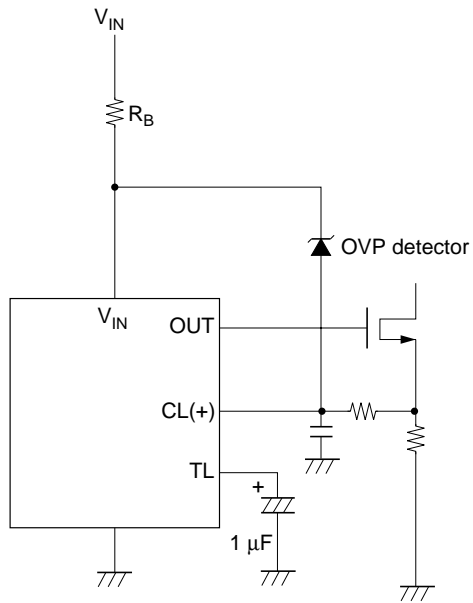
Examples of Drooping Characteristics of Power Supplies Using these ICs



• Forward Transformer Application Example



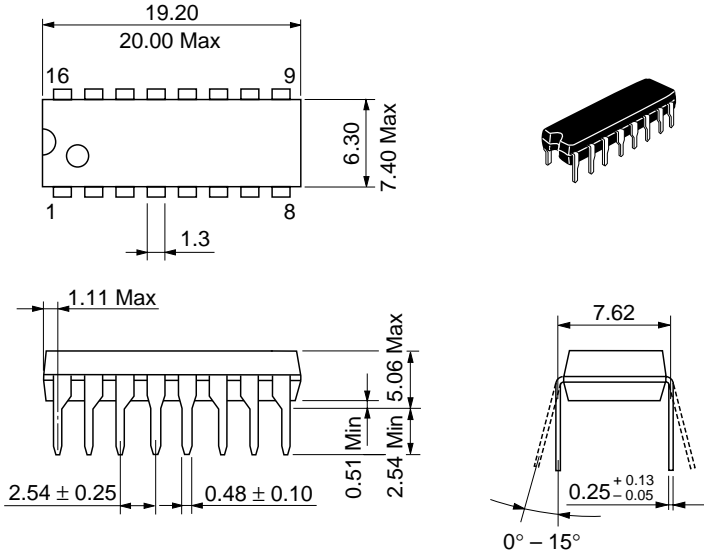
- When OVP signal is inserted at CL(+) pin



When the OVP detection Zener diode turns on, latch shutdown of the output is performed after the elapse of the time determined by the capacitance connected the TL pin.

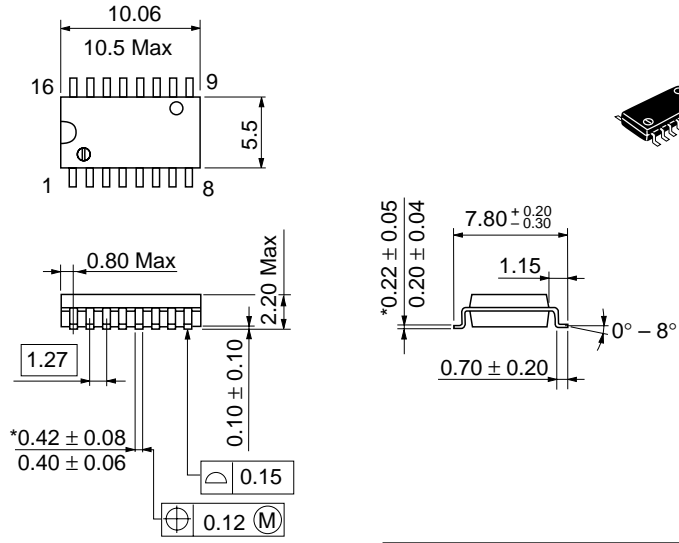
Package Dimensions

Unit: mm



Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Mass (reference value)	1.07 g

Unit: mm



Hitachi Code	FP-16DA
JEDEC	—
EIAJ	Conforms
Mass (reference value)	0.24 g

*Dimension including the plating thickness
Base material dimension

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Hitachi, Ltd.

Semiconductor & Integrated Circuits.
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109

URL NorthAmerica : <http://semiconductor.hitachi.com/>
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For further information write to:

Hitachi Semiconductor
(America) Inc.
179 East Tasman Drive,
San Jose, CA 95134
Tel: <1> (408) 433-1990
Fax: <1>(408) 433-0223

Hitachi Europe GmbH
Electronic Components Group
Dornacher Straße 3
D-85622 Feldkirchen, Munich
Germany
Tel: <49> (89) 9 9180-0
Fax: <49> (89) 9 29 30 00

Hitachi Europe Ltd.
Electronic Components Group.
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA, United Kingdom
Tel: <44> (1628) 585000
Fax: <44> (1628) 585160

Hitachi Asia Ltd.
Hitachi Tower
16 Collyer Quay #20-00,
Singapore 049318
Tel: <65>-538-6533/538-8577
Fax : <65>-538-6933/538-3877
URL : <http://www.hitachi.com.sg>

Hitachi Asia Ltd.
(Taipei Branch Office)
4/F, No. 167, Tun Hwa North Road,
Hung-Kuo Building,
Taipei (105), Taiwan
Tel : <886>-(2)-2718-3666
Fax : <886>-(2)-2718-8180
Telex : 23222 HAS-TP
URL : <http://www.hitachi.com.tw>

Hitachi Asia (Hong Kong) Ltd.
Group III (Electronic Components)
7/F., North Tower,
World Finance Centre,
Harbour City, Canton Road
Tsim Sha Tsui, Kowloon,
Hong Kong
Tel : <852>-(2)-735-9218
Fax : <852>-(2)-730-0281
URL : <http://www.hitachi.com.hk>

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0.0	Oct. 11, 1994	Initial issue	A. Koizumi	M. Yamamura
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0.2	Nov. 12, 1994	Initial issue	A. Koizumi	M. Yamamura