
HA19510/MP

High-Speed, Low-Power 8-bit Flash D/A Converter

HITACHI

November 1996

Description

The HA19510/MP consists of high-speed, low-power 8-bit D/A converters. The digital and clock inputs of these monolithic bipolar LSIs are fully TTL/CMOS compatible. The noise-minimizing internal reference voltage generator and high conversion rate ($f_{CLK} = 40 \text{ MHz Min}$) make these devices suitable for high-speed image processing applications.

Features

- 8-bit resolution
- Conversion rate: 40 MHz (Min)
- Single power supply: +5 V
- TTL/CMOS compatible clock and digital inputs
- Internal reference voltage: +3.0 V (Typ)
- Low power consumption: 225 mW (Typ)

Applications

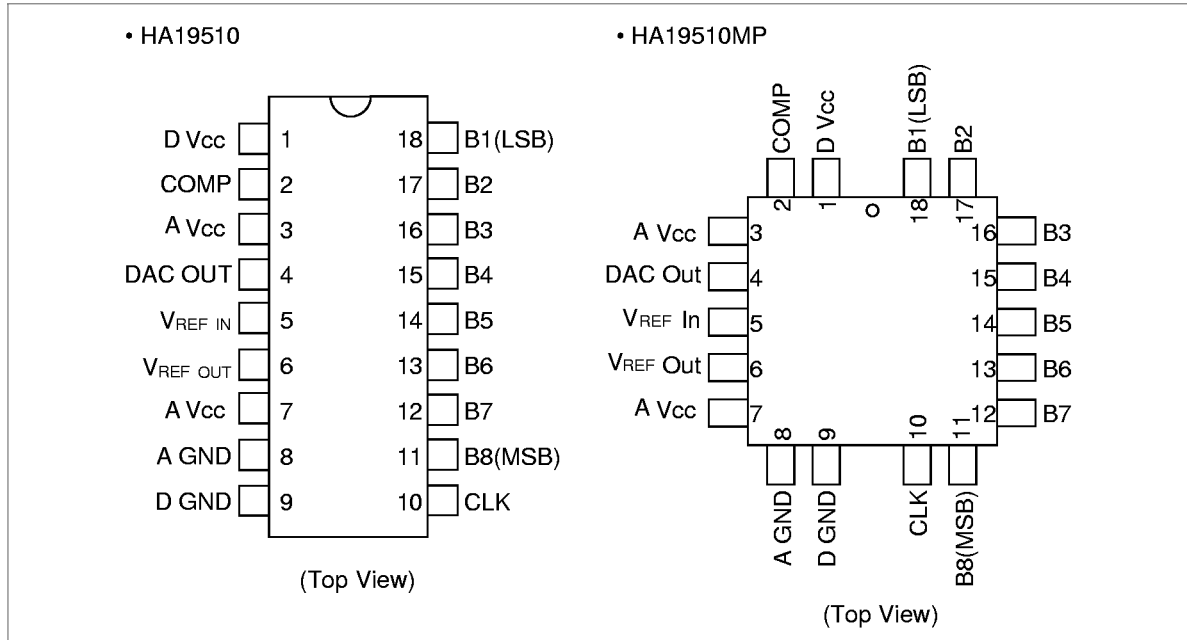
- Video signal processing
- Image processing, etc.

Ordering Information

Type No.	Package
HA19510	300mil 18-pin plastic DIP (DP-18A)
HA19510MP	18-pin plastic QFI (MP-18)

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Pin Arrangement

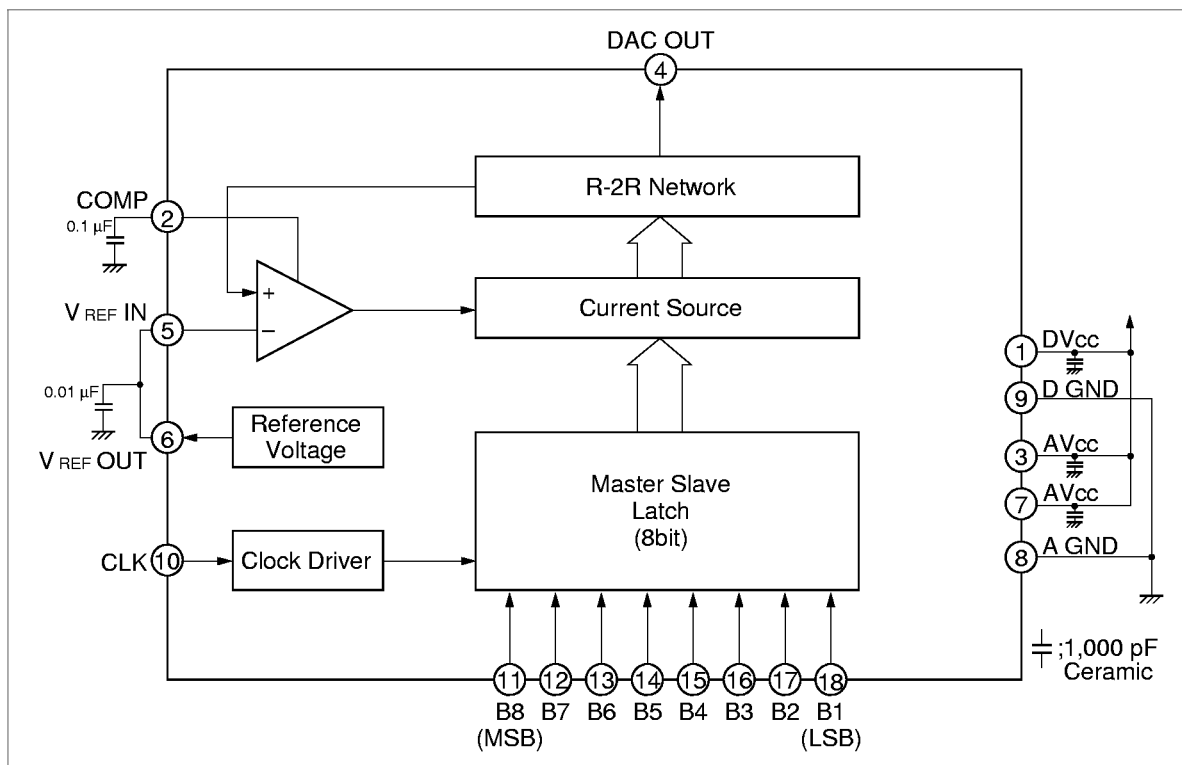


Pin Descriptions

Pin No.	Symbol	Function
1	D V_{CC}	Digital power supply (+5 V)
2	COMP	Phase compensation
3	A V_{CC}	Analog power supply (+5 V)
4	DAC OUT	Analog voltage output
5	$V_{REF IN}$	Reference voltage input
6	$V_{REF OUT}$	Reference voltage output
7	A V_{CC}	Analog power supply (+5 V)
8	AGND	Analog ground
9	DGND	Digital ground
10	CLK	Clock input
11	B8	Digital input (MSB)
12	B7	Digital input
13	B6	Digital input
14	B5	Digital input
15	B4	Digital input
16	B3	Digital input
17	B2	Digital input
18	B1	Digital input (LSB)

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Block Diagram



Absolute Maximum Ratings (Ta = 25°C, unless otherwise specified)

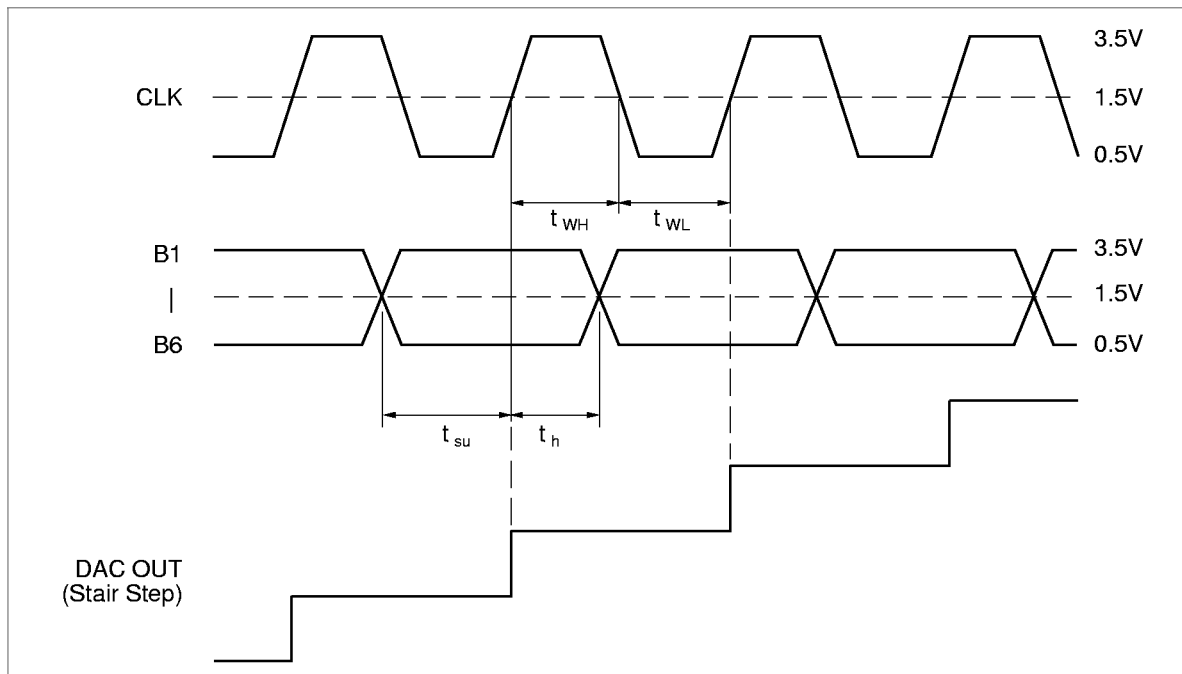
Item	Symbol	Rating	Unit
Power supply voltage	V_{CC}	+7.0	V
Digital input voltage	V_{IN}	0 to V_{CC}	V
Power dissipation	P_T	500	mW
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{stg}	-55 to +125	°C

Electrical Characteristics ($T_a = 25^\circ\text{C}$, $V_{CC} = 5.0\text{ V}$, and pins 5 and 6 are shorted, unless otherwise specified)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Resolution		8	8	8	bit	
Conversion rate	f_{CLK}	40	—	—	MHz	
Linearity error	LE	-0.5	—	0.5	LSB	
Clock pulsewidth H-level	t_{WH}	12.5	—	—	ns	$f_{CLK} = 40\text{ MHz}$
Clock pulsewidth L-level	t_{WL}	12.5	—	—	ns	$f_{CLK} = 40\text{ MHz}$
Data setup time	t_{su}	10	—	—	ns	$f_{CLK} = 40\text{ MHz}$
Data hold time	t_h	10	—	—	ns	$f_{CLK} = 40\text{ MHz}$
Power supply voltage	V_{CC}	4.75	5.00	5.25	V	
Current consumption	I_{CC}	—	45	60	mA	
Digital input voltage	V_{IH}	2.0	—	V_{CC}	V	
	V_{IL}	0	—	0.8	V	
Digital input current	I_{IH}	—	—	20	μA	$V_{IH} = 2.7\text{ V}$
	I_{IL}	-400	—	—	μA	$V_{IL} = 0.4\text{ V}$
Reference input current	$I_{REF\ IN}$	-20	0	20	μA	$V_{REF\ IN} = 3.0\text{ V}$
Reference input voltage	$V_{REF\ IN}$	2.0	3.0	4.0	V	
Reference output voltage	$V_{REF\ OUT}$	3.0	3.1	3.22	V	
Analog output voltage	Full Scale V_{FS}	$V_{CC} - 15\text{ m}$	V_{CC}	$V_{CC} + 15\text{ m}$	V	$V_{IH} \geq 2.0\text{ V}$
	Zero Scale V_{ZS}	3.94	4.00	4.06	V	$V_{IL} \leq 0.8\text{ V}$
Output Impedance	Z_{out}	55	75	95	Ω	

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Timing Chart



Input Code Table

B8	B7	B6	B5	B4	B3	B2	B1	Aout (V)
0	0	0	0	0	0	0	0	V_{ZS}
0	0	0	0	0	0	0	1	$V_{ZS} + 1 \text{ LSB}$
1	1	1	1	1	1	1	0	$V_{FS} - 1 \text{ LSB}$
1	1	1	1	1	1	1	1	V_{FS}

Note: $1 \text{ LSB} = (V_{FS} - V_{ZS})/255$

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