

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC74VHC125F, TC74VHC125FN, TC74VHC125FT
TC74VHC126F, TC74VHC126FN, TC74VHC126FT

TC74VHC125F/FN/FT QUAD BUS BUFFER
TC74VHC126F/FN/FT QUAD BUS BUFFER

(Note) The JEDEC SOP (FN) is not available in Japan.

The TC74VHC125/126 are high speed CMOS QUAD BUS BUFFERS fabricated with silicon gate C²MOS technology. They achieve the high speed operation similar to equivalent Bipolar Shottky TTL while maintaining the CMOS low power dissipation.

The TC74VHC125 requires the 3-state control input \bar{G} to be set high to place the output into the high impedance state, whereas the TC74VHC126 requires the control input G to be set low to place the output into high impedance.

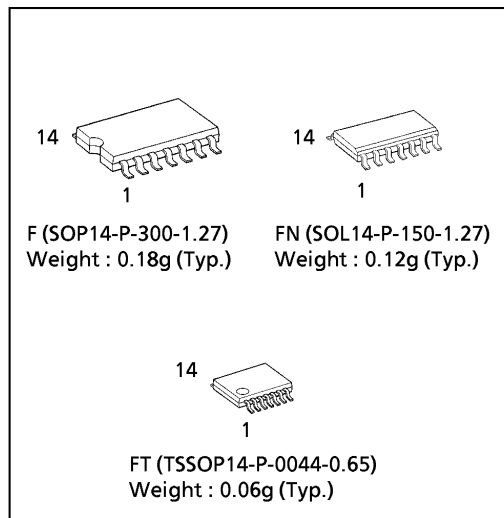
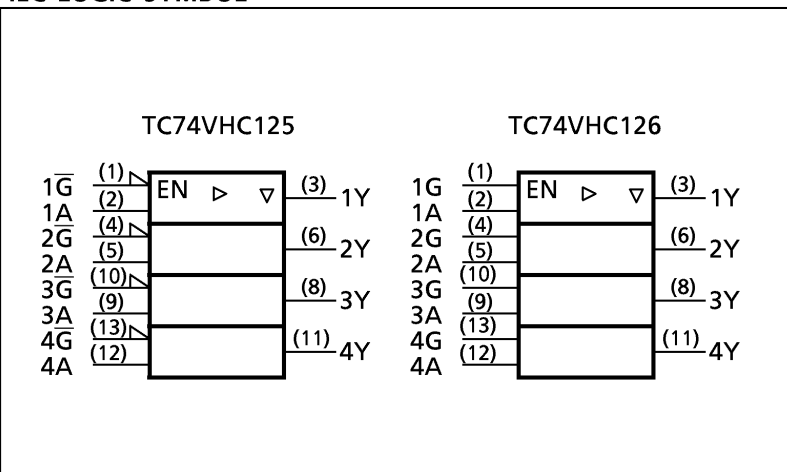
An input protection circuit ensures that 0 to 5.5V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up.

This circuit prevents device destruction due to mismatched supply and input voltages.

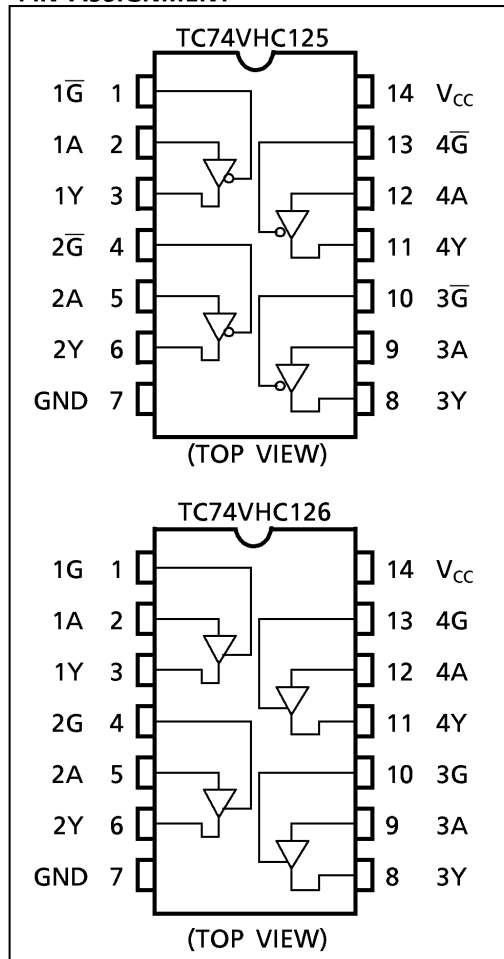
FEATURES :

- High Speed..... $t_{pd} = 3.8ns$ (typ.) at $V_{CC} = 5V$
- Low Power Dissipation..... $I_{CC} = 4\mu A$ (Max.) at $T_a = 25^\circ C$
- High Noise Immunity..... $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (Min.)
- Power Down Protection is provided on all inputs.
- Balanced Propagation Delays..... $t_{pLH} \approx t_{pHL}$
- Wide Operating Voltage Range.... V_{CC} (opr.) = 2V~5.5V
- Low Noise $V_{OLP} = 0.8V$ (Max.)
- Pin and Function Compatible with 74ALS125/126

IEC LOGIC SYMBOL



PIN ASSIGNMENT



980910EBA2

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TRUTH TABLE

TC74VHC125

INPUTS		OUTPUTS
\bar{G}	A	Y
H	X	Z
L	L	L
L	H	H

X: Don't Care
Z: High Impedance

TC74VHC126

INPUTS		OUTPUTS
G	A	Y
L	X	Z
H	L	L
H	H	H

X: Don't Care
Z: High Impedance

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5~7.0	V
DC Input Voltage	V_{IN}	-0.5~7.0	V
DC Output Voltage	V_{OUT}	-0.5~ $V_{CC} + 0.5$	V
Input Diode Current	I_{IK}	-20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC} /Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	180	mW
Storage Temperature	T_{stg}	-65~150	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~5.5	V
Input Voltage	V_{IN}	0~5.5	V
Output Voltage	V_{OUT}	0~ V_{CC}	V
Operating Temperature	T_{opr}	-40~85	°C
Input Rise and Fall Time	dt/dv	0~100 ($V_{CC} = 3.3 \pm 0.3V$) 0~20 ($V_{CC} = 5 \pm 0.5V$)	ns/V

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DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	V _{CC} (V)	Ta = 25°C			Ta = -40~85°C		UNIT	
				MIN.	TYP.	MAX.	MIN.	MAX.		
High - Level Input Voltage	V _{IH}		2.0 3.0~ 5.5	1.50 V _{CC} ×0.7	— —	— —	1.50 V _{CC} ×0.7	—	V	
Low - Level Input Voltage	V _{IL}		2.0 3.0~ 5.5	— —	— —	0.50 V _{CC} ×0.3	— —	0.50 V _{CC} ×0.3	V	
High - Level Output Voltage	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -50μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5	— — —	1.9 2.9 4.4	—	V
			I _{OH} = -4mA I _{OH} = -8mA	3.0 4.5	2.58 3.94	— —	— —	2.48 3.80	— —	
Low - Level Output Voltage	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 50μA	2.0 3.0 4.5	— — —	0.0 0.0 0.0	0.1 0.1 0.1	— — —	0.1 0.1 0.1	V
			I _{OL} = 4mA I _{OL} = 8mA	3.0 4.5	— —	— —	0.36 0.36	— —	0.44 0.44	
3 - State Output Off - State Current	I _{OZ}	V _{IN} = V _{IH} or V _{IL} V _{OUT} = V _{CC} or GND	5.5	—	—	±0.25	—	±2.50	μA	
Input Leakage Current	I _{IN}	V _{IN} = 5.5V or GND	0~5.5	—	—	±0.1	—	±1.0		
Quiescent Supply Current	I _{CC}	V _{IN} = V _{CC} or GND	5.5	—	—	4.0	—	40.0		

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C			Ta = -40~85°C		UNIT
		V _{CC} (V)	CL (pF)	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time	t _{pLH} t _{pHL}	3.3 ± 0.3	15	—	5.6	8.0	1.0	9.5	ns
			50	—	8.1	11.5	1.0	13.0	
	5.0 ± 0.5	15	—	3.8	5.5	1.0	6.5		
		50	—	5.3	7.5	1.0	8.5		
Output Enable time	t _{pZL} t _{pZH}	3.3 ± 0.3	15	—	5.4	8.0	1.0	9.5	
			50	—	7.9	11.5	1.0	13.0	
	5.0 ± 0.5	15	—	3.6	5.1	1.0	6.0		
		50	—	5.1	7.1	1.0	8.0		
Output Disable time	t _{pLZ} t _{pHZ}	3.3 ± 0.3	50	—	9.5	13.2	1.0	15.0	
			5.0 ± 0.5	50	—	6.1	8.8	1.0	10.0
Output to Output Skew	t _{osLH} t _{osHL}	(Note 1)	3.3 ± 0.3	50	—	—	1.5	—	1.5
			5.0 ± 0.5	50	—	—	1.0	—	1.0
Input Capacitance	C _{IN}			—	4	10	—	10	pF
Output Capacitance	C _{OUT}			—	6	—	—	—	
Power Dissipation Capacitance (Note 2)	C _{PD}	TC74VHC125		—	14	—	—	—	
		TC74VHC126		—	15	—	—	—	

Note (1) Parameter guaranteed by design. $t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$

Note (2) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

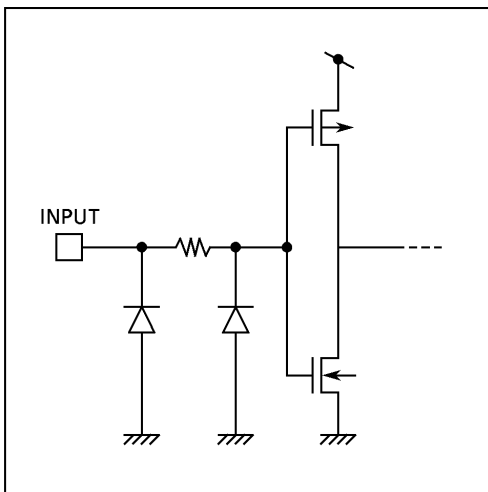
Average operating current can be obtained by the equation :

$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 4 \text{ (per Gate)}$$

NOISE CHARACTERISTICS (Input $t_r = t_f = 3ns$)

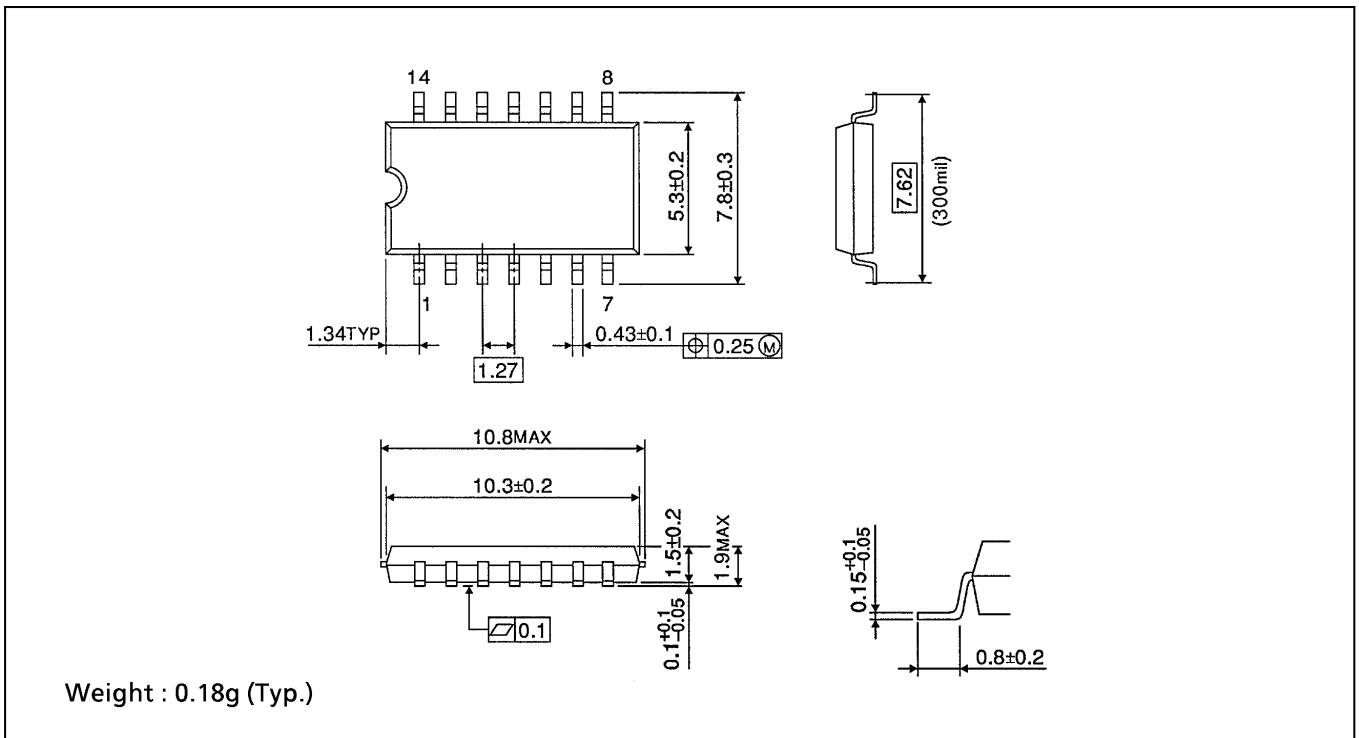
PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C			UNIT
			V _{CC} (V)	TYP.	LIMIT	
Quiet Output Maximum Dynamic V _{OL}	V _{OLP}	C _L = 50pF	5.0	0.3	0.8	V
Quiet Output Minimum Dynamic V _{OL}	V _{OLV}	C _L = 50pF	5.0	-0.3	-0.8	V
Minimum High Level Dynamic Input Voltage	V _{IHD}	C _L = 50pF	5.0	-	3.5	V
Maximum Low Level Dynamic Input Voltage	V _{ILD}	C _L = 50pF	5.0	-	1.5	V

INPUT EQUIVALENT CIRCUIT



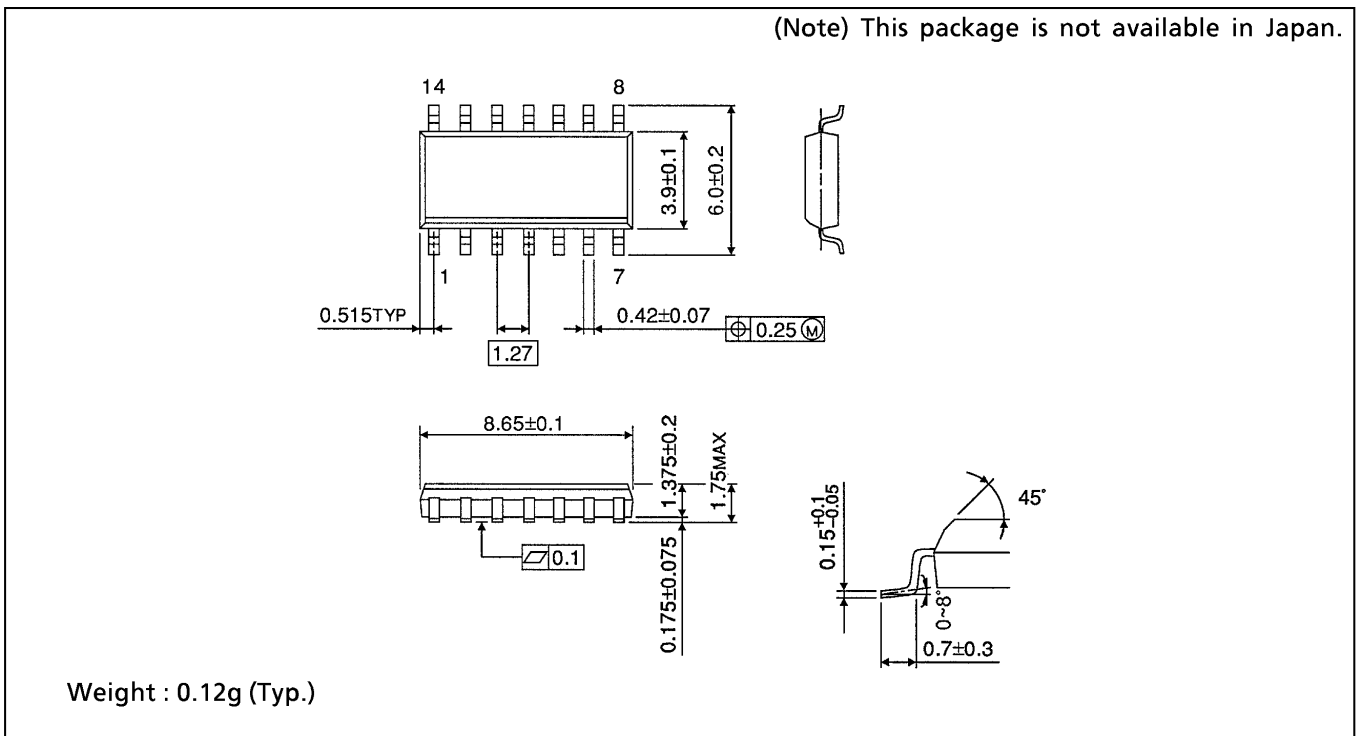
SOP 14PIN (200mil BODY) PACKAGE DIMENSIONS (SOP14-P-300-1.27)

Unit in mm



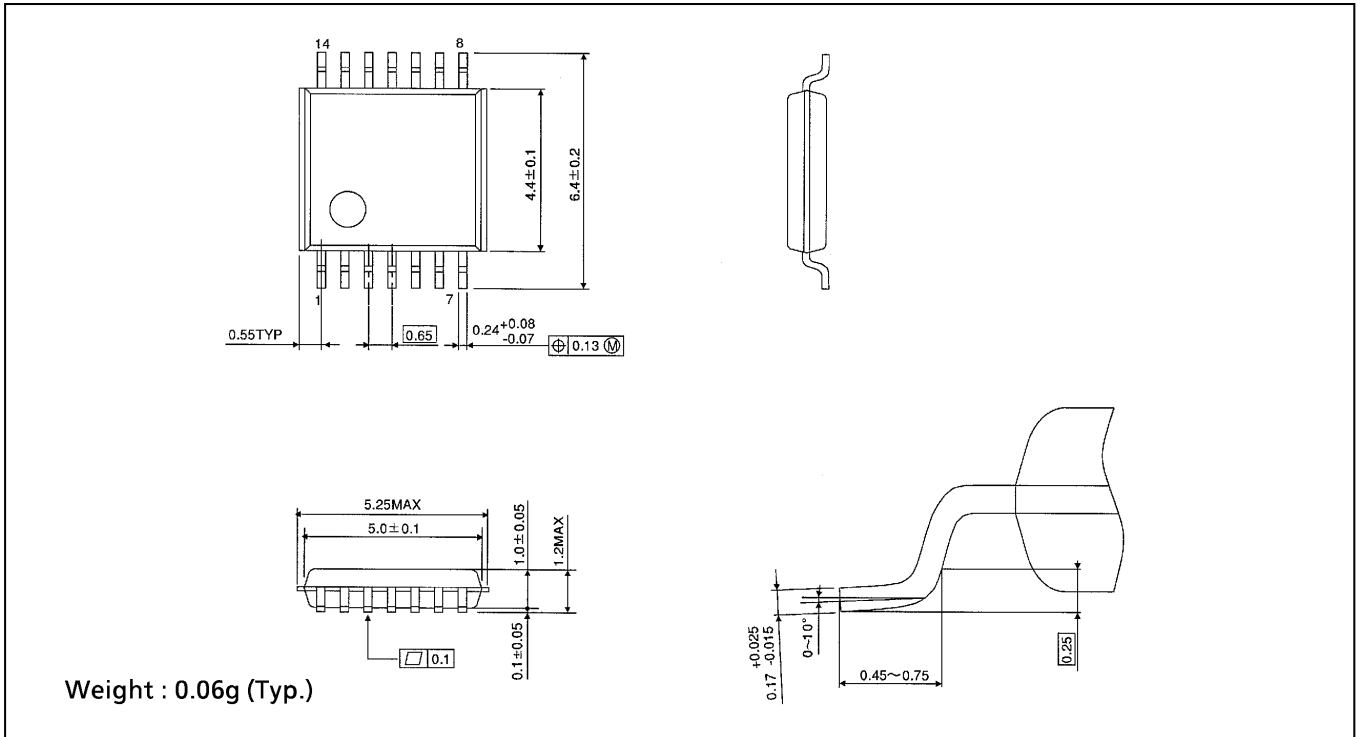
SOP 14PIN (150mil BODY) PACKAGE DIMENSIONS (SOP14-P-150-1.27)

Unit in mm



TSSOP 14PIN PACKAGE DIMENSIONS (TSSOP14-P-0044-0.65)

Unit in mm



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