



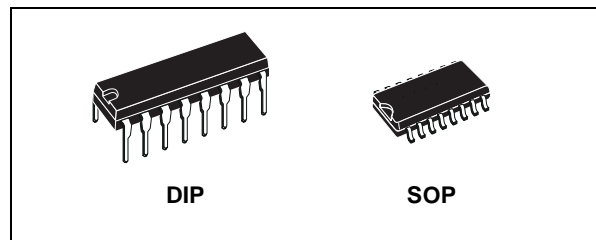
# HCF40174B

## HEX "D" TYPE FLIP-FLOP

- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- QUIESCENT CURRENT SPECIFIED UP TO 20V
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- INPUT LEAKAGE CURRENT  
 $I_l = 100\text{nA (MAX) AT } V_{DD} = 18\text{V } T_A = 25^\circ\text{C}$
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC JESD13B "STANDARD SPECIFICATIONS FOR DESCRIPTION OF B SERIES CMOS DEVICES"

### DESCRIPTION

HCF40174B is a monolithic integrated circuit fabricated in Metal Oxide Semiconductor technology available in DIP and SOP packages. HCF40174B consists of six identical "D" Type flip-flops having independent DATA inputs. The

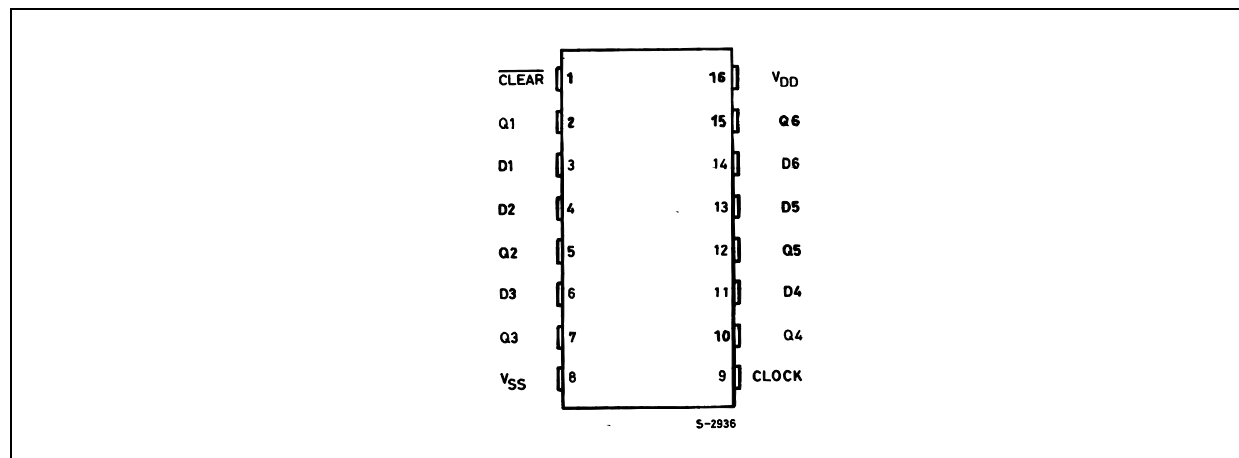


### ORDER CODES

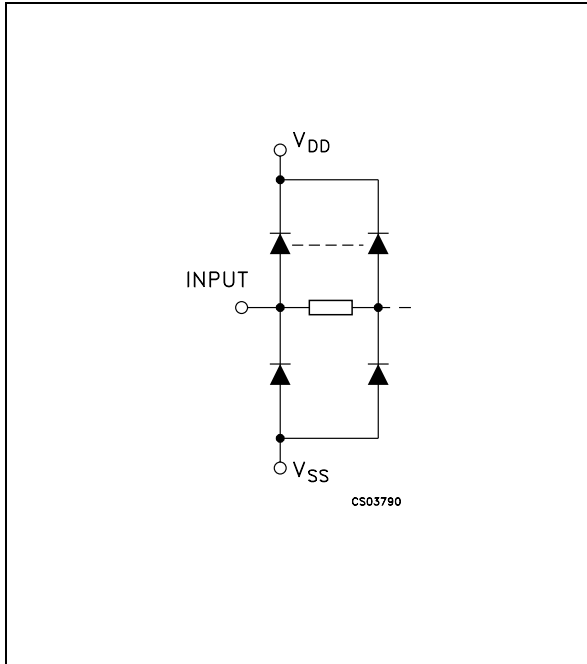
PACKAGE	TUBE	T & R
DIP	HCF40174BEY	
SOP	HCF40174BM1	HCF40174M013TR

CLOCK and  $\overline{\text{CLEAR}}$  inputs are common in all six units. Data is transferred to the Q outputs on the positive-going transition of the clock pulse. All six flip-flops are simultaneously reset by a low level on the  $\overline{\text{CLEAR}}$  input.

### PIN CONNECTION



**IINPUT EQUIVALENT CIRCUIT**



**PIN DESCRIPTION**

PIN No	SYMBOL	NAME AND FUNCTION
3, 4, 6, 11, 13, 14	D1 to D6	Data Inputs
2, 5, 7, 10, 12, 15	Q1 to Q6	Data Outputs
9	CLOCK	Common Clock Inputs
1	CLEAR	Common Clear Inputs
8	V <sub>SS</sub>	Negative Supply Voltage
16	V <sub>DD</sub>	Positive Supply Voltage

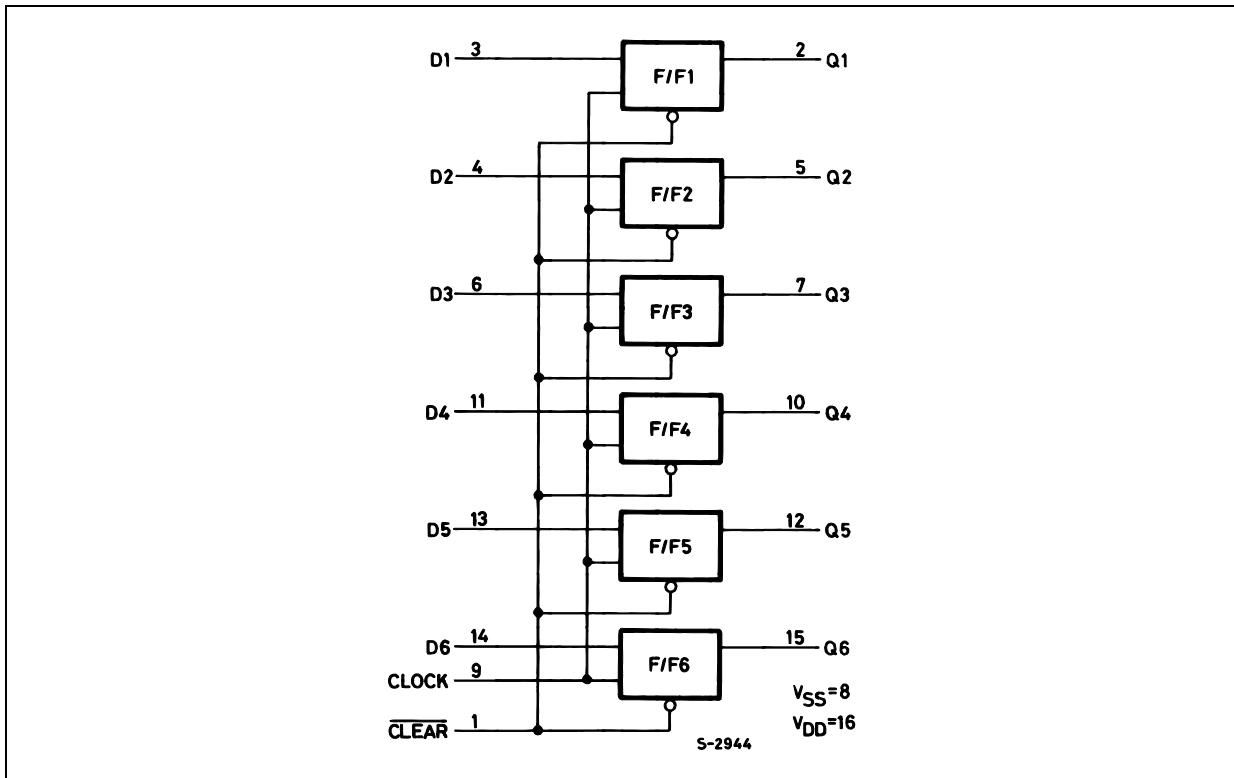
**TRUTH TABLE**

INPUTS			OUTPUT
CLOCK	DATA	<u>CLEAR</u>	Q
	L	H	L
	H	H	H
	X	H	NC
X	X	L	L

X : Don't Care

NC : NO CHANGE

**FUNCTIONAL DIAGRAM**





## DC SPECIFICATIONS

Symbol	Parameter	Test Condition				Value						Unit	
		V <sub>I</sub> (V)	V <sub>O</sub> (V)	I <sub>OL</sub>   ( $\mu$ A)	V <sub>DD</sub> (V)	T <sub>A</sub> = 25°C			-40 to 85°C		-55 to 125°C		
						Min.	Typ.	Max.	Min.	Max.	Min.		Max.
I <sub>L</sub>	Quiescent Current	0/5			5		0.02	1		30		30	$\mu$ A
		0/10			10		0.02	2		60		60	
		0/15			15		0.02	4		120		120	
		0/20			20		0.02	20		600		600	
V <sub>OH</sub>	High Level Output Voltage	0/5		<1	5	4.95			4.95		4.95		V
		0/10		<1	10	9.95			9.95		9.95		
		0/15		<1	15	14.95			14.95		14.95		
V <sub>OL</sub>	Low Level Output Voltage	5/0		<1	5		0.05			0.05		0.05	V
		10/0		<1	10		0.05			0.05		0.05	
		15/0		<1	15		0.05			0.05		0.05	
V <sub>IH</sub>	High Level Input Voltage		0.5/4.5	<1	5	3.5			3.5		3.5		V
			1/9	<1	10	7			7		7		
			1.5/13.5	<1	15	11			11		11		
V <sub>IL</sub>	Low Level Input Voltage		4.5/0.5	<1	5			1.5		1.5		1.5	V
			9/1	<1	10			3		3		3	
			13.5/1.5	<1	15			4		4		4	
I <sub>OH</sub>	Output Drive Current	0/5	2.5	<1	5	-1.1	-2.6		-0.9		-0.9		mA
		0/5	4.6	<1	5	-0.31	-0.75		-0.25		-0.25		
		0/10	9.5	<1	10	-0.68	-1.6		-0.54		-0.54		
		0/15	13.5	<1	15	-2.3	-5.4		-1.84		-1.84		
I <sub>OL</sub>	Output Sink Current	0/5	0.4	<1	5	0.44	1		0.36		0.36		mA
		0/10	0.5	<1	10	1.1	2.6		0.9		0.9		
		0/15	1.5	<1	15	3.0	6.8		2.4		2.4		
I <sub>I</sub>	Input Leakage Current	0/18	Any Input		18		$\pm 10^{-5}$	$\pm 0.1$		$\pm 1$		$\pm 1$	$\mu$ A
C <sub>I</sub>	Input Capacitance		Any Input				5	7.5					pF

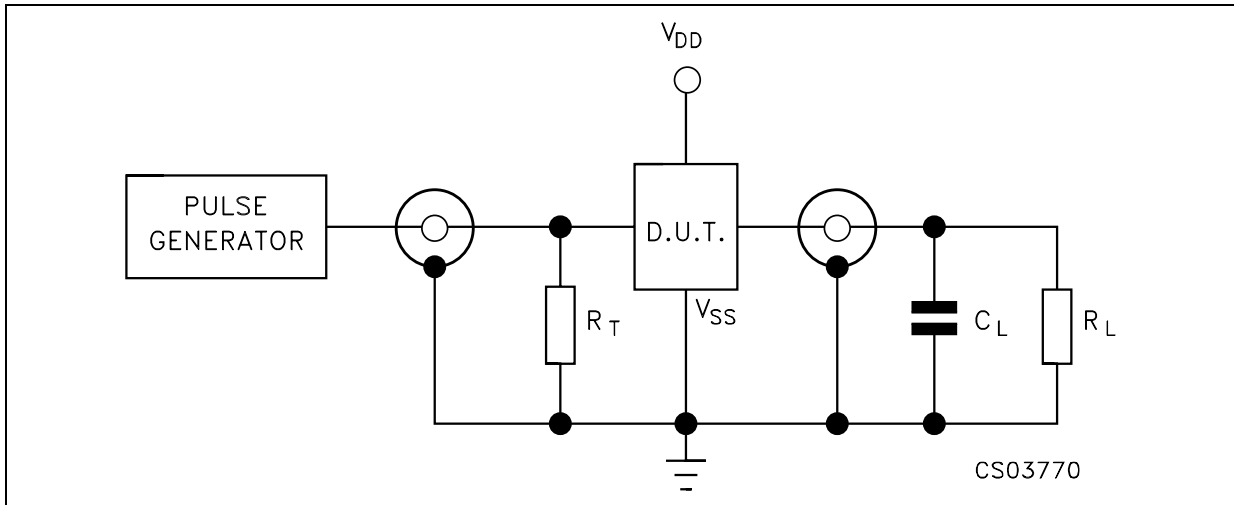
The Noise Margin for both "1" and "0" level is: 1V min. with V<sub>DD</sub>=5V, 2V min. with V<sub>DD</sub>=10V, 2.5V min. with V<sub>DD</sub>=15V

**DYNAMIC ELECTRICAL CHARACTERISTICS** ( $T_{amb} = 25^{\circ}\text{C}$ ,  $C_L = 50\text{pF}$ ,  $R_L = 200\text{K}\Omega$ ,  $t_r = t_f = 20\text{ ns}$ )

Symbol	Parameter	Test Condition		Value (*)			Unit
		$V_{DD}$ (V)		Min.	Typ.	Max.	
$t_{PLH}$ , $t_{PHL}$	Propagation Delay Time : Clock to Output	5			150	300	ns
		10			70	140	
		15			50	100	
$t_{PHL}$	Propagation Delay Time : Clear to Output	5			100	200	ns
		10			50	100	
		15			40	80	
$t_{THL}$ , $t_{TLH}$	Transition Time	5			100	200	ns
		10			50	100	
		15			40	80	
$t_{setup}$	Data Setup Time	5		40	20		ns
		10		20	10		
		15		10	0		
$t_{hold}$	Data Hold Time	5		80	40		ns
		10		40	20		
		15		30	15		
$t_W$	Clock Input Pulse Widht Low Level	5		130	65		ns
		10		60	30		
		15		40	20		
$t_W$	Clear Input Pulse Widht HIGH and LOW	5		100	50		ns
		10		50	25		
		15		40	20		
$t_r$ , $t_f$	Clock Input Rise or Fall Time	5				15	$\mu\text{s}$
		10				15	
		15				15	
$t_{rem}$	Clear Removal Time	5		0	-40		ns
		10		0	-15		
		15		0	-10		
$f_{CL}$	Maximum Clock Input Frequency	5		3.5	7		MHz
		10		6	12		
		15		8	16		

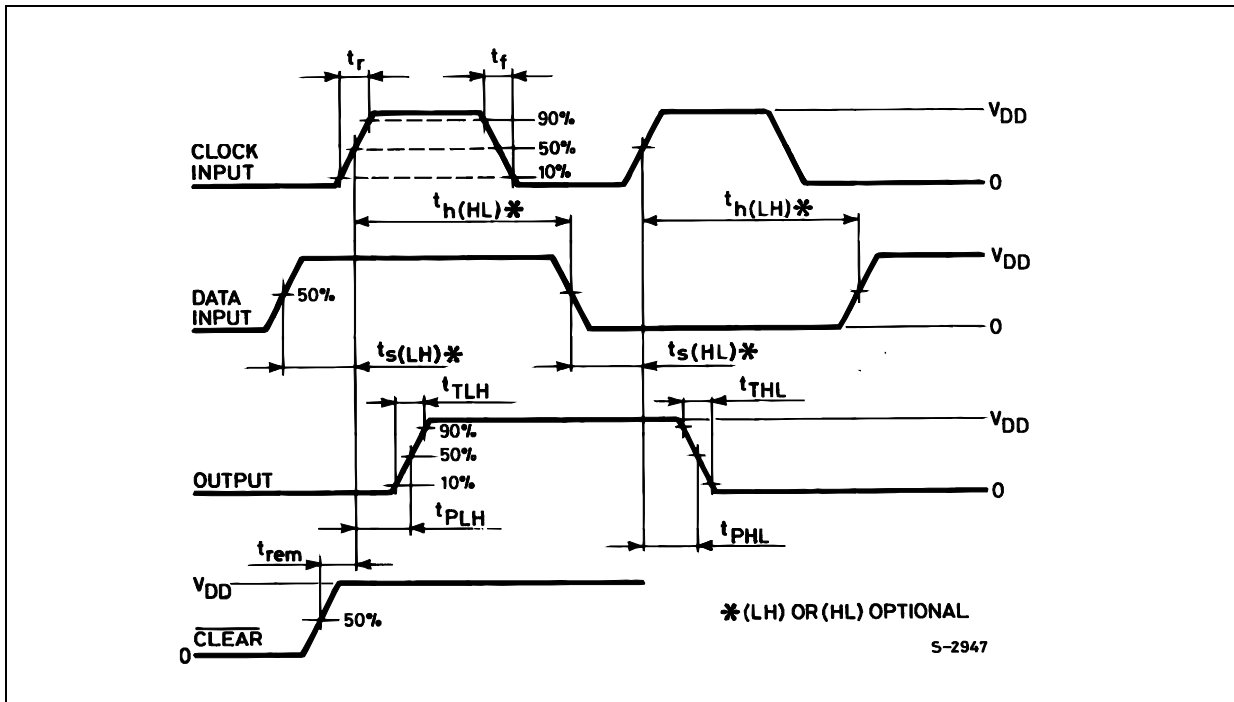
(\*) Typical temperature coefficient for all  $V_{DD}$  value is 0.3 %/°C.

TEST CIRCUIT



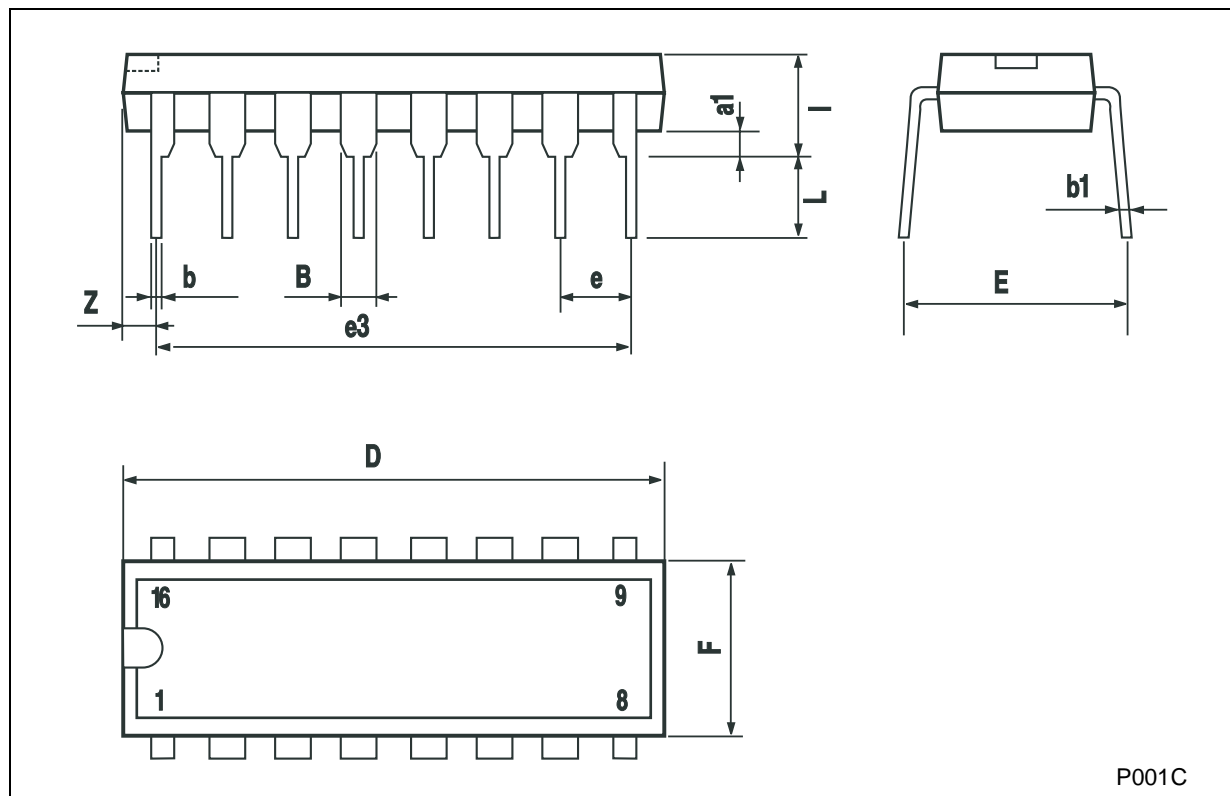
$C_L = 50\text{pF}$  or equivalent (includes jig and probe capacitance)  
 $R_L = 200\text{k}\Omega$   
 $R_T = Z_{OUT}$  of pulse generator (typically  $50\Omega$ )

WAVEFORM : PROPAGATION DELAY TIMES (f=1MHz; 50% duty cycle)



**Plastic DIP-16 (0.25) MECHANICAL DATA**

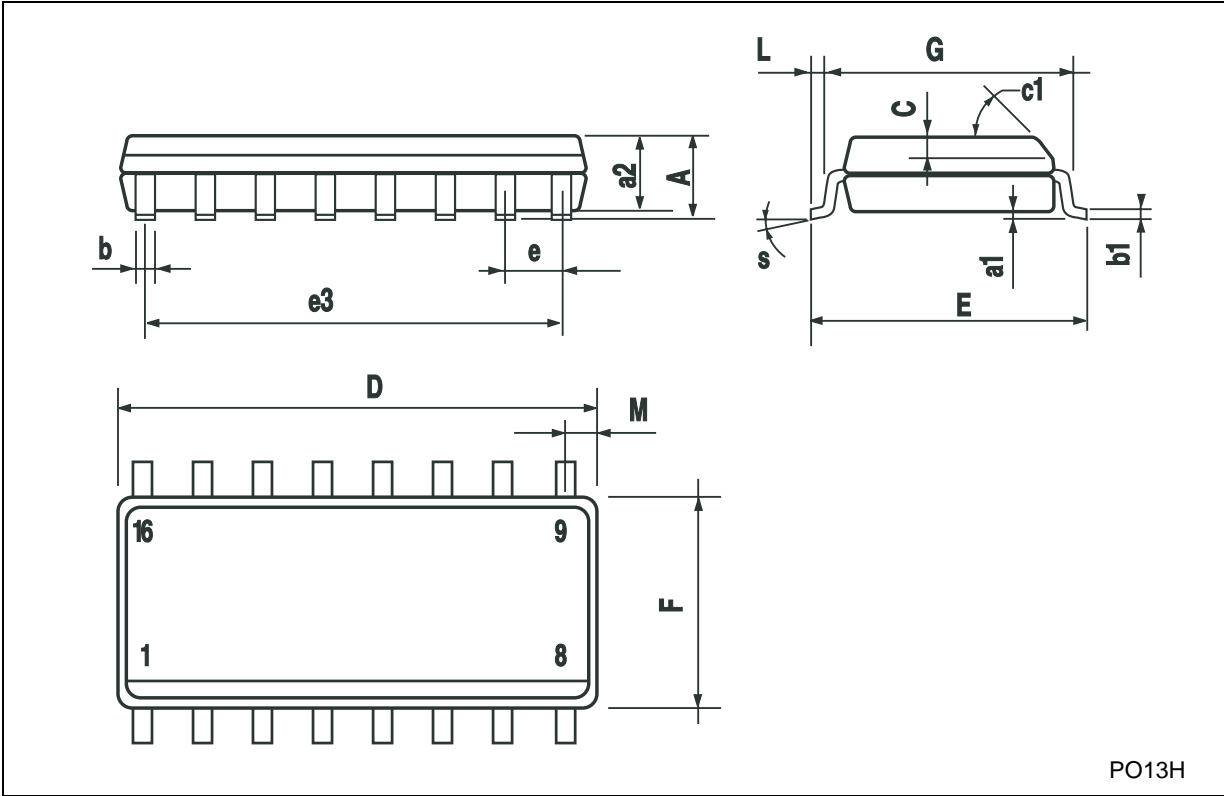
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



P001C

**SO-16 MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8° (max.)					



PO13H

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