Agilent HDMP-1687 Four Channel SerDes Circuit for Gigabit Ethernet and Fibre Channel

Data Sheet

Features

- **Four ANSI x3.230- 1994 Fibre Channel (FC-0) or IEEE 802.3z Gigabit Ethernet compatible SerDes in a single package**
- **Supports serial data rates of 1062.5 MBd (Fibre Channel) & 1250 MBd (Gigabit Ethernet)**
- **Based on X3T11 Fibre Channel "10 bit specification"**
- **Uses reference clock (RFCT) for Tx data latching**
- **Half or full speed Rx clocks**
- **5-Volt tolerant TTL I/Os**
- **Low power consumption**
- **208 ball, 23 mm TBGA package**
- **Single +3.3 V power supply**
- **1.5 kV ESD protection on all pins**
- **Equalizers on inputs**
- **Copper drive capability**
- **Buffered line logic outputs**

Applications

- **1250 MBd Gigabit Ethernet high density ports**
- **1062.5 MBd Fibre Channel interface**
- **Mass storage system I/O channel**
- **Work station/server I/O channel**
- **FC interface for disk drives and arrays**
- **Serial backplanes**
- **Clusters**

Functional Description

The HDMP-1687 is a four channel SERDES device. HDMP-1687 is in a 208-ball TBGA package with four 1.0625/1.25 Gbps serial I/O. This integrated circuit provides a low-cost, low-power, small-form-factor physical-layer solution for multi-link Gigabit Ethernet/Fibre Channel interfaces. This IC may be used to directly drive copper cables, or it may be used to interface with optical transceivers. Each IC contains transmit and receive channel circuitry for all four channels.

The transmitter section accepts 10-bit-wide parallel TTL data on each channel and serializes it into a high-speed serial stream. The parallel data is expected to be 8B/10B encoded (or equivalent). Four banks of parallel data are latched into the input registers of the transmitter sections on the rising edge of RFCT.

Receive data are latched out with separate clock pins for each channel. These pins may be single 106.25/125 MHz TTL clock outputs RC [0:3] [1] or dual 53.125/62.5 MHz TTL pairs RC [0:3] [0:1] to serve legacy applications where single SerDes devices were used before. The receive clock mode select (RCM0) pin is used to define the designer's choice.

RCM0	Receive Clock Mode
0	half speed dual clocks
1	full speed single clocks

The SYNC pin enables bytesync detection on all four channels. When a comma character is detected on any channel, its corresponding SYN [0:3] pin goes high.

A single LOOP pin is provided for all channels to enable the local loopback function.

HDMP-1687 Block Diagram

The following is a description of the blocks in each channel. Except for the transmit PLL section, circuits for the channels are independent. Figure 1 shows how this IC may be connected to a protocol device that controls four channels. Each channel of the four channel SERDES (Figure 2) was designed to transmit and receive 10-bit-wide characters over dedicated differential high-speed lines. The parallel data applied to the transmitter is expected to be encoded per the 8B/10B encoding scheme, with special reserve characters for link management purposes. Other encoding schemes will also work as long as they provide dc balance and sufficient transition density. In order to accomplish this task, the SERDES circuitry incorporates the following:

- TTL parallel I/Os
- High-speed phase locked loops
- Parallel-to-serial converter
- High-speed serial clock and data recovery circuitry
- Comma character recognition circuitry for 8B/10B
- Character alignment circuitry
- Serial-to-parallel converter

PARALLEL INPUT LATCH

The transmitter accepts 10-bit wide single-ended TTL parallel data at inputs TX [0:3] [0:9]. The RFCT pin is used as transmit byte clock. The TX [0:3] [0:9] and RFCT signals must be properly aligned, as shown in Figure 3. RFCT is also used as a clean frequency reference for the receiver PLLs.

TX PLL/CLOCK GENERATOR

The transmitter Phase Locked Loop and Clock Generator (TX PLL/CLOCK GENERATOR) block generates all internal clocks needed by the transmitter section to perform its functions. These clocks are based on the supplied reference clock (RFCT). RFCT is used as the frequency reference clock for the PLL as well as for the incoming data latches. The RFCT clock is multiplied by 10 to generate the serial rate clock necessary for clocking the high speed serial outputs.

FRAME MUX

The FRAME MUX accepts the 10-bit wide parallel data from the INPUT LATCH. Using internally generated high speed clocks, this parallel data is multiplexed into serial data streams. The data bits are transmitted sequentially, from TX [0:3] [0] to TX [0:3] [9].

SERIAL OUTPUT SELECT

The OUTPUT SELECT block provides for an optional internal loopback of the high speed serial signal for testing purposes. In normal operation, LOOP is set low and the serial data stream is placed at SO [0:3]±. When wrap-mode is activated by setting LOOP high, the SO [0:3]± pins are held static at logic 1 and the serial output signal is internally wrapped to the INPUT SELECT block of the receiver section.

SERIAL INPUT SELECT

The INPUT SELECT block determines whether the signal at SI [0:3]± or the internal loopback serial signal is used. In normal operation, LOOP is set low and the serial data is accepted at SI [0:3]±. When LOOP is set high, the outgoing high speed serial signal is internally looped-back from the transmitter section to the receiver section. This feature allows parallel loopback testing, exclusive of the transmission medium.

RX PLL/CLOCK RECOVERY

The RX PLL/CLOCK RECOVERY block is responsible for frequency and phase locking onto the incoming serial data stream and recovering the bit and byte clocks. The Rx PLL continually frequency locks onto the reference clock, and then phase locks onto the selected input data stream. The frequency lock part of the PLL is shared among all channels. Phase locking is performed separately on each channel. An internal signal detection circuit monitors the presence of the input, and invokes the phase detection once the minimum differential input signal level is supplied (AC Electrical Specifications). Once bit locked, the receiver generates the high speed sampling clock at serial data rates for the input sampler.

SERIAL INPUT SAMPLER

The INPUT SAMPLER converts the serial input signal into a high speed serial bit stream. In order to accomplish this, it uses the high speed serial clock recovered from the RX PLL/CLOCK RECOVERY block. This serial bit stream is sent to the FRAME DEMUX AND BYTE SYNC block.

FRAME DEMUX, BYTE SYNC

The FRAME DEMUX, BYTE SYNC block is responsible for restoring the 10-bit parallel data from the high speed serial bit stream. This block is also responsible for recognizing the comma character (K28.5+) of positive disparity (0011111xxx). When recognized, the FRAME DEMUX, CHAR SYNC block works with the RX PLL/CLOCK RECOVERY block to properly select the parallel data edge out of the bit stream so that the comma character starts at bit RX [0:3] [0]. When a comma character is detected and realignment of the receiver byte clock RC [0:3] [0:1] is necessary, this clock is stretched, not slivered, to the next possible correct alignment position. This clock will be fully aligned by the start of the second 4-byte ordered set. The second comma character received will be aligned with the rising edge of RC [0:3] [1] and will follow it with a delay. This delay guarantees hold time at the receiving ICs input latches. Comma characters of positive disparity must not be transmitted in consecutive bytes to allow the receiver byte clocks to maintain their proper recovered frequencies.

PARALLEL OUTPUT DRIVERS

The OUTPUT DRIVERS present the 10-bit parallel recovered data byte properly aligned to the receive byte clocks RC [0:3] [0:1] as shown in Figure 5. These output data buffers provide single ended TTL compatible signals.

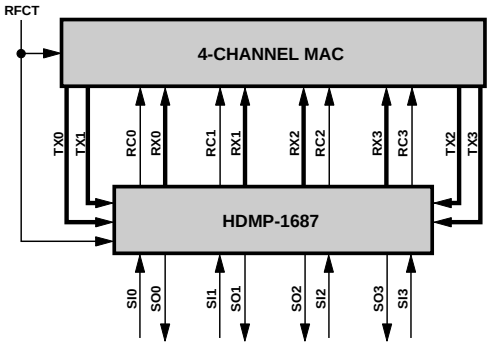


Figure 1. Typical application using HDMP-1687.

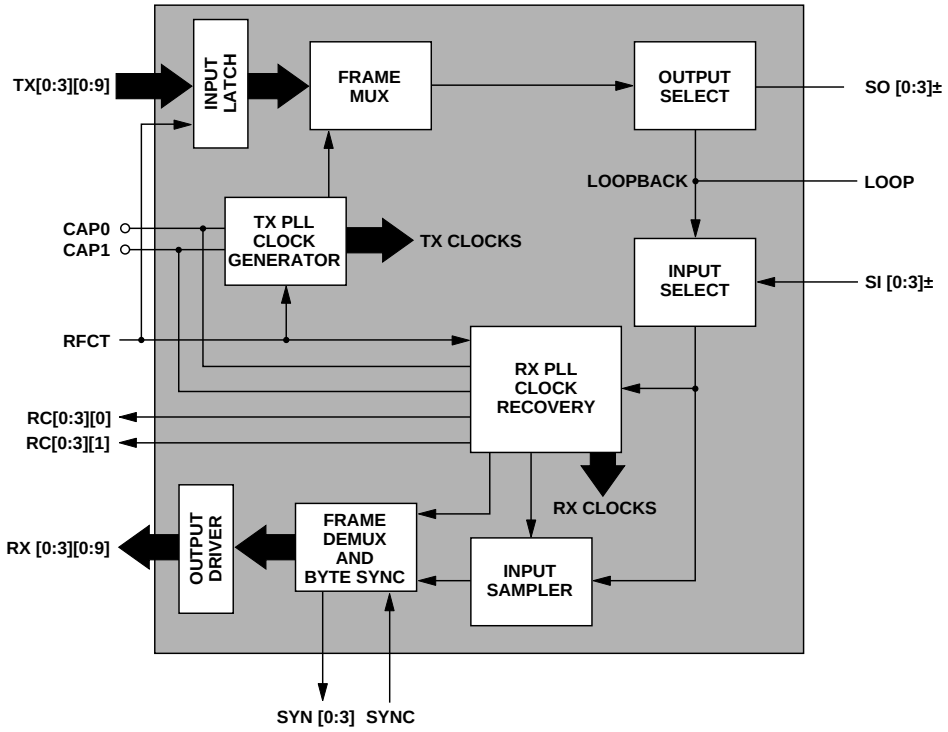


Figure 2. Block diagram of HDMP-1687.

Timing Characteristics for Gigabit Ethernet – Transmitter Section

T = 0°C Ambient to +85°C Case, V_{CC} = 3.15 V to 3.45 V

Symbol	Parameter	Units	Min.	Typ.	Max.
$T_{txsetup}$	Tx Input Setup Time	ns	1.5		
T_{txhold}	Tx Input Hold Time	ns	0.5		
t_txlat[1]	Transmitter Latency	ns		2.3	
		bits		2.8	

Note:

1. The transmitter latency, as shown in Figure 4, is defined as the time between the latching in of the parallel data word (as triggered by the rising edge of the transmit byte clock, RFCT) and the transmission of the first serial bit of that parallel word (defined by the edge of the first bit transmitted).

Timing Characteristics for Fibre Channel – Transmitter Section

T = 0°C Ambient to +85°C Case, V_{CC} = 3.15 V to 3.45 V

Symbol	Parameter	Units	Min.	Typ.	Max.
$T_{txsetup}$	Tx Input Setup Time	ns	2.0		
T_{txhold}	Tx Input Hold Time	ns	1.5		
t_txlat[1]	Transmitter Latency	ns		3.8	
		bits		4.0	

Note:

1. The transmitter latency, as shown in Figure 4, is defined as the time between the latching in of the parallel data word (as triggered by the rising edge of the transmit byte clock, RFCT) and the transmission of the first serial bit of that parallel word (defined by the edge of the first bit transmitted).

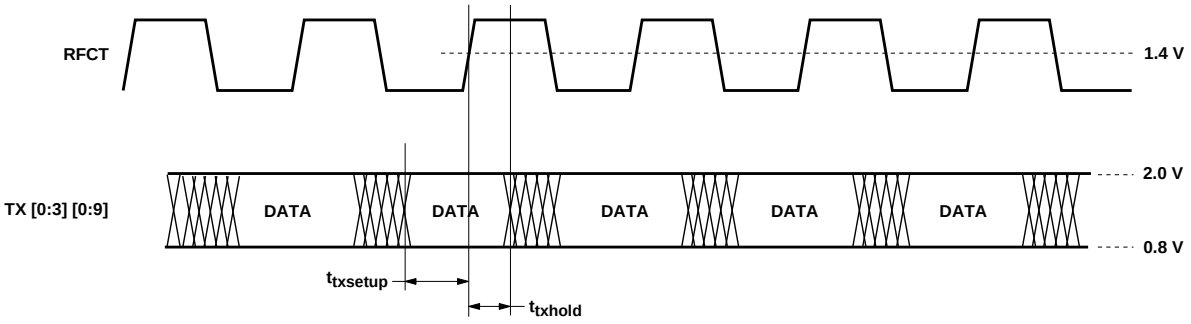


Figure 3. Transmitter section timing.

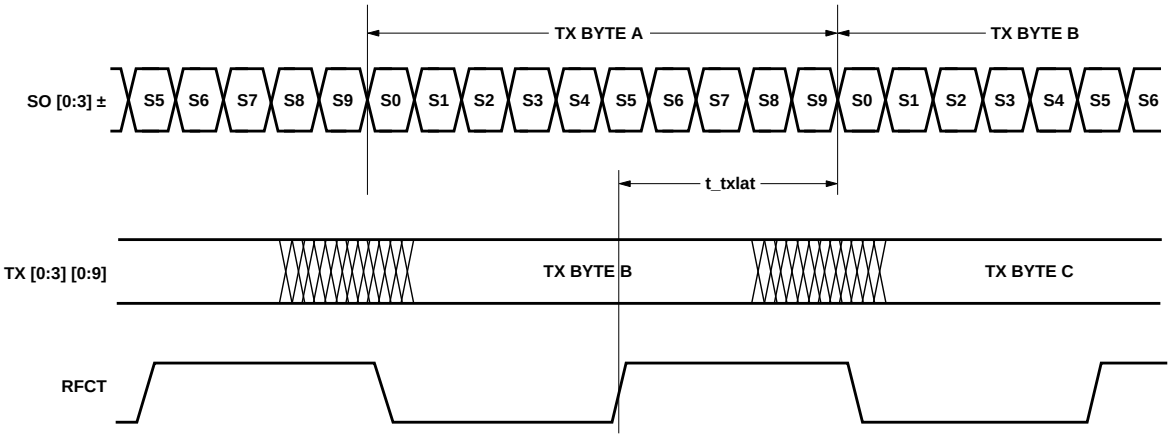


Figure 4. Transmitter latency.

Timing Characteristics for Gigabit Ethernet – Receiver Section

T = 0°C Ambient to +85°C Case, V_{CC} = 3.15 V to 3.45 V

Symbol	Parameter	Units	Min.	Typ.	Max.
f_lock	Frequency Lock at Powerup	µs			500
b_sync[1,2]	Bit Sync Time	bits			2500
$t_{rxsetup}$	RX [0:3][0:9] Output Setup Time (Data Valid Before Clock)	ns	2.5		
t_{rxhold}	RX [0:3][0:9] Output Hold Time (Data Valid After Clock)	ns	2.0		
T_{duty}	RC [0:3][0] and RC [0:3][1] Duty Cycle	%	40		60
t_{A-B}	Rising Edge Time Difference between RBC0 and RBC1 (Half Rate)	ns	7.5		8.5
t_rxlat[3]	Receiver Latency	ns bits		20.7 26.0	

Notes:

1. This is the recovery time for input phase jumps, per the Fibre Channel Specification X3.230-1994 FC-PH Standard, Sec 5.3.
2. Tested using C_{PLL} = 0.1 µF.
3. The receiver latency, as shown in Figure 6, is defined as the time between receiving the first serial bit of a parallel data word (defined as the edge of the first serial bit) and the clocking out of that parallel word (defined by the rising edge of the receive byte clock, RC[0:1]).

Timing Characteristics for Fibre Channel – Receiver Section

T = 0°C Ambient to +85°C Case, V_{CC} = 3.15 V to 3.45 V

Symbol	Parameter	Units	Min.	Typ.	Max.
f_lock	Frequency Lock at Powerup	µs			500
b_sync[1,2]	Bit Sync Time	bits			2500
$t_{rxsetup}$	RX [0:3][0:9] Output Setup Time (Data Valid Before Clock)	ns	3.0		
t_{rxhold}	RX [0:3][0:9] Output Hold Time (Data Valid After Clock)	ns	1.5		
T_{duty}	RC [0:3][0] and RC [0:3][1] Duty Cycle	%	40		60
t_{A-B}	Rising Edge Time Difference between RBC0 and RBC1 (Half Rate)	ns	8.9		9.9
t_rxlat[3]	Receiver Latency	ns bits		22.4 28.0	

Notes:

1. This is the recovery time for input phase jumps, per the Fibre Channel Specification X3.230-1994 FC-PH Standard, Sec 5.3.
2. Tested using C_{PLL} = 0.1 µF.
3. The receiver latency, as shown in Figure 6, is defined as the time between receiving the first serial bit of a parallel data word (defined as the edge of the first serial bit) and the clocking out of that parallel word (defined by the rising edge of the receive byte clock, RC[0:1]).

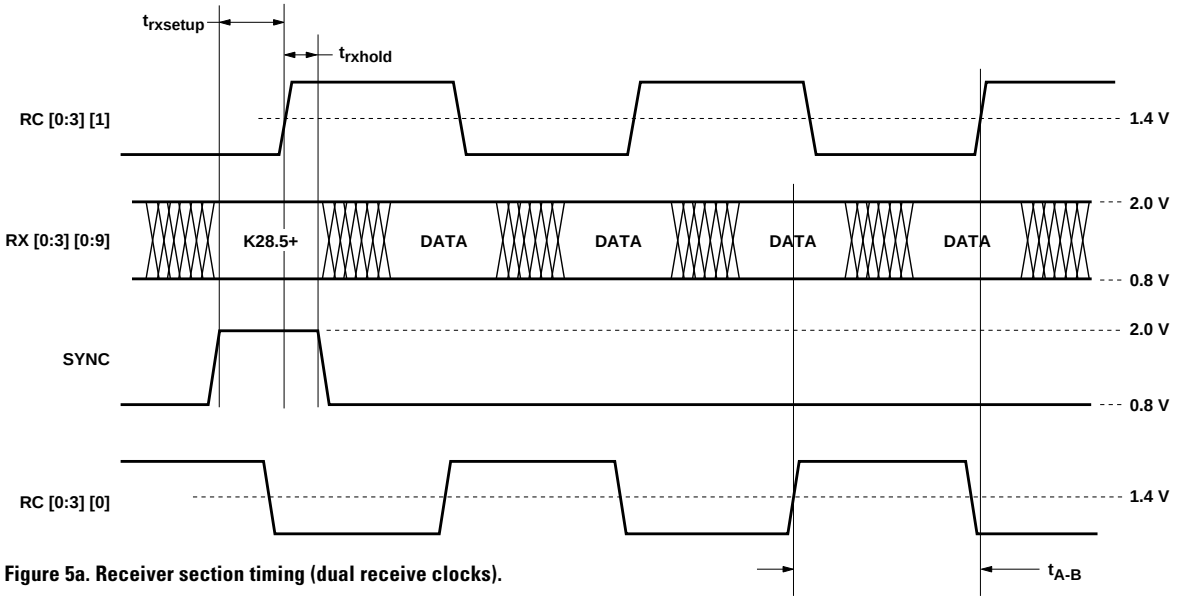


Figure 5a. Receiver section timing (dual receive clocks).

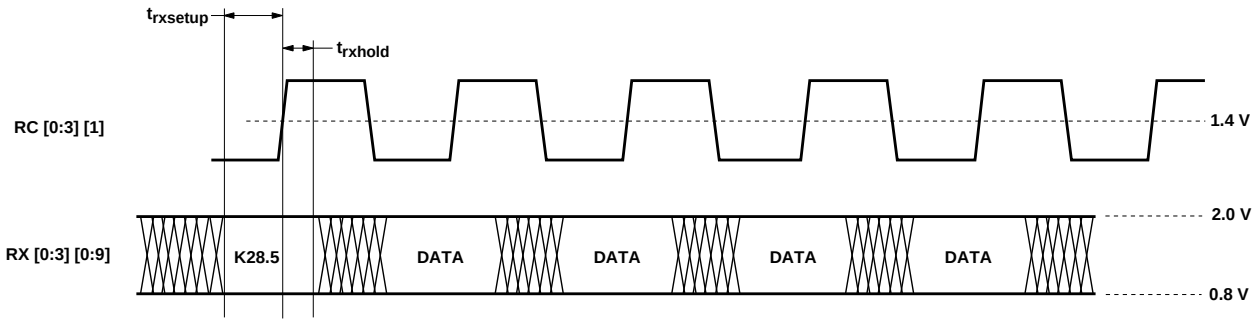


Figure 5b. Receiver section timing (single receive clock).

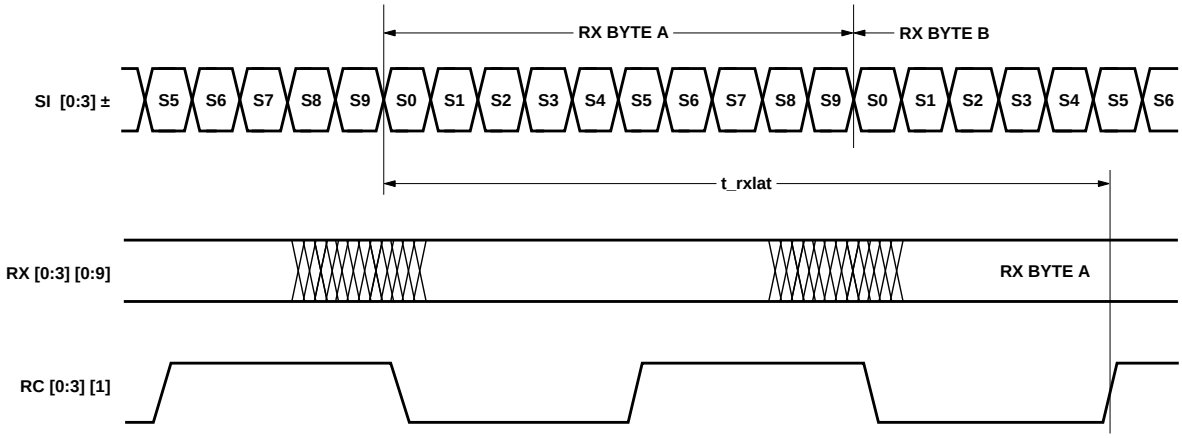


Figure 6. Receiver latency.

Absolute Maximum Ratings

T_A = 25°C, except as specified. Operation in excess of any one of these conditions may result in permanent damage to this device. Continuous operation at these minimum or maximum ratings is not recommended.

Symbol	Parameter	Units	Min.	Max.
V_{CC}	Supply Voltage	V	–0.5	4.0
$V_{IN,TTL}$	TTL Input Voltage	V	–0.7	V_{CC} + 2.8
V_{IN,HS_IN}	HS_IN Input Voltage (Differential)	V		2.2
$I_{O,TTL}$	TTL Output Sink / Source Current	mA		± 13
T_{stg}	Storage Temperature	°C	–65	+150
T_j	Junction Temperature	°C	0	+125
T_C	Case Temperature	°C	0	+95

Guaranteed Operating Rates

T = 0°C Ambient to +85°C Case, V_{CC} = 3.15 V to 3.45 V

Parallel Clock Rate (MHz)		Serial Baud Rate (MBaud)		
Min.	Max.	Min.	Max.	
124.0	126.0	1240	1260	Gigabit Ethernet
105.25	107.25	1052.5	1072.5	Fibre Channel

Transceiver Reference Clock Requirements

T = 0°C Ambient to +85°C Case, V_{CC} = 3.15 V to 3.45 V

Symbol	Parameter	Units	Min.	Typ.	Max.
f	Nominal Frequency (for Gigabit Ethernet Compliance)	MHz		125	
f	Nominal Frequency (for Fibre Channel Compliance)	MHz		106.25	
F_{tol}	Frequency Tolerance	ppm	–100		+100
Symm	Symmetry (Duty Cycle)	%	40		60

TTL I/O DC Electrical Specifications

T_A = 0°C Ambient to +85°C Case, V_{CC} = 3.15 V to 3.45 V

Symbol	Parameter	Units	Min.	Typ.	Max.
$V_{IH,TTL}$	TTL Input High Voltage Level, Guaranteed High Signal for All Inputs	V	2		5.5
$V_{IL,TTL}$	TTL Input Low Voltage Level, Guaranteed Low Signal for All Inputs	V	0		0.8
$V_{OH,TTL}$	TTL Output High Voltage Level, I_{OH} = –400 µA	V	2.2		V_{CC}
$V_{OL,TTL}$	TTL Output Low Voltage Level, I_{OL} = 1 mA	V	0		0.5
$I_{IH,TTL}$	Input High Current, V_{IN} = 2.4 V, V_{CC} = 3.45 V	µA			40
$I_{IL,TTL}$	Input Low Current, V_{IN} = 0.4 V, V_{CC} = 3.45 V	µA			–600
$I_{CC,TRx}$	Transceiver V_{CC} Supply Current, T_A = 25°C	mA		800	

AC Electrical Specifications (TRx)

T_A = 0°C Ambient to +85°C Case, V_{CC} = 3.15 V to 3.45 V

Symbol	Parameter	Units	Min.	Typ.	Max.
$t_{r,TCi}$	RFCT Rise Time, 0.8 to 2.0 Volts	ns	0.2		2.4
$t_{f,TCi}$	RFCT Fall Time, 2.0 to 0.8 Volts	ns	0.2		2.4
$t_{r,TTLin}$	Input TTL Rise Time, 0.8 to 2.0 Volts	ns		1.0	
$t_{f,TTLin}$	Input TTL Fall Time, 2.0 to 0.8 Volts	ns		1.0	
$t_{r,TTLout}$	Output TTL Rise Time, 0.8 to 2.0 Volts, 10 pF Load	ns		1.5	2.4
$t_{f,TTLout}$	Output TTL Fall Time, 2.0 to 0.8 Volts, 10 pF Load	ns		1.1	2.4
$t_{rs,\ HS\_OUT}$	HS_OUT Single-Ended SO [0:3]± Rise Time	ps		200	300
$t_{fs,\ HS\_OUT}$	HS_OUT Single-Ended SO [0:3]± Fall Time	ps		200	300
$t_{rd,\ HS\_OUT}$	HS_OUT Differential Rise Time	ps		200	300
$t_{fd,\ HS\_OUT}$	HS_OUT Differential Fall Time	ps		200	300
V_{IP,HS_IN}	HS_IN Input Peak-To-Peak Differential Voltage	mV	200	1200	2000
V_{OP,HS_OUT}[1]	HS_OUT Output Pk-Pk Diff. Voltage (Z0=50 Ohms, Fig.10)	mV	1000	1300	1800

Note:

1. Output Peak-to-Peak Differential Voltage specified as SO [0:3]+ minus SO [0:3]–. The output will be 25% higher when terminating into 75 Ω loads.

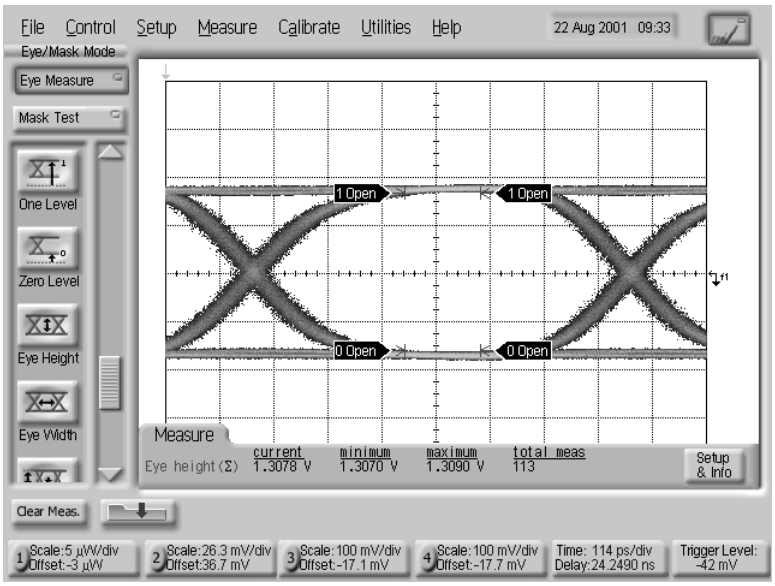


Figure 7a. Eye diagram of a high speed differential output for Gigabit Ethernet.

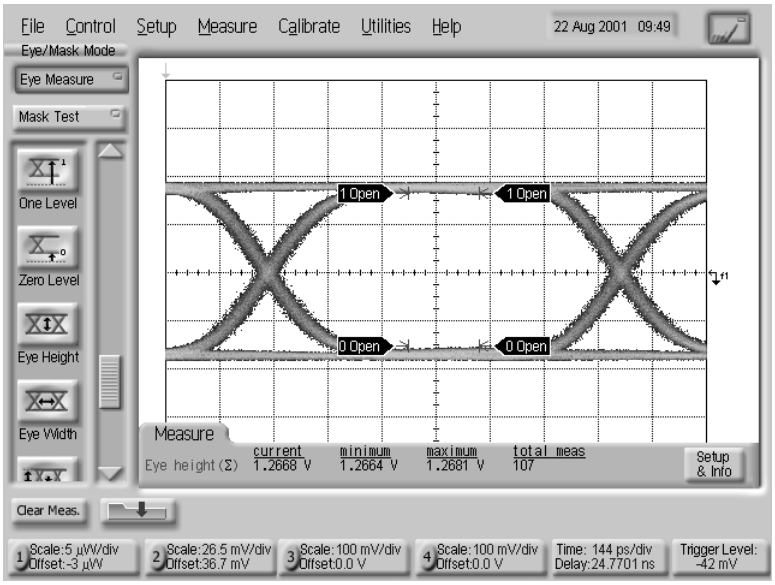


Figure 7b. Eye diagram of a high speed differential output for Fibre Channel.

Output Jitter Characteristics – Transmitter Section

T_A = 0°C Ambient to +85°C Case, V_{CC} = 3.15 V to 3.45 V

Symbol	Parameter	Units	Typ.
RJ[1]	Random Jitter at SO [0:3]±, the High Speed Electrical Data Port, specified as 1 sigma deviation of the 50% crossing point (RMS)	ps	11
DJ[1]	Deterministic Jitter at SO [0:3]±, the High Speed Electrical Data Port (pk-pk)	ps	36

Note:

1. Defined by Fibre Channel Specification X3.230-1994 FC-PH Standard, Annex A, Section A.4 and tested using measurement method shown in Figure 8.

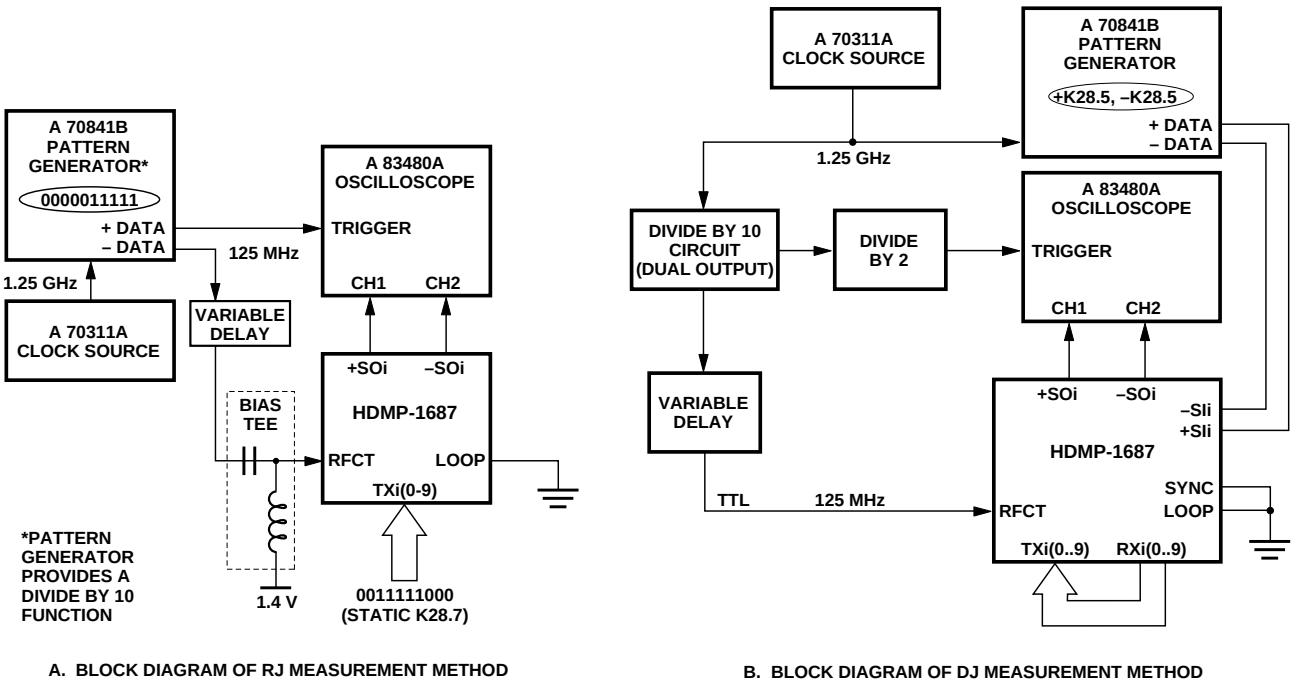


Figure 8. Transmitter jitter measurement method.

Thermal and Power Characteristics (TRx)

T = 0°C Ambient to 85°C Case, V_{CC} = 3.15 V to 3.45 V

Symbol	Parameter	Units	Typ.	Max.
$P_{D, TRx}$	Transceiver Power Dissipation, Outputs Connected per Recommended Bias Terminations with Idle Pattern	W	2.6	3.3
θ_{JA}[1]	Thermal Resistance: Junction to Ambient	°C/W	15.8	
θ_{JC}[2]	Thermal Resistance: Junction to Case	°C/W	2.5	
ψ_{JT}[3]	Thermal Characterization Parameter: Junction to Package Top	°C/W	1.1	

Notes:

1. θ_{JA} is measured in a still air environment at 25°C on a standard 3 x 3" FR4 PCB as specified in EIA/JESD 51-7.
2. θ_{JC} data relevant for packages used with external heat sink.
3. To determine the actual junction temperature in a given application, use the following: $T_J = T_T + (\psi_{JT} \times P_D)$, where T_T is the case temperature measured on the top center of the package and P_D is the power being dissipated.

I/O Type Definitions

I/O Type	Definition
I-TTL	Input TTL, floats high when left open
O-TTL	Output TTL
HS_OUT	50 Ω matched output driver. Will drive AC coupled 50 Ω loads. PECL Level Compatible (Figure 10).
HS_IN	PECL Level Compatible. Must be AC coupled (Figure 10).
C	External Circuit Node
S	Power Supply or Ground

Pin Input Capacitance (TRx)

Symbol	Parameter	Units	Typ.	Max.
C_{INPUT}	Input Capacitance on TTL Input Pins	pF	1.6	

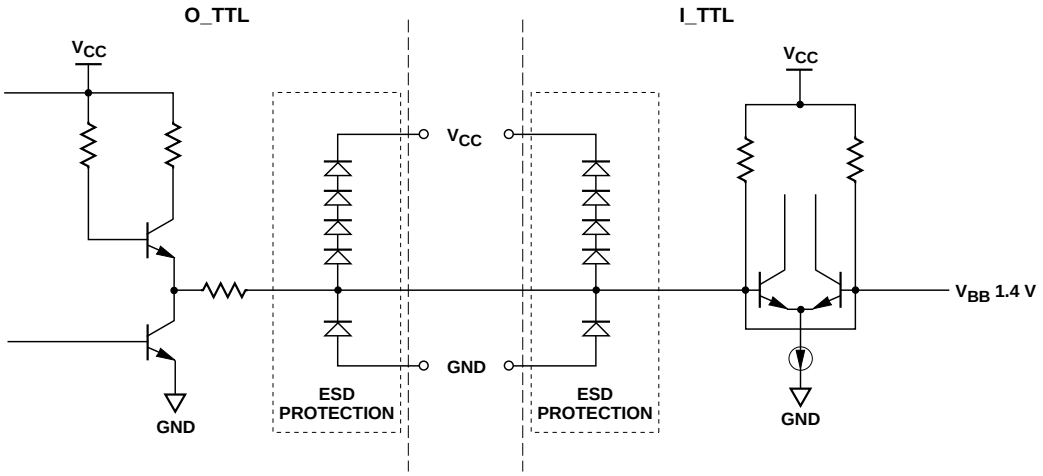
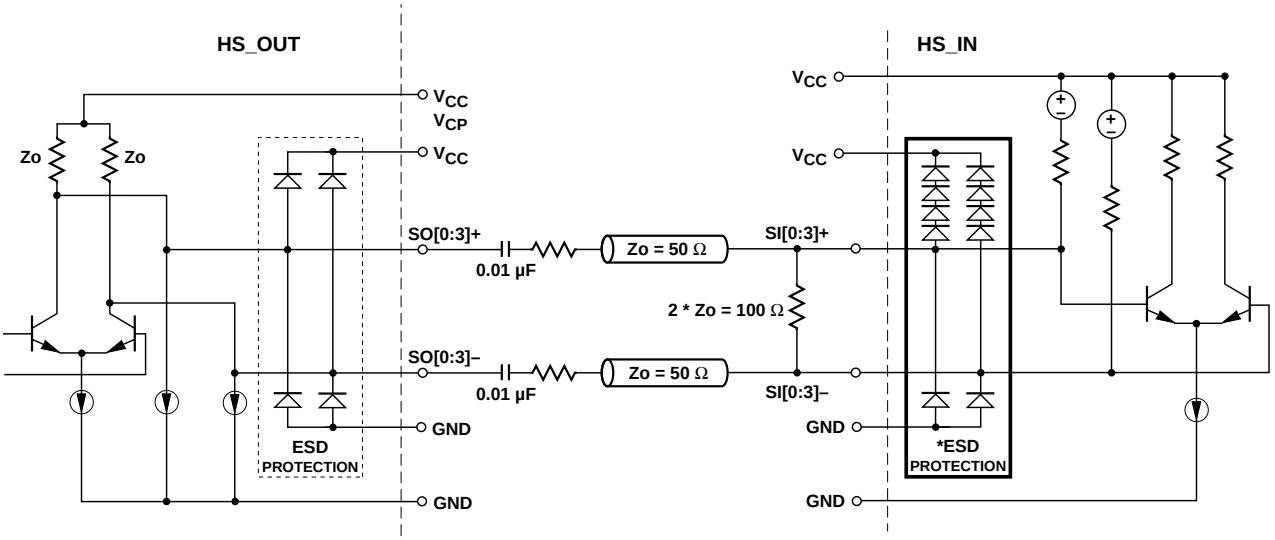


Figure 9. O-TTL and I-TTL simplified circuit schematic.



NOTES:
1. HS_IN INPUTS SHOULD NEVER BE CONNECTED TO GROUND AS PERMANENT DAMAGE TO THE DEVICE MAY RESULT.
2. CAPACITORS MAY BE PLACED AT THE SENDING END OR THE RECEIVING END.

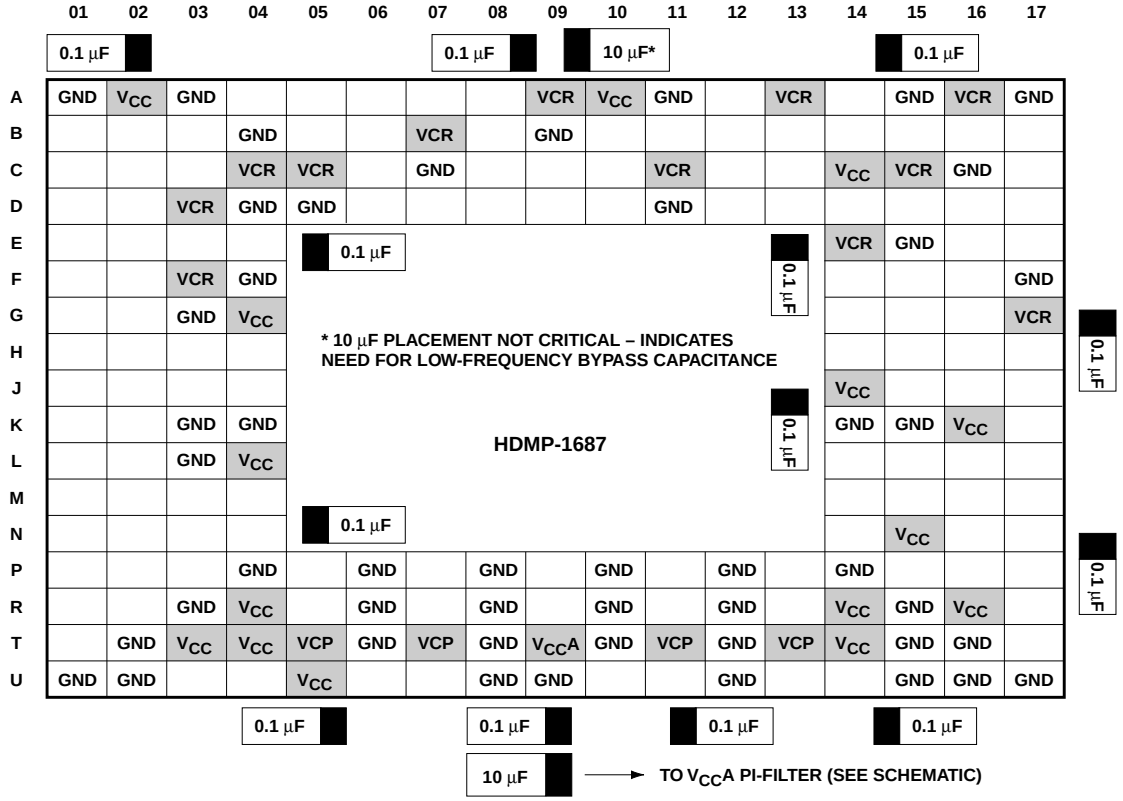
Figure 10. HS_OUT and HS_IN simplified circuit schematic.

	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17
A	GND	V_{CC}	GND	SYN1	RC10	RX10	RX14	RX16	VCR1	V_{CC}	GND	RX21	VCR2	RX28	GND	VCR2	GND
B	RX07	RX08	RX09	GND	RC11	RX11	VCR1	RX17	GND	SYN2	RX20	RX22	RX25	RX29	SYN3	RC30	RC31
C	RX04	RX05	RX06	VCR0	VCR1	RX12	GND	RX18	N/C	RC20	VCR2	RX23	RX26	V_{CC}	VCR3	GND	RX30
D	RX00	RX01	VCR0	GND	GND	RX13	RX15	RX19	N/C	RC21	GND	RX24	RX27	RX31	RX32	RX33	RX34
E	RC00	RC01	RX02	RX03										VCR3	GND	RX35	RX36
F	N/C	SYN0	VCR0	GND										RX37	RX38	RX39	GND
G	TX18	TX19	GND	V_{CC}				GND						TX22	TX21	TX20	VCR3
H	TX14	TX15	TX16	TX17				GNDA						TX26	TX25	TX24	TX23
J	TX10	TX11	TX12	TX13				V_{CRX}						V_{CC}	TX29	TX28	TX27
K	N/C	N/C	GND	GND				V_{CC}						GND	GND	V_{CC}	N/C
L	TX08	TX09	GND	V_{CC}				V_{CCA}						TX33	TX32	TX31	TX30
M	TX04	TX05	TX06	TX07				VCPX						TX37	TX36	TX35	TX34
N	TX00	TX01	TX02	TX03										LOOP	V_{CC}	TX39	TX38
P	N/C	N/C	N/C	GND	SO0–	GND	SO1–	GND	CAP0	GND	SO2+	GND	SO3+	GND	N/C	N/C	N/C
R	RFCT	N/C	GND	V_{CC}	SO0+	GND	SO1+	GNDA	CAP1	GND	SO2–	GND	SO3–	V_{CC}	GND	V_{CC}	SYNC
T	RCM0*	GND	V_{CC}	V_{CC}	VCP0	GND	VCP1	GND	V_{CCA}	GND	VCP2	GND	VCP3	V_{CC}	GND	GND	N/C
U	GND	GND	SIO–	SIO+	V_{CC}	SI1–	SI1+	GND	GND	SI2–	SI2+	GND	SI3–	SI3+	GND	GND	GND

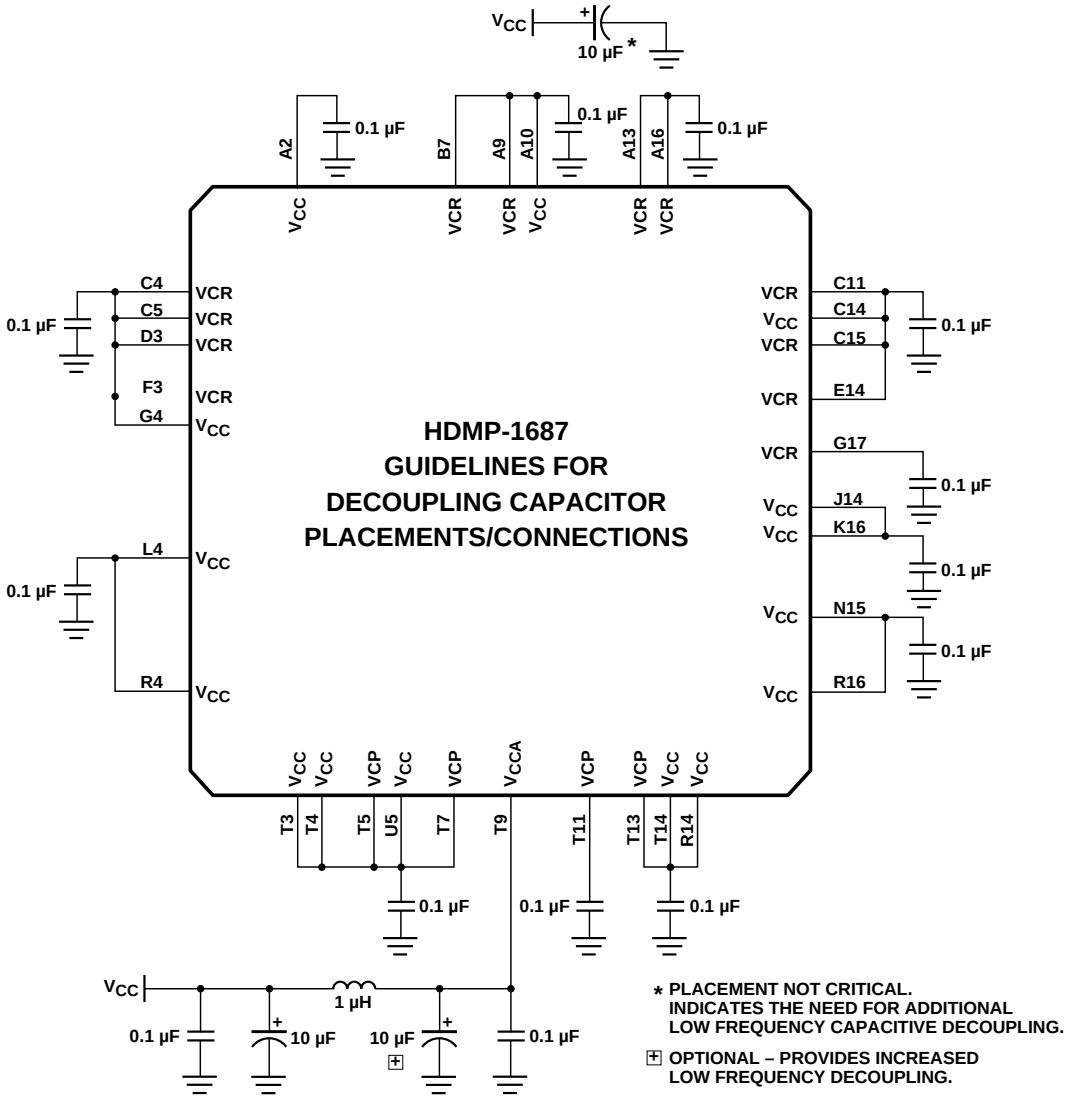
* Previously RFC1 changed to RFCT for data sheet consistency.

Figure 11. Pinout of HDMP-1687 (top view).

Filtering Schematic



Guidelines for Decoupling Capacitor Placements/Connections



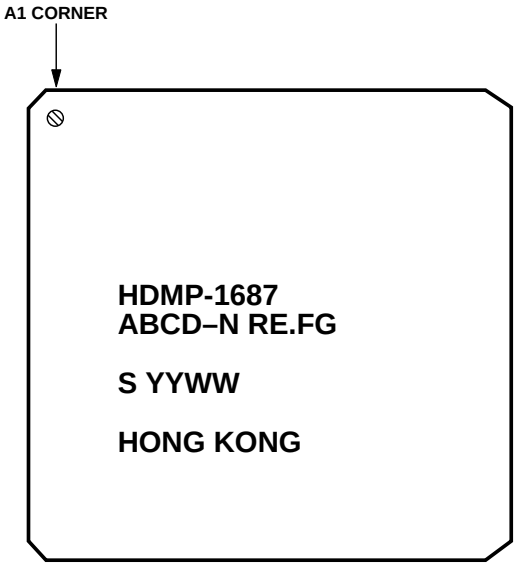
TRx I/O Definition

Name	Type	Signal
SI [0:3]+ SI [0:3]–	HS_IN	**Serial Data Inputs:** High-speed inputs. Serial data is accepted from the SI [0:3]± inputs when LOOP is low.
SO [0:3]+ SO [0:3]–	HS_ OUT	**Serial Data Outputs:** High speed outputs. These lines are active when LOOP is set low. When LOOP is set high, these outputs are held static at logic 1.
SYNC	I-TTL	**Enable Byte Sync Input:** When high, turns on the internal byte sync functions to allow clock synchronization to a comma character of positive disparity (0011111XXX). When the line is low, the function is disabled and will not reset registers and clocks, or strobe the SYN [0:3] lines.
SYN [0:3]	O-TTL	**Byte Sync Outputs:** Active high outputs. Used to indicate detection of a comma character of positive disparity (0011111XXX) when SYNC is enabled.
N/C		These pins need to be left open. Do not apply voltage on this pin.
LOOP	I-TTL	**Loopback Enable Input:** When set high, the high speed serial signal is internally wrapped from the transmitter's serial loopback outputs back to the receiver's loopback inputs. Also when in loopback mode, the SO [0:3]± outputs are held static at logic 1. When set low, SO [0:3]± outputs and SI [0:3]± inputs are active.
RCM0	I-TTL	**Receivers Clocking Mode Definition Pins:** These pins define how received parallel data are driven as follows: RCM0 — Receive Clock Mode 0 — half speed dual clocks 1 — full speed single clocks
RC [0:3] [0:1]	O-TTL	**Receiver Byte Clocks:** The receiver sections drive 125 MHz receive byte clocks RC [0:3] [1]. Alternatively, they may drive half speed clocks RC [0:3] [0:1]. See RCM0 definition.
RFCT	I-TTL	**Reference Clock and Transmit Byte Clock:** A 125 MHz clock supplied by the host system. The transmitter sections accept this signal as the frequency reference clock. It is multiplied by 10 to generate the serial bit clock and other internal clocks. The transmit sections use this clock as the transmit byte clock for transmitting parallel data at TX [0:3] [0:9].
RX [0:3] [0] RX [0:3] [1] RX [0:3] [2] RX [0:3] [3] RX [0:3] [4] RX [0:3] [5] RX [0:3] [6] RX [0:3] [7] RX [0:3] [8] RX [0:3] [9]	O-TTL	**Data Outputs:** Four 10 bit data bytes. RX [0:3] [0] are the first bits received.
CAP0 CAP1	C	**Loop Filter Capacitor:** A loop filter capacitor for the internal PLLs must be connected across the CAP0 and CAP1 pins. (typical value = 0.1µF).

TRx I/O Definition, continued

Name	Type	Signal
TX [0:3] [0] TX [0:3] [1] TX [0:3] [2] TX [0:3] [3] TX [0:3] [4] TX [0:3] [5] TX [0:3] [6] TX [0:3] [7] TX [0:3] [8] TX [0:3] [9]	I-TTL	**Data Inputs:** Four 10 bit, 8B/10B encoded data bytes. TX [0:3] [0] are the first bits transmitted.
V_{CC}	S	**Power Supply:** Nominally 3.3 volts. Used for logic and TTL inputs.
V_{CCA}	S	**Analog Power Supply:** Nominally 3.3 volts. Used to provide a clean supply line for the PLLs and high speed analog cells.
VCR3-0	S	**Rx TTL Output Power Supply:** Nominally 3.3 volts. Used for all TTL receiver output buffer cells.
VCP3-0	S	**High Speed Output Supply:** Nominally 3.3 volts. Used only for the last stage of the high speed transmitter output cells (HS_OUT) as shown in Figure 10. Due to high current transitions, this Vcc should be well bypassed to a ground plane.
GND	S	**Ground:** Nominally 0 volts. All GND pads on the chip are connected to one ground slug in the package which then distributes these to GND balls.
GNDA	S	**Analog Ground:** Normally 0 volts. All GND pads on the chip are connected to one ground slug in the package, which then distributes these to GND balls.

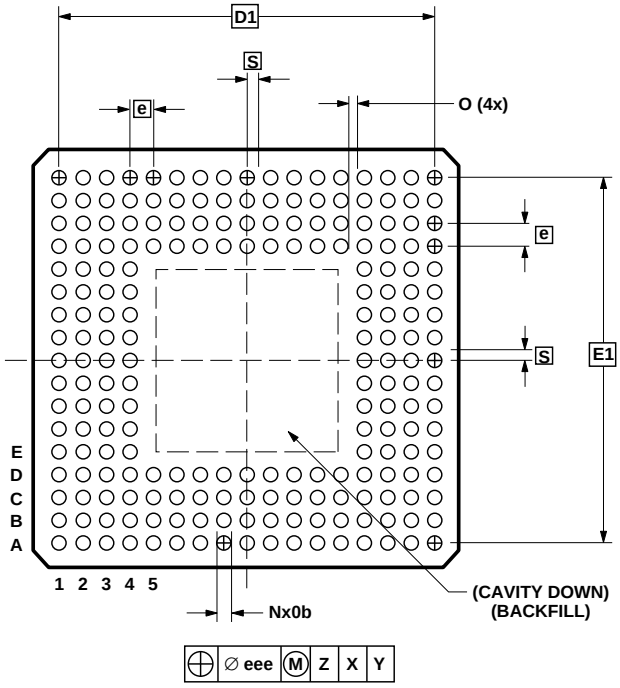
208 Ball 23 mm x 23 mm TBGA Package Drawing

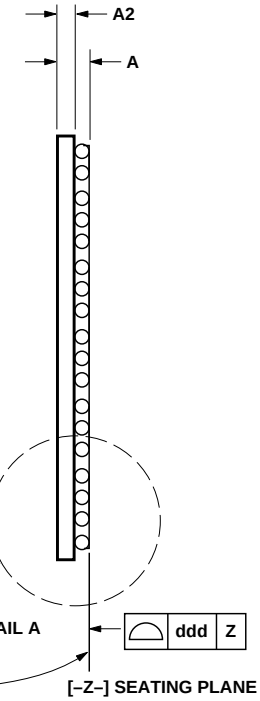


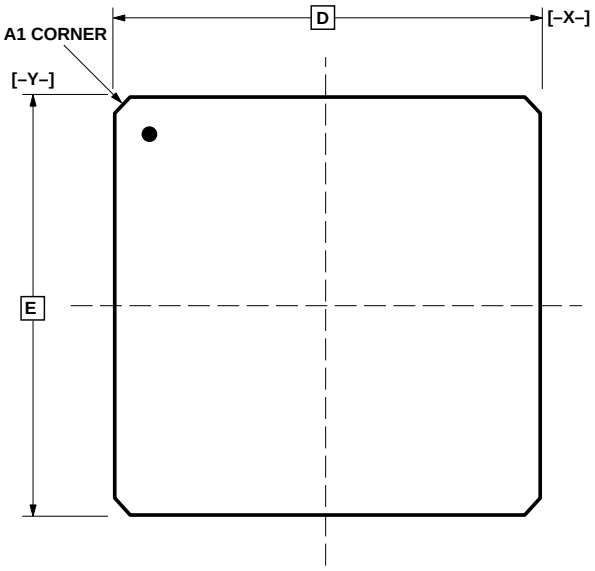
TOP VIEW

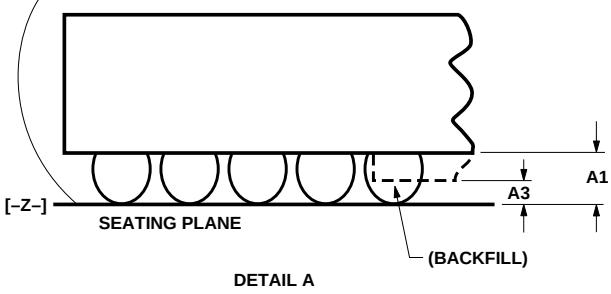
Procedure to follow for soldering the HDMP-1687, 208-ball TBGA package:
IR or Convective Reflow per IPC/JEDEC J-STD-020A standard for BGA IR Reflow.

Package Drawing









DETAIL A

DIMENSIONS IN MILLIMETERS

SYMBOL	MIN.	NOM.	MAX.
A	1.35	1.50	1.65
A1	0.60	0.65	0.70
A2	0.85	0.90	0.95
A3	0.15		
D		23.00 ± 0.20	
D1		20.32 BSC	
E		23.00 ± 0.20	
E1		20.32 BSC	
MD/ME		17	
N		208	
N1		4	
O	0.60		
b	0.60	0.75	0.90
e		1.27 ± 0.10	

TOLERANCE OF FORM AND POSITION

SYMBOL	MIN.	NOM.	MAX.
ddd			0.15
eee			0.30

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Obsoletes 5988-1305EN
5988-4080EN

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