DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4508B
MSI
Dual 4-bit latch

Product specification
File under Integrated Circuits, IC04

January 1995

Philips Semiconductors

PHILIPS

DESCRIPTION

The HEF4508B is a dual 4-bit latch, which consists of two identical independent 4-bit latches with separate strobe (ST), master reset (MR), output-enable input ($\overline{EO}$) and 3-state outputs (O).

With the ST input in the HIGH state, the data on the D inputs appear at the corresponding outputs provided $\overline{EO}$ is LOW. Changing the ST input to the LOW state locks the data into the latch. A HIGH on the reset line forces the outputs to a LOW level regardless of the state of the ST input. The 3-state outputs are controlled by the output-enable input. A HIGH on $\overline{EO}$ causes the outputs to assume a high impedance OFF-state regardless of other input conditions. This allows the outputs to interface directly with bus orientated systems. When $\overline{EO}$ is LOW the contents of the latches are available at the outputs.

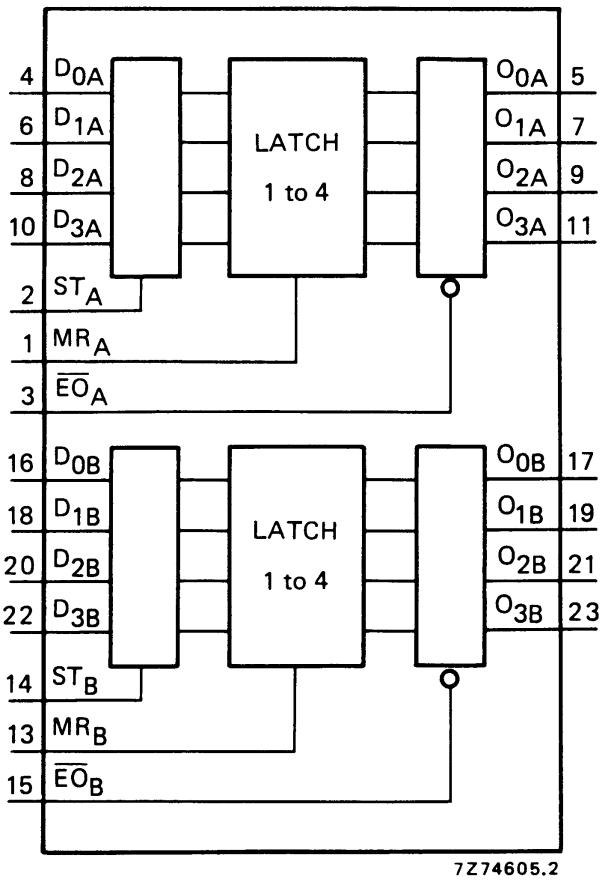

Fig.1 Functional diagram.

FAMILY DATA, I_{DD} LIMITS category MSI

See Family Specifications

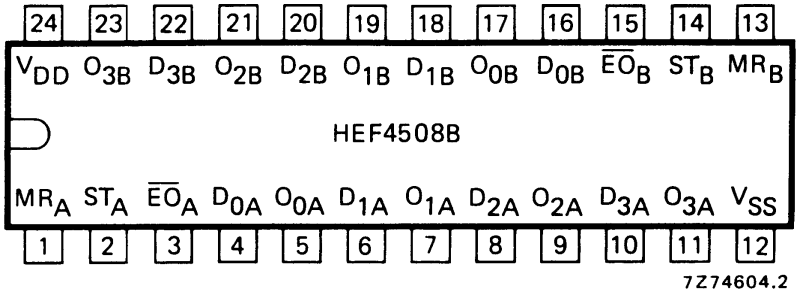

Fig.2 Pinning diagram.

HEF4508BP(N): 24-lead DIL; plastic (SOT101-1)
HEF4508BD(F): 24-lead DIL; ceramic (cerdip) (SOT94)
HEF4508BT(D): 24-lead SO; plastic (SOT137-1)

( ): Package Designator North America

PINNING

D_{0A} to D_{3A}, D_{0B} to D_{3B}	data inputs
ST_A , ST_B	strobe inputs
MR_A, MR_B	master reset inputs
$\overline{EO}_A$, $\overline{EO}_B$	output enable inputs
O_{0A} to O_{3A}, O_{0B} to O_{3B}	3-state outputs

FUNCTION TABLE

INPUTS				OUTPUT
MR	**ST**	$\overline{\textbf{EO}}$	$\mathbf{D_n}$	$\mathbf{O_n}$
L	H	L	H	H
L	H	L	L	L
L	L	L	X	latched
H	X	L	X	L
X	X	H	X	Z

Notes

1. H = HIGH state (the more positive voltage)
   L = LOW state (the less positive voltage)
   X = state is immaterial
   Z = high impedance OFF state

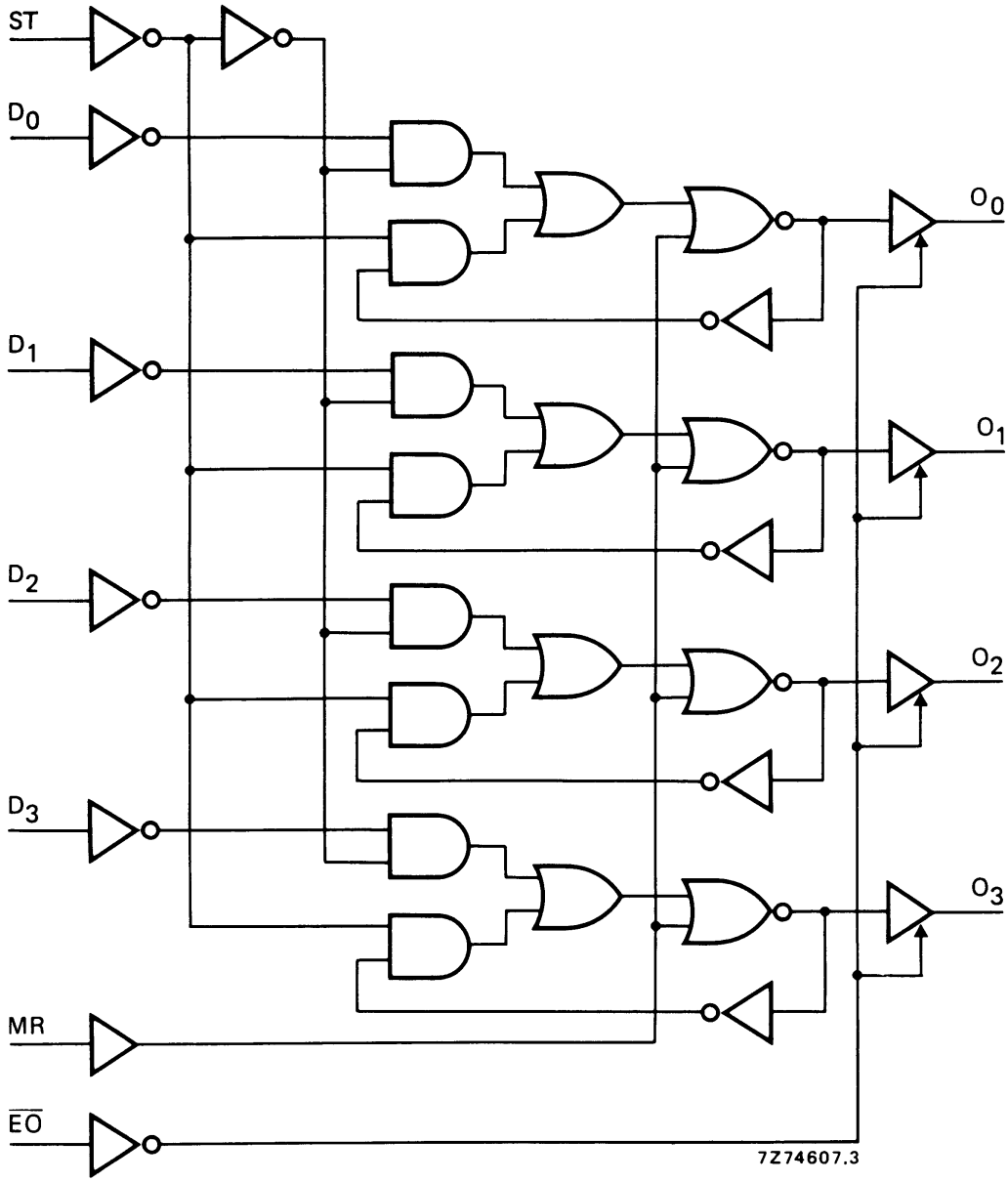

Fig.3 Logic diagram (one 4-bit latch).

AC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns; see also waveforms Fig.4.

	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.		TYPICAL EXTRAPOLATION FORMULA
Propagation delays							
ST → O_n	5			115	230	ns	88 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		50	100	ns	39 ns + (0,23 ns/pF) C_L
	15			35	70	ns	27 ns + (0,16 ns/pF) C_L
	5			115	230	ns	88 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		50	100	ns	39 ns + (0,23 ns/pF) C_L
	15			35	70	ns	27 ns + (0,16 ns/pF) C_L
D_n → O_n	5			95	190	ns	68 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		40	80	ns	29 ns + (0,23 ns/pF) C_L
	15			30	60	ns	22 ns + (0,16 ns/pF) C_L
	5			95	190	ns	68 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		40	80	ns	29 ns + (0,23 ns/pF) C_L
	15			30	60	ns	22 ns + (0,16 ns/pF) C_L
MR → O_n	5			100	200	ns	73 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		40	80	ns	29 ns + (0,23 ns/pF) C_L
	15			30	60	ns	22 ns + (0,16 ns/pF) C_L
Output transition times	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
3-state propagation delays							
Output enable times							
$\overline{EO}$ → O_n	5			45	90	ns	
HIGH	10	t_{PZH}		20	40	ns	
	15			18	36	ns	
	5			45	90	ns	
LOW	10	t_{PZL}		20	40	ns	
	15			18	36	ns	
Output disable times							
$\overline{EO}$ → O_n	5			35	70	ns	
HIGH	10	t_{PHZ}		20	40	ns	
	15			18	36	ns	
	5			45	90	ns	
LOW	10	t_{PLZ}		20	40	ns	
	15			18	36	ns	

AC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns

	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.		
Minimum ST	5			50	25		ns	
pulse width; HIGH	10	t_{WSTH}		30	15		ns	
	15			20	10		ns	
Minimum MR pulse	5			40	20		ns	
width; HIGH	10	t_{WMRH}		24	12		ns	
	15			20	10		ns	
Recovery time	5			20	0		ns	
for MR	10	t_{RMR}		20	0		ns	see also waveforms Fig.4
	15			15	0		ns	
Set-up times	5			35	10		ns	
$D_n \rightarrow$ ST	10	t_{su}		25	5		ns	
	15			20	0		ns	
Hold times	5			20	0		ns	
$D_n \rightarrow$ ST	10	t_{hold}		20	0		ns	
	15			15	0		ns	

	V_{DD} V	TYPICAL FORMULA FOR P (μW)	
Dynamic power	5	$2\,000\ f_i + \sum (f_o C_L) \times V_{DD}^2$	where
dissipation per	10	$9\,000\ f_i + \sum (f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz)
package (P)	15	$25\,000\ f_i + \sum (f_o C_L) \times V_{DD}^2$	f_o = output freq. (MHz)
			C_L = load capacitance (pF)
			$\sum (f_o C_L)$ = sum of outputs
			V_{DD} = supply voltage (V)

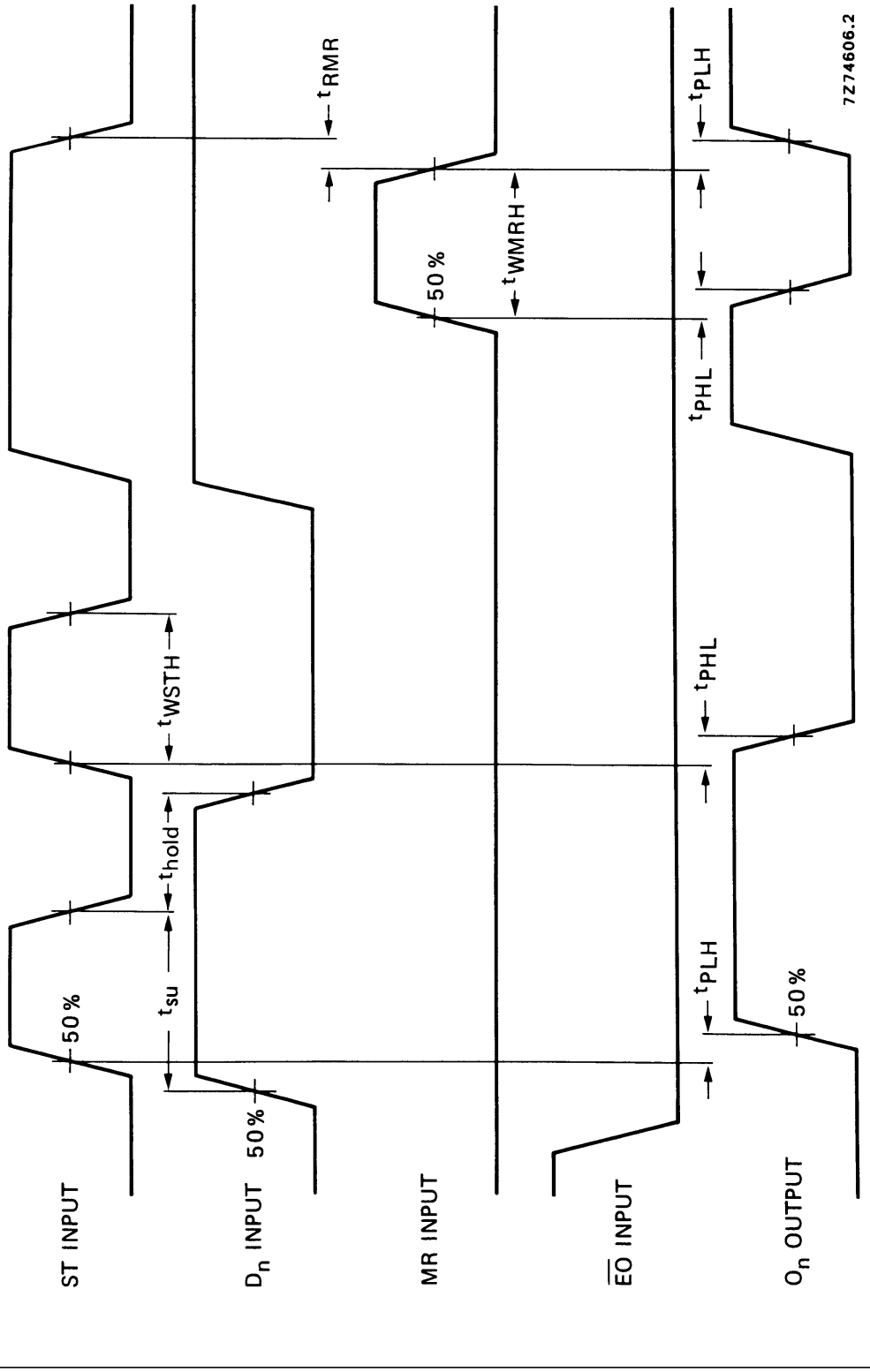

Fig.4 Waveforms showing minimum ST and MR pulse widths, set-up and hold times for D_n to ST, recovery time for MR and propagation delays from ST to O_n, to D_n to O_n and MR to O_n.

APPLICATION INFORMATION

Some examples of application for the HEF4508B are:

- Buffer storage
- Holding registers
- Data storage and multiplexing

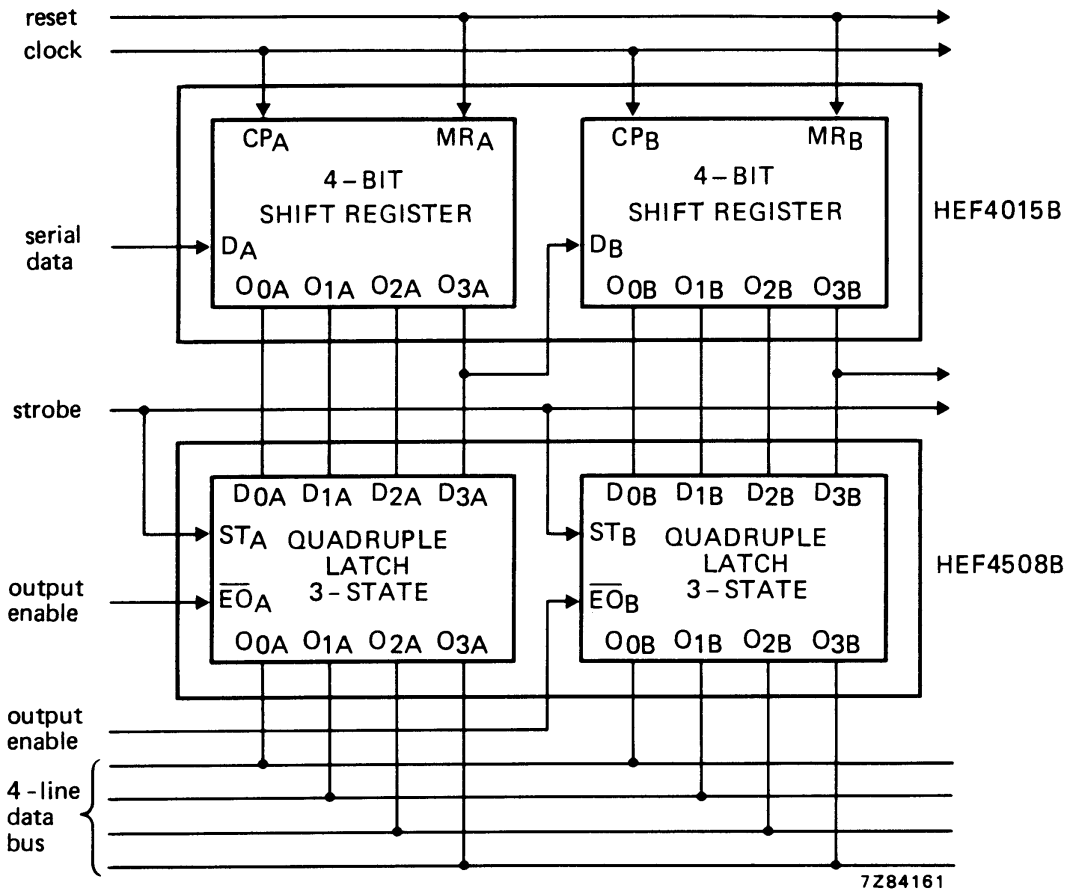

Fig.5 Example of a bus register using HEF4508B and HEF4015B.

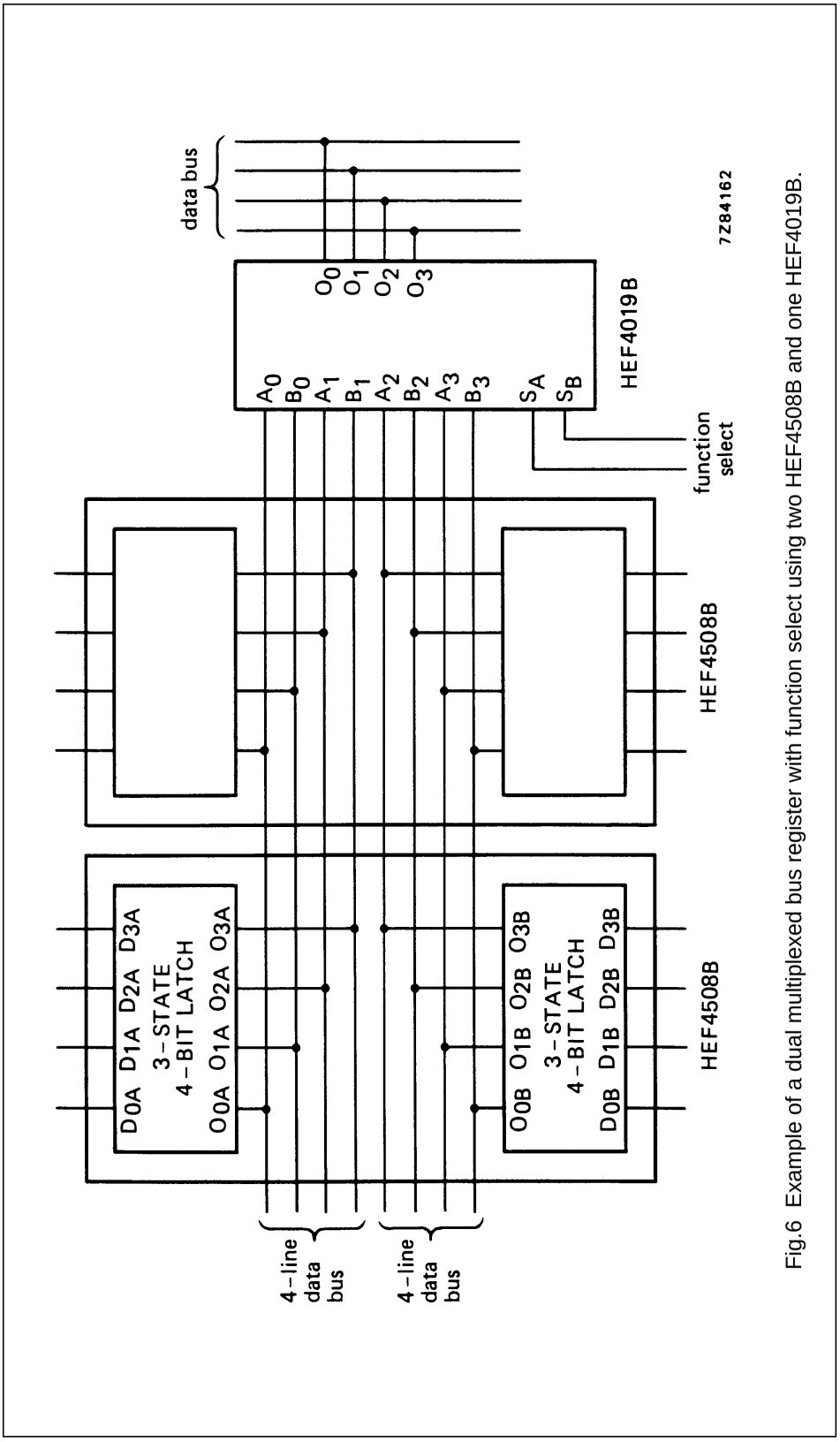

Fig.6 Example of a dual multiplexed bus register with function select using two HEF4508B and one HEF4019B.

FUNCTION SELECT

S_A	S_B	FUNCTION
L	L	inhibit (all L)
H	L	select A bus
L	H	select B bus
H	H	$A_1 + B_1$

littlediode
COMPONENTS FOR ALL

Littlediode supplies new, hard to find or obsolete electronic components and semiconductors all over the world.

With over two million different components listed you are sure to find the part you need.

Feel free to visit us today at our online store:

LittleDiode.com

Looking forward to providing you with the best possible service.