

DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4521B

MSI

24-stage frequency divider and oscillator

Product specification
File under Integrated Circuits, IC04

January 1995

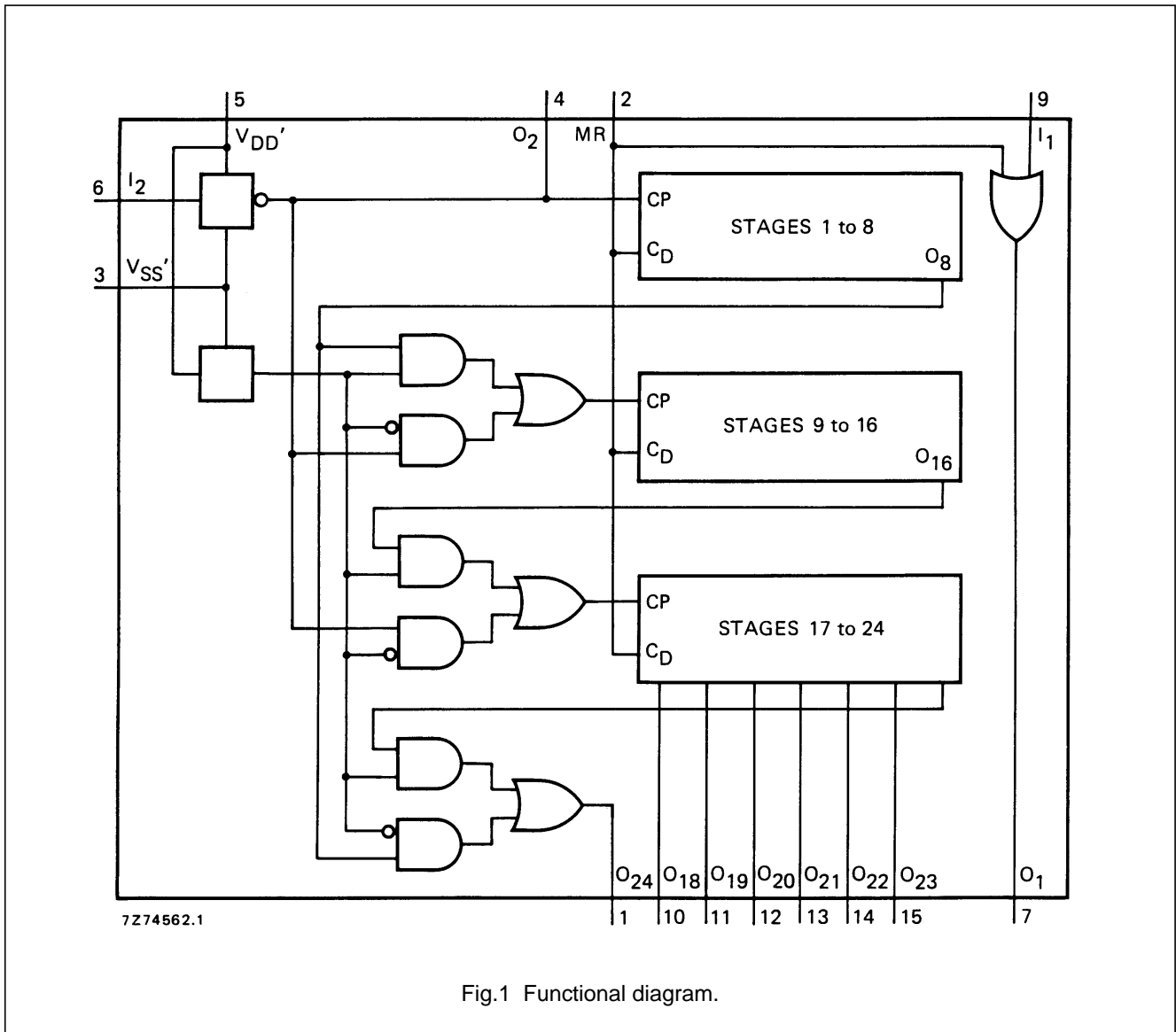
24-stage frequency divider and oscillator

HEF4521B MSI

DESCRIPTION

The HEF4521B consists of a chain of 24 toggle flip-flops with an overriding asynchronous master reset input (MR), and an input circuit that allows three modes of operation. The single inverting stage (I_2/O_2) will function as a crystal oscillator, or in combination with I_1 as an RC oscillator, or as an input buffer for an external oscillator. Low-power

operation as a crystal oscillator is enabled by connecting external resistors to pins 3 (V_{SS}') and 5 (V_{DD}'). Each flip-flop divides the frequency of the previous flip-flop by two, consequently the HEF4521B will count up to $2^{24} = 16777216$. The counting advances on the HIGH to LOW transition of the clock (I_2). The outputs of the last seven stages are available for additional flexibility.

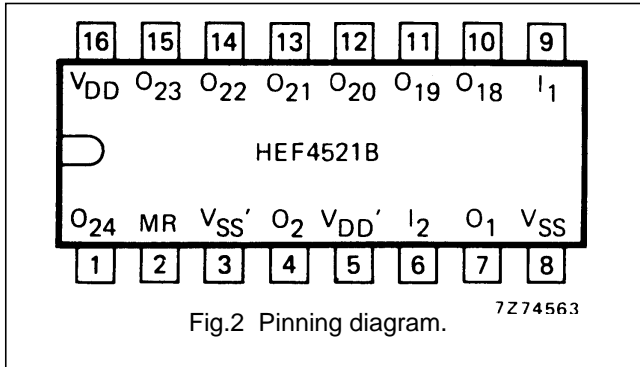


FAMILY DATA, I_{DD} LIMITS category MSI

See Family Specifications

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COUNT CAPACITY

OUTPUT	COUNT CAPACITY
O ₁₈	2 ¹⁸ = 262 144
O ₁₉	2 ¹⁹ = 524 288
O ₂₀	2 ²⁰ = 1 048 576
O ₂₁	2 ²¹ = 2 097 152
O ₂₂	2 ²² = 4 194 304
O ₂₃	2 ²³ = 8 388 608
O ₂₄	2 ²⁴ = 16 777 216

- HEF4521BP(N): 16-lead DIL; plastic (SOT38-1)
- HEF4521BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
- HEF4521BT(D): 16-lead SO; plastic (SOT109-1)
- (): Package Designator North America

FUNCTIONAL TEST SEQUENCE

INPUTS		CONTROL TERMINALS			OUTPUTS	REMARKS
MR	I ₂	O ₂	V _{SS} '	V _{DD} '	O ₁₈ to O ₂₄	
H	L	L	V _{DD}	V _{SS}	L	counter is in three 8-stage sections in parallel mode; I ₂ and O ₂ are interconnected (O ₂ is now input); counter is reset by MR
L			V _{DD}	V _{SS}	H	255 pulses are clocked into I ₂ , O ₂ (the counter advances on the LOW to HIGH transition)
L	L	L	V _{SS}	V _{SS}	H	V _{SS} ' is connected to V _{SS}
L	H	L	V _{SS}	V _{SS}	H	the input I ₂ is made HIGH
L	H	L	V _{SS}	V _{DD}	H	V _{DD} ' is connected to V _{DD} ; O ₂ is now made floating and becomes an output; the device is now in the 2 ²⁴ mode
L			V _{SS}	V _{DD}	L	counter ripples from an all HIGH state to an all LOW state

A test function has been included for the reduction of the test time required to exercise all 24 counter stages. This test function divides the counter into three 8-stage sections by connecting V_{SS}' to V_{DD} and V_{DD}' to V_{SS}. Via I₂ (connected to O₂) 255 counts are loaded into each of the 8-stage sections in parallel. All flip-flops are now at a HIGH state.

The counter is now returned to the normal 24-stage in series configuration by connecting V_{SS}' to V_{SS} and V_{DD}' to V_{DD}. One more pulse is entered into input I₂, which will cause the counter to ripple from an all HIGH state to an all LOW state.

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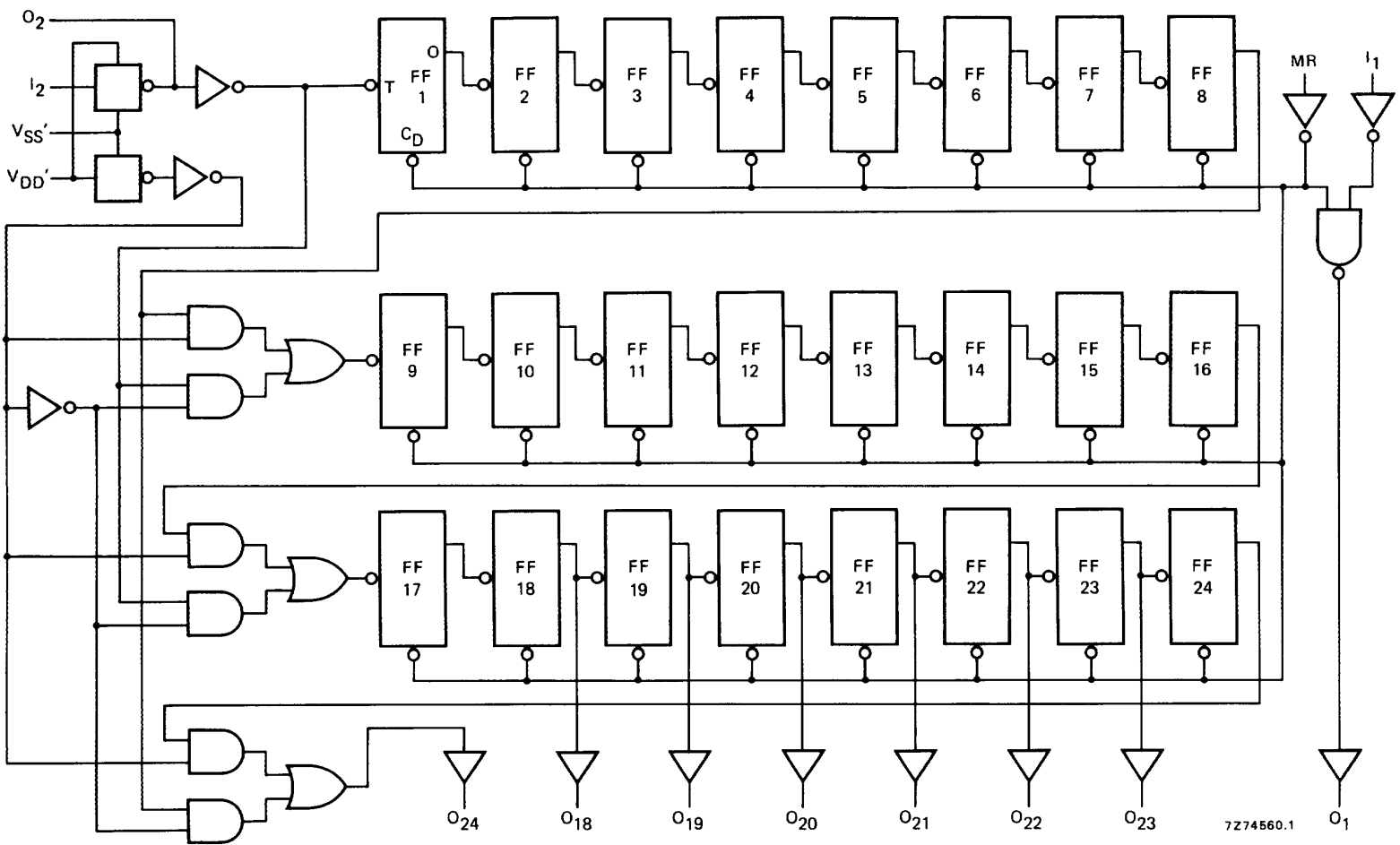


Fig.3 Logic diagram; for schematic diagram of clock circuit see Fig.4.

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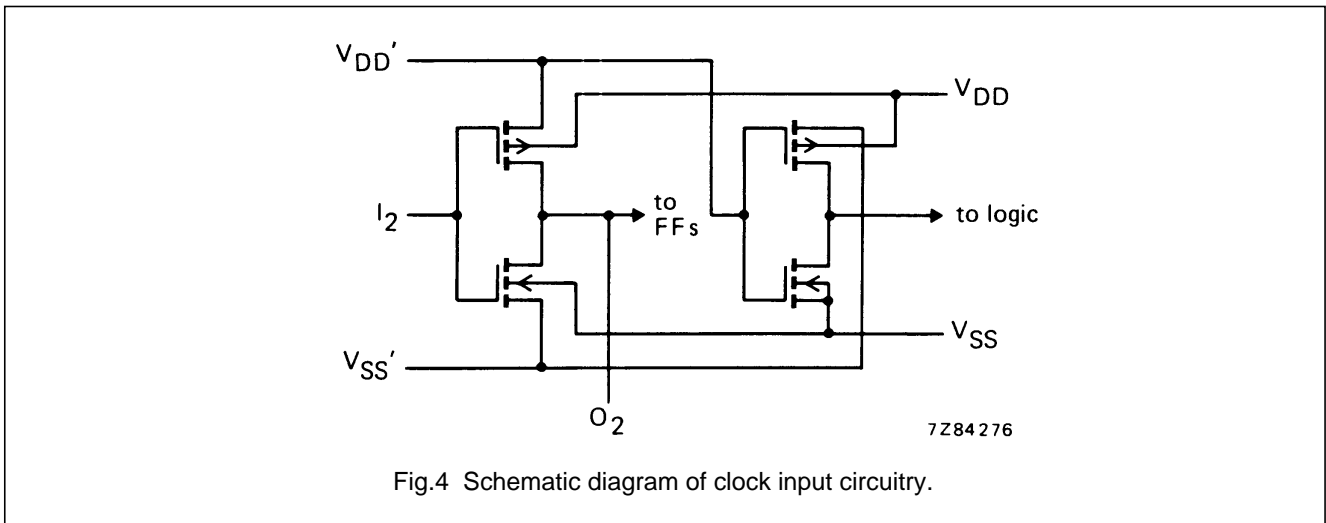


Fig.4 Schematic diagram of clock input circuitry.

AC CHARACTERISTICS

$V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^\circ\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA	
Propagation delays $I_2 \rightarrow O_{18}$ HIGH to LOW	5	t_{PHL}		950	1900	ns	923 ns + (0,55 ns/pF) C_L
	10			350	700	ns	339 ns + (0,23 ns/pF) C_L
	15			220	440	ns	212 ns + (0,16 ns/pF) C_L
LOW to HIGH	5	t_{PLH}		950	1900	ns	923 ns + (0,55 ns/pF) C_L
	10			350	700	ns	339 ns + (0,23 ns/pF) C_L
	15			220	440	ns	212 ns + (0,16 ns/pF) C_L
$O_n \rightarrow O_{n+1}$ HIGH to LOW	5	t_{PHL}		40	80	ns	13 ns + (0,55 ns/pF) C_L
	10			15	30	ns	4 ns + (0,23 ns/pF) C_L
	15			10	20	ns	2 ns + (0,16 ns/pF) C_L
LOW to HIGH	5	t_{PLH}		40	80	ns	13 ns + (0,55 ns/pF) C_L
	10			15	30	ns	4 ns + (0,23 ns/pF) C_L
	15			10	20	ns	2 ns + (0,16 ns/pF) C_L
$MR \rightarrow O_n$ HIGH to LOW	5	t_{PHL}		120	240	ns	93 ns + (0,55 ns/pF) C_L
	10			55	110	ns	44 ns + (0,23 ns/pF) C_L
	15			40	80	ns	32 ns + (0,16 ns/pF) C_L
$I_1 \rightarrow O_1$ HIGH to LOW	5	t_{PHL}		90	180	ns	63 ns + (0,55 ns/pF) C_L
	10			35	70	ns	24 ns + (0,23 ns/pF) C_L
	15			25	50	ns	17 ns + (0,16 ns/pF) C_L
LOW to HIGH	5	t_{PLH}		60	120	ns	33 ns + (0,55 ns/pF) C_L
	10			30	60	ns	19 ns + (0,23 ns/pF) C_L
	15			20	40	ns	12 ns + (0,16 ns/pF) C_L

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	V _{DD} V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA	
Output transition times HIGH to LOW	5	t _{THL}		60	120	ns	10 ns + (1,0 ns/pF) C _L
	10		30	60	ns	9 ns + (0,42 ns/pF) C _L	
	15		20	40	ns	6 ns + (0,28 ns/pF) C _L	
LOW to HIGH	5	t _{TLH}		60	120	ns	10 ns + (1,0 ns/pF) C _L
	10		30	60	ns	9 ns + (0,42 ns/pF) C _L	
	15		20	40	ns	6 ns + (0,28 ns/pF) C _L	

AC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns

	V _{DD} V	SYMBOL	MIN.	TYP.	MAX.	
Minimum I ₂ pulse width; HIGH	5	t _{WI2H}	80	40		ns
	10		40	20		ns
	15		30	15		ns
Minimum MR pulse width; HIGH	5	t _{WMRH}	70	35		ns
	10		40	20		ns
	15		30	15		ns
Recovery time for MR	5	t _{RMR}	20	-10		ns
	10		15	-5		ns
	15		15	0		ns
Maximum clock pulse frequency	5	f _{max}	6	12		MHz
	10		12	25		MHz
	15		17	35		MHz

see also waveforms
Fig.5

	V _{DD} V	TYPICAL FORMULA FOR P (μW)	
Dynamic power dissipation per package (P)	5	1 200 f _i + ∑ (f _o C _L) × V _{DD} ²	where f _i = input freq. (MHz) f _o = output freq. (MHz) C _L = load capacitance (pF) ∑ (f _o C _L) = sum of outputs V _{DD} = supply voltage (V)
	10	5 100 f _i + ∑ (f _o C _L) × V _{DD} ²	
	15	13 050 f _i + ∑ (f _o C _L) × V _{DD} ²	

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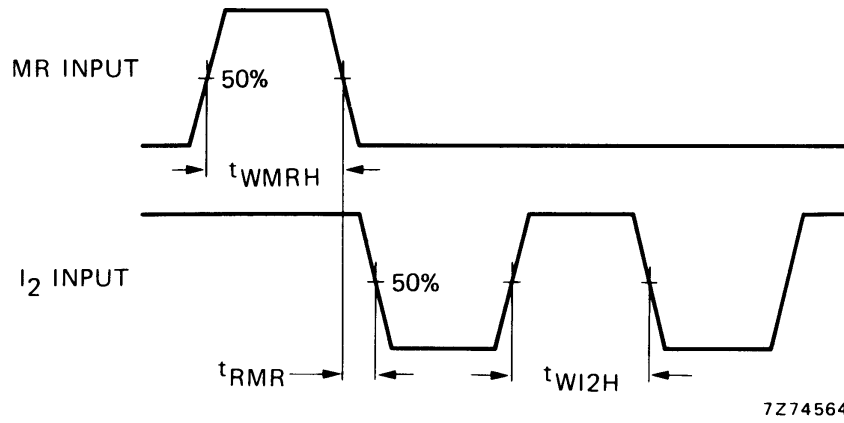
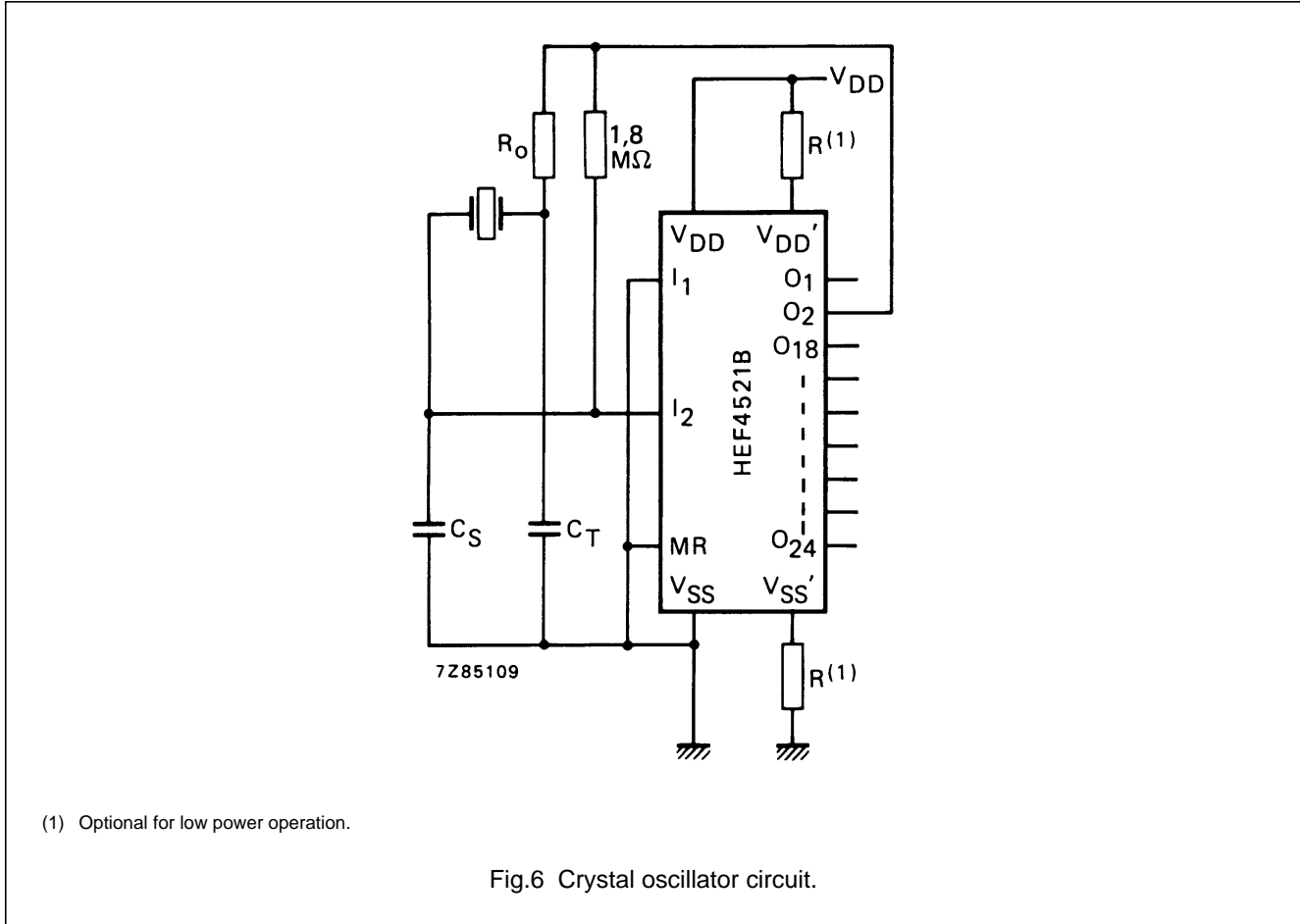


Fig.5 Waveforms showing minimum pulse widths for MR and I₂, recovery time for MR.

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APPLICATION INFORMATION

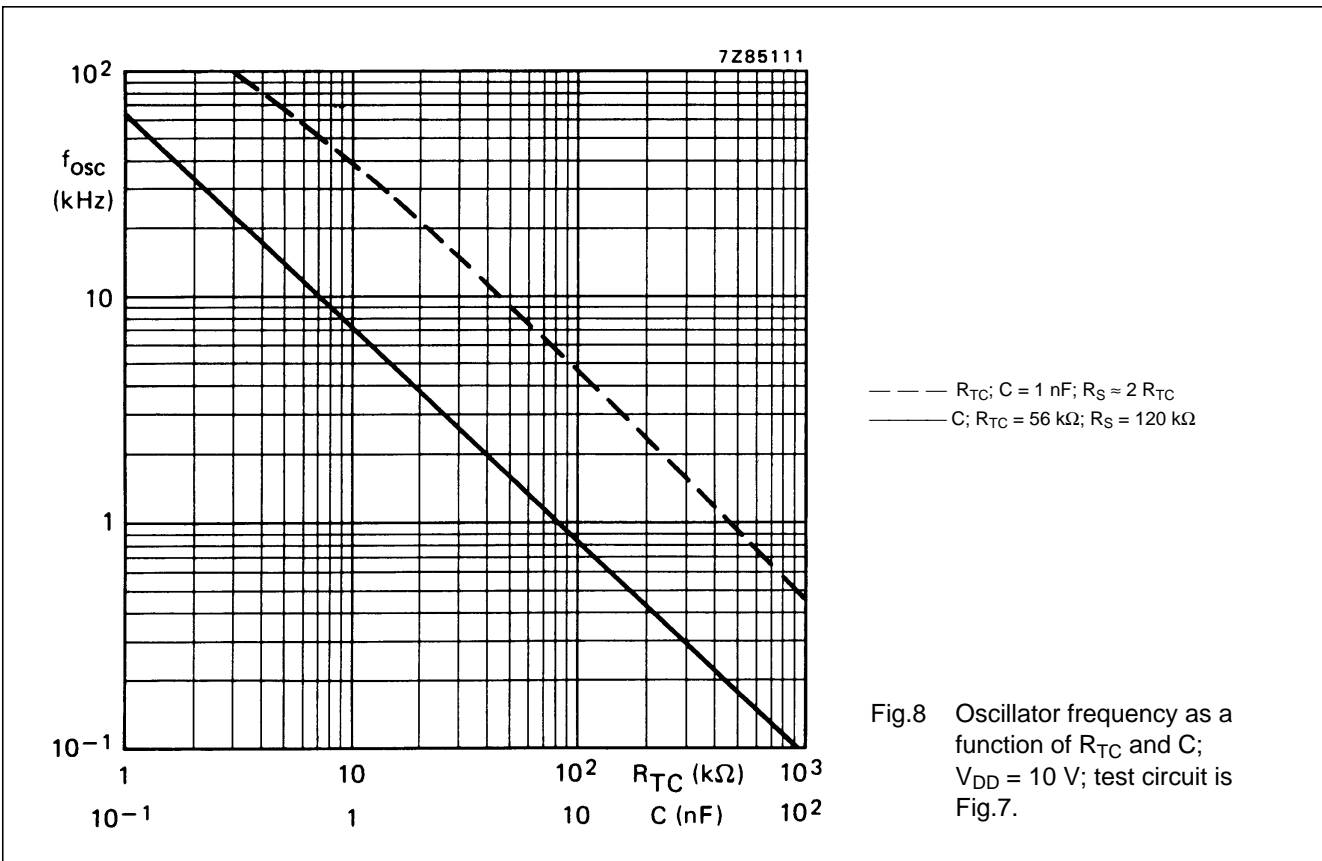
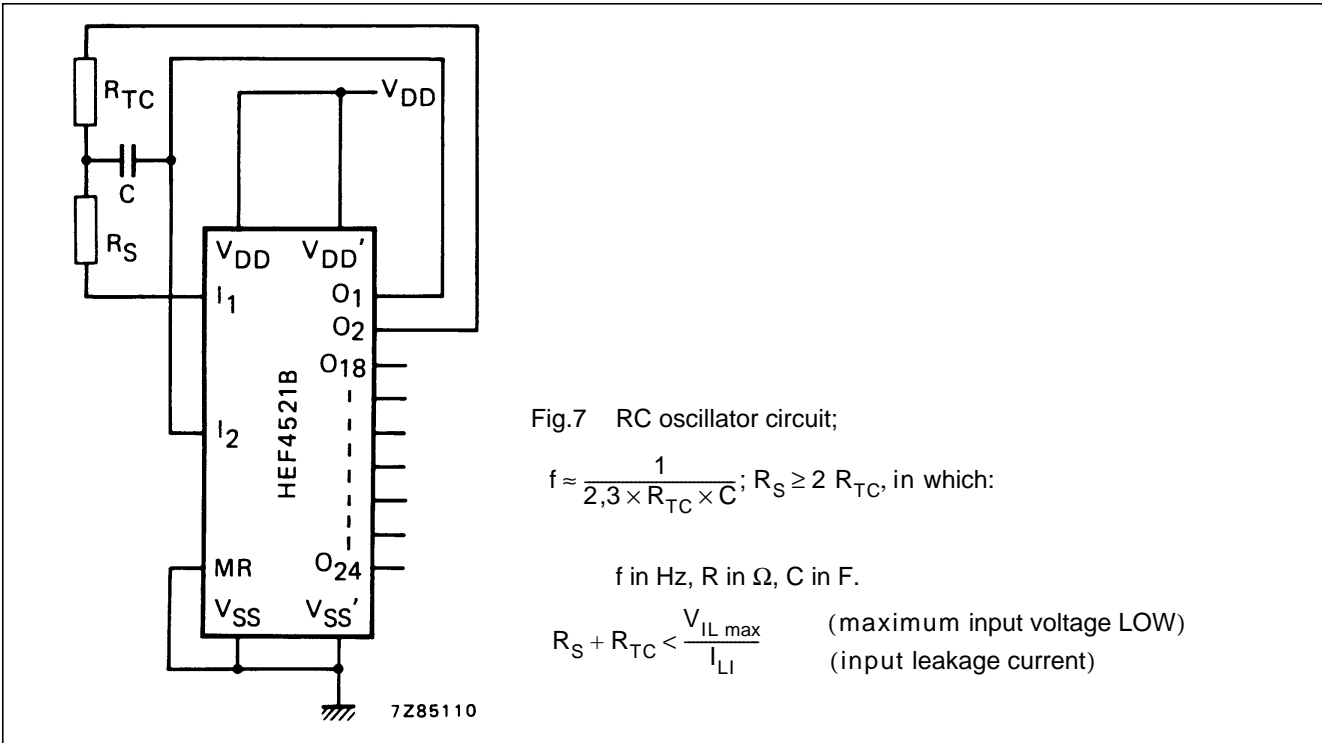


Typical characteristics for crystal oscillator circuit (Fig.6):

	500 kHz CIRCUIT	50 kHz CIRCUIT	UNIT
Crystal characteristics			
resonance frequency	500	50	kHz
crystal cut	S	N	-
equivalent resistance; R_S	1	6,2	kΩ
External resistor/capacitor values			
R_0	47	750	kΩ
C_T	82	82	pF
C_S	20	20	pF

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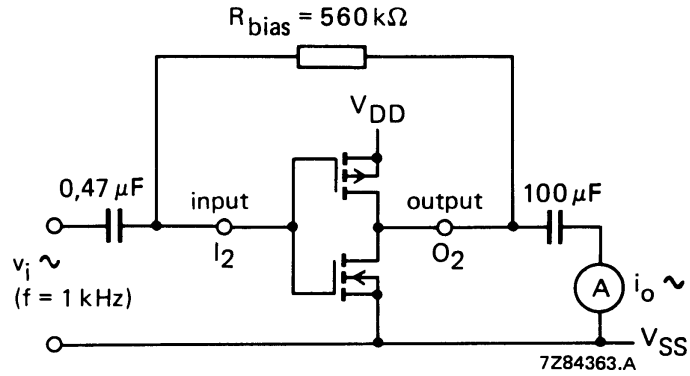
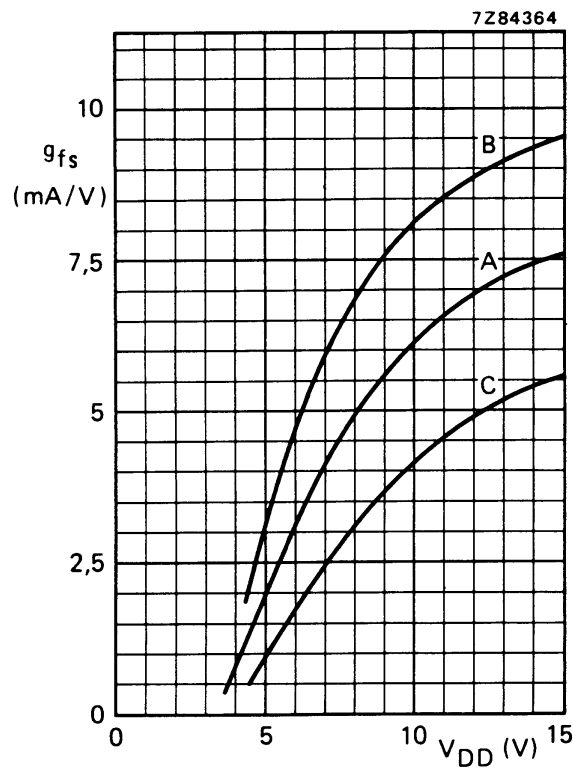


Fig.9 Test set-up for measuring forward transconductance $g_{fs} = di_o/dv_i$ at v_o is constant (see also graph Fig.10).

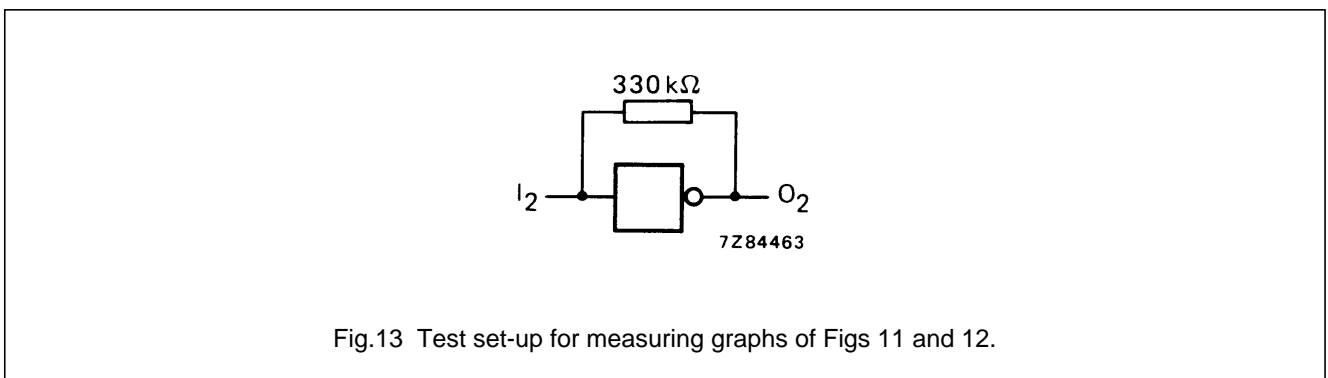
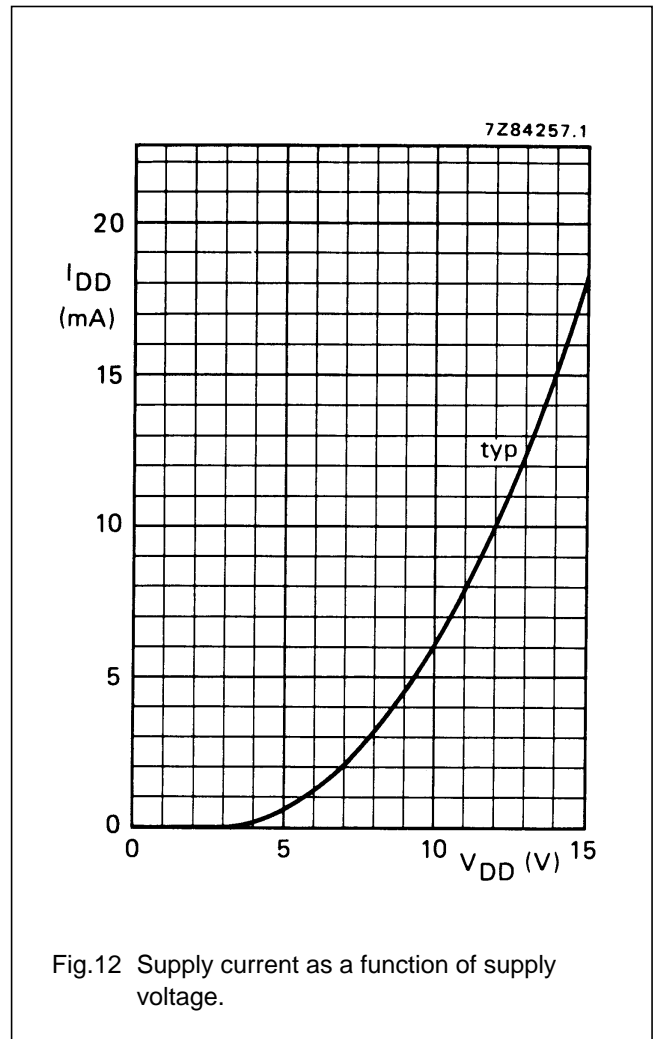
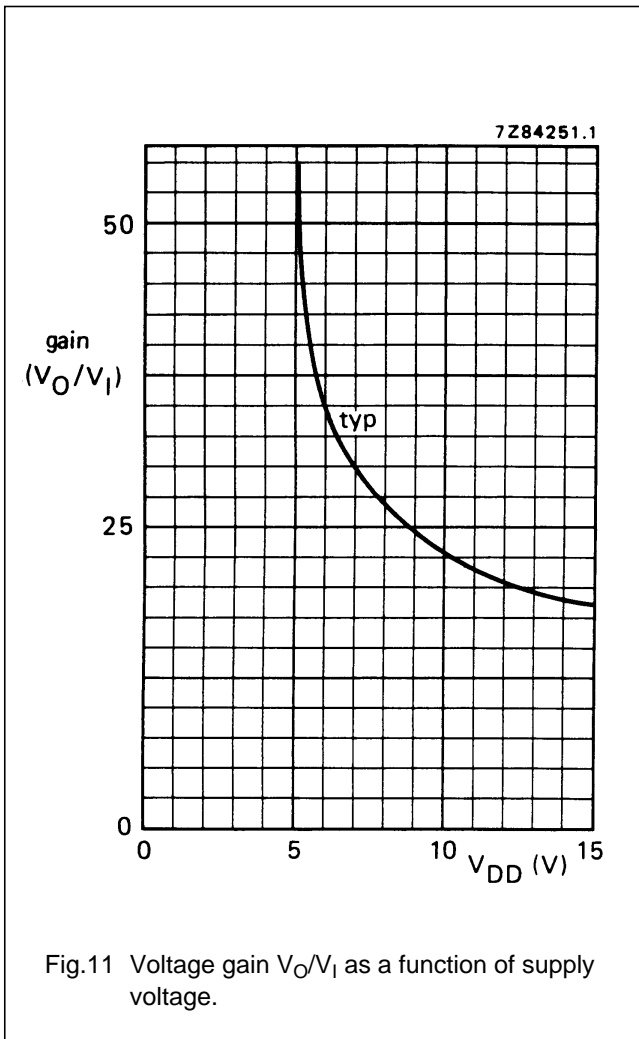


A: average,
 B: average + 2 s,
 C: average - 2 s, in which: 's' is the observed standard deviation.

Fig.10 Typical forward transconductance g_{fs} as a function of the supply voltage at $T_{amb} = 25\text{ }^\circ\text{C}$.

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