Single Chip 10BASE-FL Transceiver

Technical Data

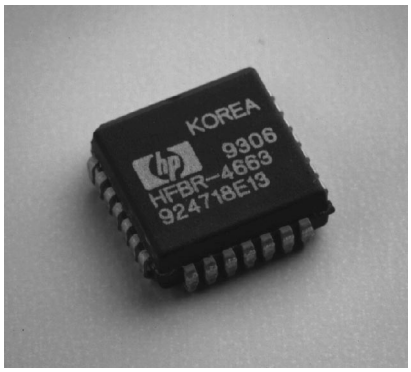
HFBR-4663

General Description

The HFBR-4663 Single Chip 10BASE-FL Transceiver is a highly integrated circuit for IEEE 802.3 10Base-FL transceivers. This product, when used with HP's fiber-optic transmitters and receivers (HFBR-14X4 and HFBR-2416), ensures compliance to the 10Base-FL Standard with a minimum number of external components and board space.

The HFBR-4663 offers a standard IEEE 802.3 AU interface that allows it to be directly connected to industry standard manchester encoder/decoder chips or an AUI connector. The fiber-optic LED driver offers a current drive output that directly drives the HFBR-14X4 transmitter. The data quantizer section of the HFBR-4663 is directly compatible with the output of the HFBR-24X6 fiber-optic receiver and is capable of accepting input signals as low as 2 mVp-p with a 55 dB dynamic range.

The transmitter automatically inserts 1 MHz signal during idle time and removes this signal on reception. Low light is continuously monitored for both activity as well as power level. Five LED status indicators monitor error conditions as well as transmissions, receptions, and collisions.

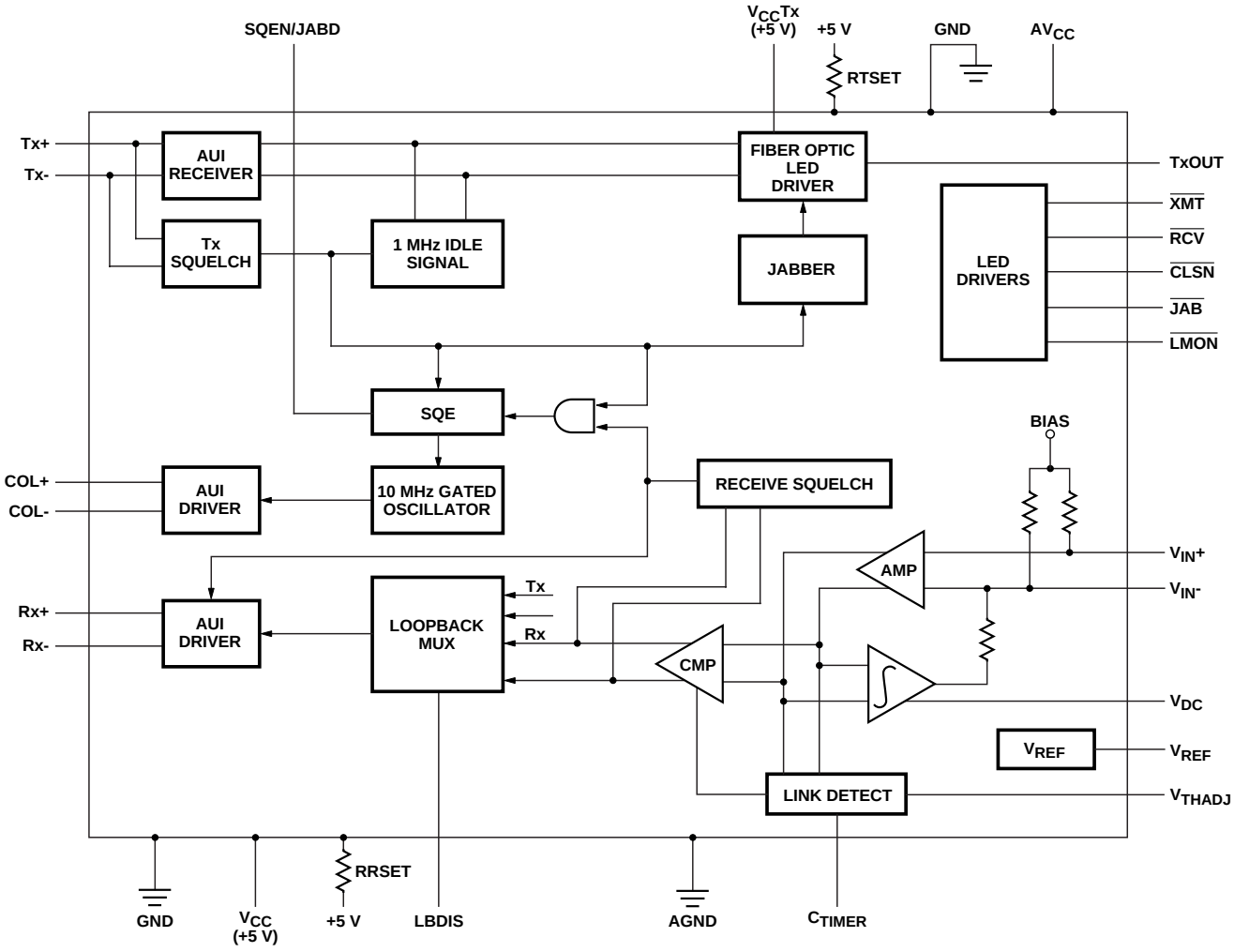


Features

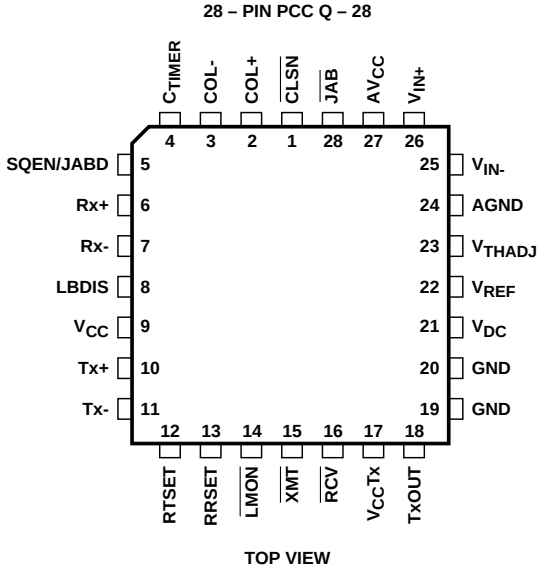
- **Single Chip Solution for 10BASE-FL Internal or External Medium Attachment Units (MAUs)**
- **Specifically Designed for Use with HFBR-14X4 and HFBR-24X6 Fiber-optic Transmitters and Receivers**
- **Incorporates an AU Interface**
- **Highly Stable Data Quantizer with 55 dB Input Dynamic Range**
- **Input Sensitivity as Low as 2 mV_{P-P}**
- **Current Driven Fiber Optic LED Driver for Accurate Launch Power**
- **Single +5 Volt Supply**
- **No Crystal or Clock Required**
- **Five Network Status LED Outputs**
- **Available in 28 Pin PCC Package**
- **Semi-Standard Option Available**

CAUTION: The small junction sizes inherent to the design of this component increase the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

Block Diagram



Pin Connection



Pin Description

Pin	Name	Function
1	$\overline{\text{CLSN}}$	Indicates that a collision is taking place. Active low LED driver, open collector. Event is extended with internal timer for visibility.
2	COL+	Gated 10 MHz oscillation used to indicate a collision, SQE test, or jabber.
3	COL-	Balanced differential line driver outputs that meet AUI specifications.
4	C_{TIMER}	A capacitor from this pin to V_{CC} determines the Link Monitor response time.
5	SQEN/JABD	SQE Test Enable, jabber Disable. When tied low, SQE test is disabled, when tied high SQE test is enabled. When tied to 2.0 V both SQE test and jabber are disabled.
6	Rx+	Manchester encoded receive data output to the local device. Balanced
7	Rx-	differential line driver outputs that meet AUI specifications.
8	LBDIS	Loopback Disable. When this pin is tied to V_{CC}, the AUI transmit pair data is not looped back to the AUI receive pair, and collision is disabled. When this pin is tied to GND (normal operation) or left floating, the AUI transmit pair data is looped back to the AUI receiver pair, except during collision.
9	V_{CC}	+5 V power input.
10	Tx+	Balanced differential line receiver inputs that meet AUI specifications. These
11	Tx-	inputs may be transformer or capacitively coupled. The Tx input pins are internally DC biased for AC coupling.
12	RTSET	Sets the current driven output of the transmitter.
13	RRSET	A 1% 61.9 kΩ resistor tied from this pin to V_{CC} sets the biasing currents for internal nodes.
14	$\overline{\text{LMON}}$	Link Monitor “Low Light” LED status output. This pin is pulled low when the voltage on the V_{IN}+, V_{IN}- inputs exceed the minimum threshold set by the V_{THADJ} pin, and there are transitions on V_{IN}+, V_{IN}- indicating an idle signal or active data. If either the voltage on the V_{IN}+, V_{IN}- inputs fall below the minimum threshold or transitions cease on V_{IN}+, V_{IN}-, $\overline{\text{LMON}}$ will go high. Active low LED driver, open collector.

Pin Description (cont.)

Pin	Name	Function
1 5	$\overline{\text{XMT}}$	Indicates that transmission is taking place. Active low LED driver, open collector. Event is extended with internal timer for visibility.
1 6	$\overline{\text{RCV}}$	Indicates that the transceiver is receiving a frame from the optical input. Active low LED driver, open collector. Event is extended with internal timer for visibility.
17	V_{CC}Tx	+5 V supply for fiber optic LED driver.
18	TxOUT	Fiber optic LED driver output.
19	GND	Ground Reference.
20	GND	Ground Reference.
21	V_{DC}	An external capacitor on this pin integrates an error signal which nulls the offset of the input amplifier. If the DC feedback loop is not being used, this pin should be connected to V_{REF}.
22	V_{REF}	A 2.5 V reference with respect to GND.
23	V_{THADJ}	This input pin sets the link monitor threshold.
24	AGND	Analog Filtered Ground.
25	V_{IN}-	This input pin should be capacitively coupled to the input source or to filtered AV_{CC}. (The input resistance is approximately 1.3 kΩ.)
26	V_{IN}+	This input pin should be capacitively coupled to the input source or to filtered AV_{CC}. (The input resistance is approximately 1.3 kΩ.)
27	AV_{CC}	Analog Filtered +5 V.
28	$\overline{\text{JAB}}$	Jabber network status LED. When in the jabber "OK" state this pin will be low and the transmitter will be disabled. In the jabber "OK" state this pin will be high. Active low LED, open collector.

Absolute Maximum Ratings[1]

Parameter	Symbol	Min.	Max.	Units
Storage Temperature	T_S	-65	+150	C
Operating Temperature	T_A	0	70	C
Lead Soldering Cycle Temperature			260	C
Lead Soldering Cycle Time			10	sec
Power Supply Voltage Range	V_{CC}	-0.3	6.0	V
Input Voltage Range	Digital Inputs (SQEN, LBDIS) Tx+, Tx-, V_{IN}+, V_{IN}-	-0.3 -0.3	6.0 6.0	V V
Input Current	RRSET, RTSET, JAB, CLSN, XMT, RCV, LMON		60	mA
Output Current	TxOUT		70	mA

Operating Conditions

Parameter	Min.	Typ.	Max.	Units
Supply Voltage (V_{CC})	4.75	5.0	5.25	V
LED on Current		10		mA
RRSET		61.9 k ± 1%		Ω
RTSET		140 ± 1%		Ω

Electrical Characteristics

Unless otherwise specified, T_A = 0°C to 70°C, V_{CC} = V_{CC}Tx = 5 V ± 5% [2,3]

Parameter	Condition	Min.	Typ.	Max.	Units
Power Supply Current I_{CC}: While Transmitting	V_{CC} = 5 V, RTSET = 140 Ω[4]			220	mA
LED Drivers: V_{CC}	I_{OL} = 10 mA[5]			0.8	V
Transmit Peak Output Current[6]	RTSET = 140 Ω	47	52	57	mA
Transmit Squelch Voltage Level (Tx+, Tx-)		-300	-250	-200	mV
Differential Output Voltage (Rx± , COL±)		± 550		± 1200	mV
Common Mode Output Voltage (Rx± , COL±)			4.0		V
Differential Output Voltage Imbalance (Rx± , COL±)				± 40	mV
SQE/JABD	SQE Test Disable Both Disabled Both Enabled	 1.5 V_{CC} - 0.5		0.3 V_{CC} - 2	V V V
LBDIS Threshold	Disabled Enabled	V_{CC} - 0.1		 1	V V
Common Mode Voltage (Tx+, Tx-)			3.5		V
Common Mode Voltage (V_{IN}+, V_{IN}-)			1.65		V
Reference Voltage		2.35	2.45	2.55	V
V_{REF} Output Source Current				5	mA
Amplifier Gain			100		V/V
Input Signal Range		2		1600	mV_{P-P}
External Voltage at V_{THADJ} to Set V_{TH}		0.5		2.7	V
Input Offset	V_{DC} = V_{REF} (DC loop active)		3		mV
Input Referred Noise	50 MHz BW		25		µV
Input Resistance	V_{IN}+, V_{IN}-	0.8	1.3	2.0	kΩ
Input Bias Current of V_{THADJ}		-200	10	+200	µA
Input Threshold Voltage	V_{THADJ} = V_{REF}[7]	5	6	7	mV_{P-P}
Hysteresis			20		%

AC Electrical Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units
Transmit					
t_{TXNPW}	Transmit Turn-On Pulse Width		20		ns
t_{TXFPW}	Transmit Turn-Off Pulse Width from Data to Idle	400		2100	ns
t_{TXLP}	Transmit Loopback Start-up Delay			500	ns
t_{TXODY}	Transmit Turn-On Delay			100	ns
t_{TXIDF}	Transmit Idle Frequency	0.85		1.25	MHz
t_{TXDC}	Transmit Idle Duty Cycle	45		55	%
t_{TXSDY}	Transmit Steady State Propagation delay		15	50	ns
t_{TXJ}	Transmit Jitter into 31 Ω Load			± 1.5	ns
Receive					
t_{RXSFT}	Receive Squelch Frequency Threshold	2.51		4.5	MHz
t_{RXODY}	Receive Turn-On Delay			270	ns
t_{RXFX}	Last Bit Received to Slow Decay Output	230	300		ns
t_{RXSDY}	Receive Steady State Propagation Delay		15	50	ns
t_{RXJ}	Receive Jitter			± 1.5	ns
t_{AR}	Differential Output Rise Time 20% to 80% (Rx± , COL±)		4		ns
t_{AF}	Differential Output Fall Time 20% to 80% (Rx± , COL±)		4		ns
Collision					
t_{CPSQE}	Collision Present to SQE Assert	0		350	ns
t_{SQEXR}	Time for SQE to Deactivate After Collision	0		700	ns
t_{CLF}	Collision Frequency	8.5		11.5	MHz
t_{CLPDC}	Collision Pulse Duty Cycle	40	50	60	%
t_{SQEDY}	SQE Test Delay (Tx Inactive to SQE)	0.6		1.6	µs
t_{SQETD}	SQE Test Duration	0.5	1.0	1.5	µs
Jabber and LED Timing					
t_{JAD}	Jabber Activation Delay	20	70	150	ms
t_{JRT}	Jabber Reset Unjab Time	250	450	750	ms
t_{JSQE}	Delay from Outputs Disabled to Collision Oscillator On		100		ns
t_{LED}	$\overline{RCV}$, $\overline{CLSN}$, $\overline{XMT}$ On Time	8	16	32	ms
t_{LLPH}	Low Light Present to $\overline{LMON}$ High	3	5	10	µs
t_{LLCL}	Low Light Present to $\overline{LMON}$ Low	250		750	ms

Notes:
1. Absolute maximum ratings are limits beyond which the life of the integrated circuit may be impaired. All voltages unless otherwise specified are measured with respect to ground.
2. Limits are guaranteed by 100% testing, sampling, or correlation with worst-case test conditions.
3. Low Duty Cycle pulse testing is performed at T_A.
4. This does not include the current from the AUI pull-down resistors, or LED status otuputs.
5. LED drivers can sink up to 20 mA, but V_{OL} will be higher.
6. Does not include pre-bias current for fiber optic LED which would typically be 3 mA.
7. Threshold for switching from Link Fail ot Link Pass (Low Light).

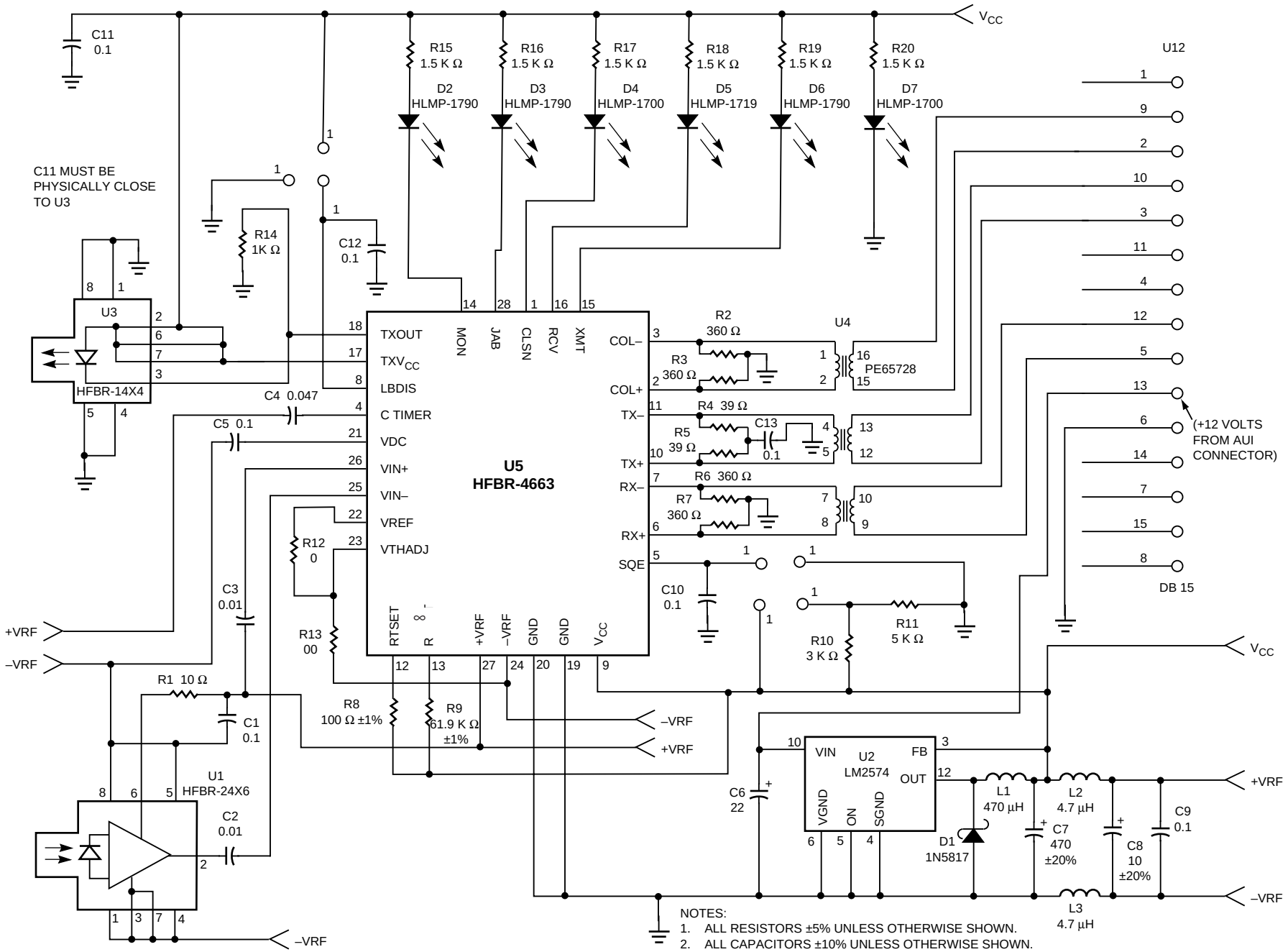


Figure 1. HFBR-4663 Schematic Diagram.

NOTES:
1. ALL RESISTORS ±5% UNLESS OTHERWISE SHOWN.
2. ALL CAPACITORS ±10% UNLESS OTHERWISE SHOWN.
3. THE HFBR-4663 DATA SHEET (PUBLICATION #5091-7391E 4/93) CONTAINS ERRORS THAT HAVE SUBSEQUENTLY BEEN CORRECTED IN THIS SCHEMATIC.
4. ALL CAPACITORS ARE IN µF.

System Description

Figure 1 shows a schematic diagram of the HFBR-4663 in an internal or external 10BASE-FL MAU. On one side of the transceiver is the AU interface and the other is the fiber optic interface. The AU interface is AC coupled when used in an external transceiver or an internal transceiver. The AU interface for an external transceiver includes isolation transformers, some biasing resistors, and a voltage regulator for power.

The fiber optic side of the transceiver requires an external fiber optic transmitter and fiber optic receiver. The transmitter uses a current driven output that directly drives the fiber optic transmitter. The receive side of the transceiver accepts the data after passing through a fiber optic receiver, which consists of a module containing a pin diode and a transimpedance amplifier.

AU Interface

The AU interface consists of 3 pairs of signals, DO, CI and DI as shown in Figure 1. The DO pair contains transmit data from the DTE which is received by the transceiver and sent out onto the fiber optic cable. The DI pair contains valid data that has been either received from the fiber optic cable or looped back from the DO and output through the DI pair to the DTE. The CI pair indicates whether a collision has occurred. It is an output that oscillates at 10 MHz if a collision, jabber or SQE Test has taken place, otherwise it remains idle.

When the transceiver is external, these three pairs are AC coupled through isolation transformers, while an internal transceiver may be capacitively coupled. Tx+, Tx- is internally DC biased (shifted up in voltage) for the proper common mode input voltage.

The two 39 Ω 1% resistors (or one 78 Ω 1% resistor) tied to he Tx+ and Tx- pins will provide the proper termination. The CI and DI pair, which are output from the transceiver to the AUI cable, require 360 Ω pull down resistors when terminated with a 78 Ω load. However on a DTE card, CI and DI do not need 78 Ω terminating resistors. This also means that the pull down resistors on CI and DI can be 1 kΩ or greater depending upon the particular Manchester encoder/ decoder chip used. Using higher value pull down resistors as in a DTE card will save power.

The AUI drivers are capable of driving the full 50 meters of cable length and have a rise and fall time of typically 4 ns. In the idle state, the outputs go to the same voltage to prevent DC standing current in the isolation transformers.

Transmission

The transmit function consists of detecting the presence of data from the AUI DO input (Tx+, Tx-) and driving that data onto the fiber optic LED transmitter. A positive signal on the Tx+ lead relative to the Tx- lead of the DO circuit will result in no current, hence the fiber optic LED is in a low light condition. When Tx+ is more negative than Tx-, the HFBR-4663 will sink current into the chip and the fiber optic LED will emit light.

Before data will be transmitted onto the fiber optic cable from the AU interface, it must exceed the squelch requirements for the DO pair. The Tx squelch circuit serves the function of preventing any noise from being transmitted onto the fiber. This circuit rejects signals with pulse widths less than typically 20 ns (negative going), or with levels less than -250 mV. Once Tx squelch circuit has unsquelched, it looks for the start of idle signal to turn on the squelch circuit again. The transmitter turns on the squelch again when it receives an input signal at Tx+, Tx- that is more positive than -250 mV for more than approximately 180 ns.

At the start of a packet transmission, no more than 2 bits are received from the DO circuit and not transmitted onto the fiber optic cable. The difference between start-up delays (bit loss plus steady-state propagation delay) for any two packets that are separated by 9.6 µs or less will not exceed 200 ns.

Fiber Optic LED Driver

The output stage of the transmitter is a current mode switch which controls the output light by sinking current through the LED into the TxOUT pin. Once the current requirement for the LED is determined, the RTSET resistor is selected. The following equation is used to select the

correct RTSET resistor:

$$RTSET = \left(\frac{52\ mA}{IOUT}\right) 162\ \Omega$$

The transmitter enters the idle state when it detects start of idle on Tx+ and Tx- input pins. After detecting the start of idle, the transmitter switches to a 1 MHz output idle signal.

The output current is switched through the TxOUT pin during the on cycle and the V_{CC}Tx pin during the off cycle as shown in figure 2. Since the sum of the current in these two pins is constant, V_{CC}Tx should be connected as close as possible to the V_{CC} connection for the LED.

If not driving an optical LED directly, a differential output can be generated by tying resistors from V_{CC}Tx and TxOUT to V_{CC} as shown in Figure 3. The minimum voltage on these two pins should not be less than V_{CC} - 2 V.

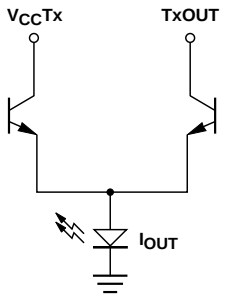


Figure 2. Fiber Optic LED Driver Structure.

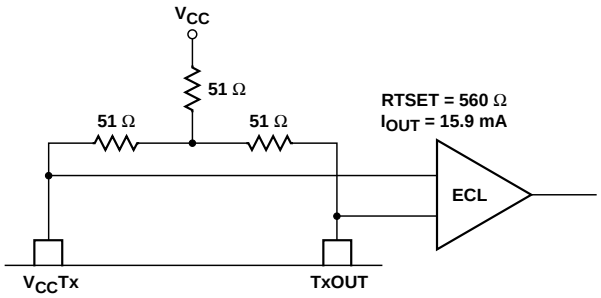


Figure 3. Converting Optical LED Driver Output to Differential ECL.

Reception

The input to the transceiver comes from a fiber optic receiver as shown in figure 1. At the start of packet reception no more than 2.7 bits are received from the fiber cable and not transmitted onto the DI circuit. The receive squelch will reject frequencies lower than 2.51 MHz.

While in the unsquelch state, the receive squelch circuit looks for the start of idle signal at the end of the packet. Start of idle occurs when the input signal remains idle for more than 160 ns. When start of idle is detected, the receive squelch circuit returns to the squelch state and the start of idle signal is output on the DI circuit (Rx+, Rx-).

Collision

Whenever the receiver and the transmitter are active at the same time the chip will activate the collision output, except when loopback is disabled (LBDIS = Vcc). The collision output is a differential square wave matching the AUI specifications and capable of driving a 78 Ω load. The frequency of the square wave is 10 MHz ± 15% with a 60/40 to 40/60 duty cycle. The collision oscillator also is activated during SQE Test and jabber.

Loopback

The loopback function emulates a 10BASE-T transceiver whereby the transmit data sent by the DTE is looped back over the AUI receive pair. Some LAN controllers use this loopback information to determine whether a MAU is connected by monitoring the carrier sense while transmitting. The software can use this loopback information to determine whether a MAU is connected to the DTE by checking the status of carrier sense after each packet transmission.

When data is received by the chip while transmitting, a collision condition exits. This will cause the collision oscillator to turn on and the data on the DI pair will follow V_{IN}+, V_{IN}-. After a collision is detected, the collision oscillator will remain on until either DO or V_{IN}+, V_{IN}- go idle.

Loopback can be disabled by strapping LBDIS to V_{CC}. In this mode the chip operates as a full duplex transmitter and receiver, and collision detection is disabled. A loopback through the transceiver can be accomplished by tying the fiber transmitter to the receiver.

SQE Test Function Signal Quality Error

The SQE test function allows the DTE to determine whether the collision detect circuitry is functional. After each transmission, during the inter packet gap time, the collision oscillator will be activated for typically 1 µs. The SQE test will not be activated if the chip is in the low light state, or the jabber on state.

For SQE to operate, the SQEN pin must be tied to V_{CC}. This allows the MAU to be interfaced to a DTE. The SQE test can be disabled by tying the SQEN pin to ground, for a repeater interface.

Jabber Function Requirements

The Jabber function prevents a babbling transmitter from bringing down the network. Within the transceiver is a Jabber timer that starts at the beginning of each transmission and resets at the end of each transmission. If the transmission lasts longer than 20 ms the jabber logic disables the transmitter, and turns on the collision signal COL+, COL-. When Tx+ and Tx- finally go idle, a second timer measures 0.5 seconds of idle time before the transmitter is enabled and collision is turned off. Even though the transmitter is disabled during jabber, the 1 MHz idle signal is still transmitted.

LED Drivers

The HFBR-4663 has five LED drivers. The LED driver pins are active low, and the LEDs are normally off (except for $\overline{\text{LMON}}$). The LEDs are tied to their respective pins through a 500 Ω resistor to 5 volts.

The $\overline{\text{XMT}}$, $\overline{\text{RCV}}$ and $\overline{\text{CLSN}}$ pins have pulse stretchers on them which enable the LEDs to be visible. When transmission or reception occurs, the LED $\overline{\text{XMT}}$, $\overline{\text{RCV}}$ or $\overline{\text{CLSN}}$ status pins will activate low for several milliseconds. If another transmit, receive or collision condition occurs before the timer expires, the LED timer will reset and restart the timing. Therefore rapid events will leave the LEDs continuously on. The $\overline{\text{JAB}}$ and $\overline{\text{LMON}}$ LEDs do not have pulse stretchers on them since their conditions occur long enough for the eye to see.

Low Light Condition

The $\overline{\text{LMON}}$ LED output is used to indicate a low light condition. $\overline{\text{LMON}}$ is activated low when both the receive power exceeds the Link Monitor threshold and there are transitions on V_{IN}+, V_{IN}- less than 3 µs apart. If either one of these conditions do not exist, $\overline{\text{LMON}}$ will go high.

Input Amplifier

The V_{IN}+, V_{IN}- input signal is fed into a limiting amplifier with a gain of about 100 and input resistance of 1.3 kΩ. Maximum sensitivity is achieved through the use of a DC restoration feedback loop and AC coupling the input. When AC coupled, the input DC bias voltage is set by an on-chip network at about 1.7 V. These coupling capacitors, in conjunction with the input impedance of the amplifier, establish a high pass filter with 3 dB corner frequency, f_L, at

$$f_L = \frac{1}{2\pi 1300C}$$

Since the amplifier has a differential input, two capacitors of equal value are required. If the signal driving the input is single ended, one of the coupling capacitors can be tied to AV_{CC} as shown in Figure 1.

The internal amplifier has a lowpass filter built-in to band limit the input signal which in turn will improve the signal noise ratio.

Although the input is AC coupled, the offset voltage *within* the amplifier will be present at the amplifier's output. This is represented by V_{OS} in Figure 4. In order to reduce this error a DC feedback loop is incorporated. This negative feedback loop nulls the offset voltage, forcing V_{OS} to be zero. Although the capacitor on V_{DC} is non-critical, the pole it creates can affect the stability of the feedback loop. To avoid stability problems, the value of this capacitor should be at least 10 times larger than the input coupling capacitors.

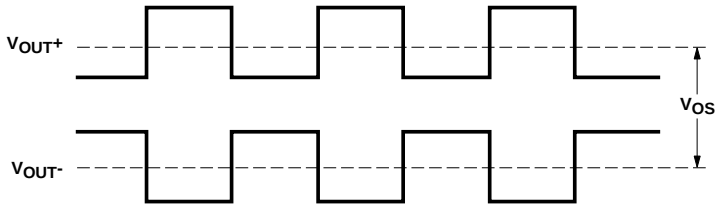


Figure 4.

The comparator is a high-speed differential zero crossing detector that slices and accurately digitizes the receive signal. The output of the comparator is fed in parallel into both the receive squelch circuit and the loopback MUX.

Link Detect Circuitry and Low Light

The link detect circuit monitors the input signal and determines when the input falls below a preset voltage level. When the input falls below a preset voltage, the HFBR-4663 goes into the Low Light state. In the Low Light state the transmitter is disabled, but continues sending the I MHz idle signal, the loopback is disabled, the receiver is disabled and the $\overline{\text{LMON}}$ LED pin goes to high shutting off the $\overline{\text{LMON}}$ LED. To return to the Link Pass state, the optical receiver power must be 20% higher than the shut-off state. This built-in hysteresis adds stability to the Link Monitor circuit. Once the receiver power threshold is exceeded, the HFBR-4663 waits 250 ms to 750 ms, then checks to see that Tx+, Tx- is idle and no data is being received before re-enabling the transmitter, receiver, loopback circuit, and lighting up the $\overline{\text{LMON}}$ LED.

The V_{THADJ} pin is used to adjust the sensitivity of the receiver. The HFBR-4663 is capable of exceeding the 10BASE-FL specifications for sensitivity. The sensitivity is dependent on the layout of the PC board. A good low noise layout will exceed the 10BASE-FL specifications, while a poor layout will fail to meet the sensitivity and BER spec.

The threshold generator shifts the reference voltage at V_{THADJ} through a circuit which has a temperature coefficient matching that of the limiting amplifier. The relationship between the V_{THADJ} and the V_{TH} (the peak to peak input threshold) is:

$$V_{THADJ} = 408\ V_{TH} \quad (2)$$

In a 10BASE-FL receiver, there must be less than 1×10^{-9} bit errors at a receive power level of -32.5 dBm average. One procedure to determine the sensitivity of a receiver is to start at the lowest optical power level and gradually increase the optical power until the BER is met. In this case the Link Detect circuit must not disable the receiver (i.e. V_{THADJ} should be tied to Ground). Once the sensitivity of the receiver is determined, V_{THADJ} can be set just above the power level that meets the BER specification. This way the receiver will shut-off before the BER is exceeded.

For 10-BASE-FL, V_{THADJ} can be tied directly to V_{REF}. However if greater sensitivity is required the circuit in Figure 5 can be used to adjust the V_{THADJ} voltage. Even if V_{REF} is tied to V_{THADJ}, it is a good idea to layout a board with these two resistors available. This will allow potential future adjustments without board revisions.

The response time of the Link Detect circuit is set by the C_{TIMER} pin. Starting from the link off state the link can be switched on if the input exceeds the set threshold for a time given by:

$$T = \frac{C_{TIMER} \times 0.7\ V}{700\ \mu A}$$

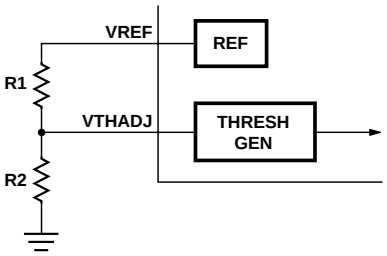


Figure 5.

To switch the link from on to off, the above time will be doubled. A value of 0.05 µF will meet the 10BASE-FL specifications.

Differences between 10BASE-FL and FOIRL

10BASE-FL is an improved version of the original FOIRL standard. The 10BASE-FL standard allows backward compatibility of a 10BASE-FL transceiver with a FOIRL transceiver. The main improvements incorporated into 10BASE-FL are that it can attach to a DTE by adding the SQE test, and the distance has been increased from 1 km to 2 km. The other differences are much more subtle.

1. SQE Test: The FOIRL standard did not include the option of attaching a fiber transceiver to a DTE. Adding the SQE test to 10BASE-FL enables a 10BASE-FL transceiver to attach to a DTE.

2. 0 to at Least 2 Km Distance: The FOIRL standard specifies a 1 km distance while 10BASE-FL specifies 2 km. The additional 1 km distance for 10BASE-FL comes from an increased flux budget for the cable of 3.5 dB. This 3.5 dB increase came from an increase of 2.5 dB sensitivity for the receiver and a 1 dB improvement for the transmitter. The following table illustrates the transmit and receive power requirements for the two standards. Note: FOIRL specifies optical power in peak and 10BASE-FL specifies it in average. Subtracting 3 dB from peak will give the average. In the table below the FOIRL specifications were converted from peak to average power.

3. MAU State Diagrams are Different: The state diagrams for 10BASE-FL are similar to 10BASE-T, while the state diagrams for FOIRL are slightly different. The differences are in the AUI loopback, and in the link integrity function.

AUI Loopback - In 10BASE-FL the DO to DI loopback is always disabled during a collision, and optical receive data is passed through to DI. For FOIRL there are some cases where loopback continues (i.e. DO looped to DI) during a collision, and others where loopback is disabled during a collision. 10BASE-FL is identical to 10BASE-T in this case. Please refer to the IEEE standards for greater detail.

Link Integrity - 10BASE-FL adds an additional state to the Link Integrity Test function that will not allow an exit from the Low Light State until both the transmitter and receiver are idle. In FOIRL, it is possible to exit from the Low Light State while still receiving data.

MAU Timing Differences - The timing differences between 10BASE-FL and FOIRL relate to propagation delays, start-up delays, and collision deassert delays. The following table provides the details of these parameters.

Timing Parameter Differences	FOIRL (BIT Times)	10BASEFL (BIT Times)
ORD input to input on DI		
Steady State Prop Delay	0.5	2
Start-Up Delay	3.5	5
Output on DO to OTD_output		
Steady State Prop Delay	0.5	2
Start-Up Delay	3.5	5
Collision Deassert to SQE Deassert minimum	**4.5**	**0**

OTD - Optical Transmit Data
ORD - Optical Receive Data
DI, DO, CI - AU Interface Signals

Transmit/Receive Average Power	Min.	Max.	Conditions
FOIRL			
Transmitter	-12 dBm	-21 dBm	
Receiver	-12 dBm	-30 dBm	BER < 10^{-10}
10BASE-FL			
Transmitter	-12 dBm	-20 dBm	
Receiver	-12 dBm	-32.5 dBm	BER < 10^{-9}

Timing Diagrams

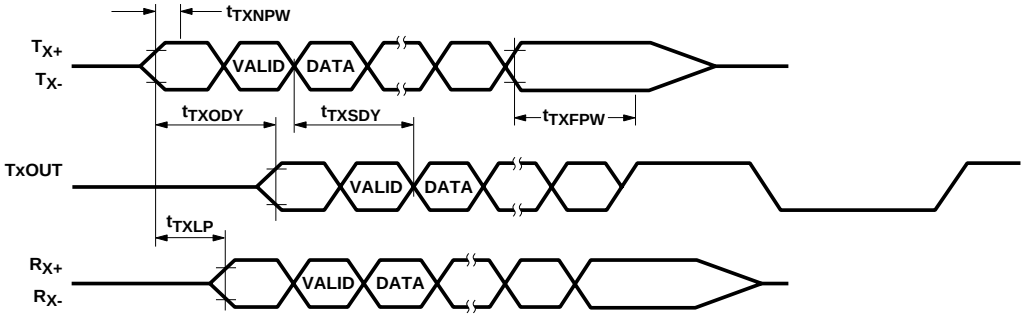


Figure 6. Transmit and Loopback Timing.

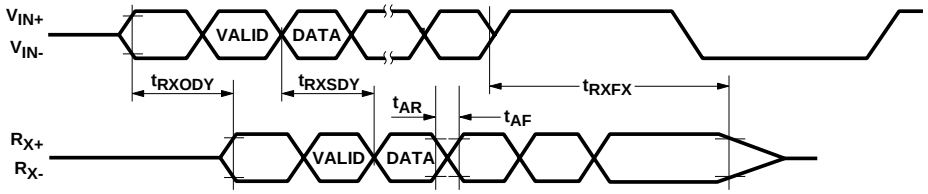


Figure 7. Receive Timing.

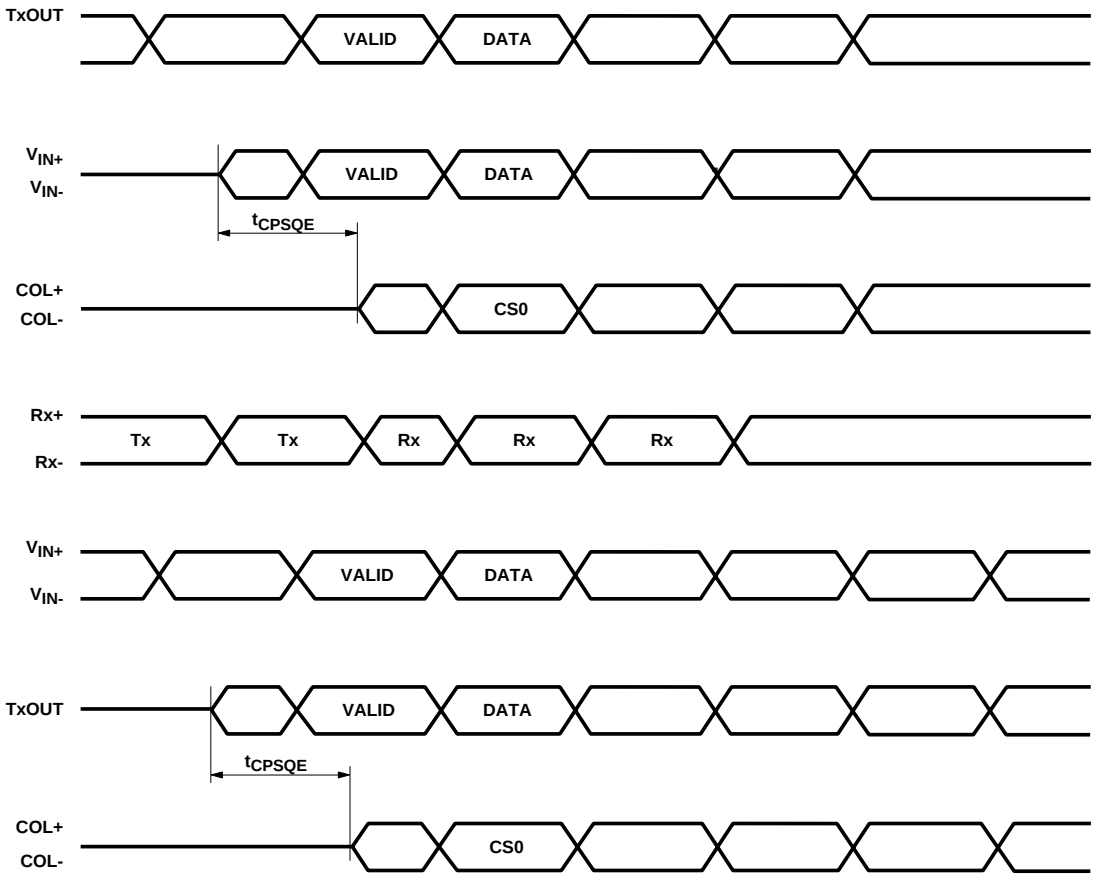


Figure 8. Collision Timing.

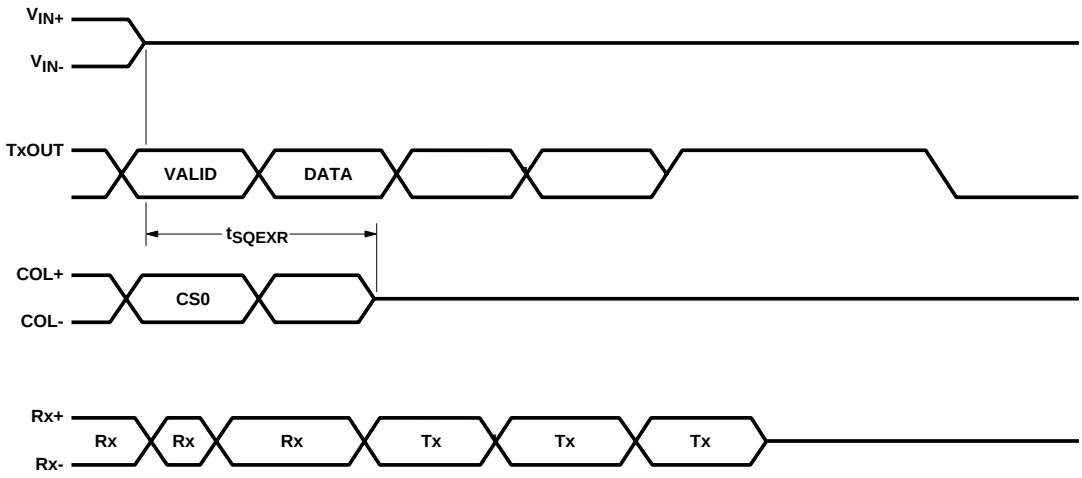


Figure 9. Collision Timing.

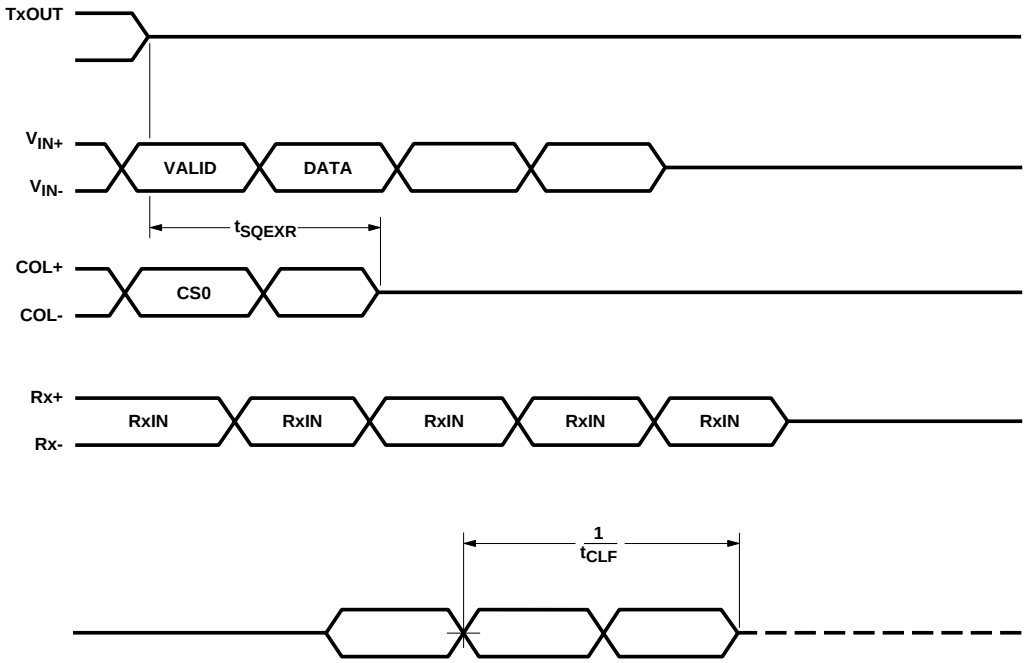


Figure 10. Collision Timing.

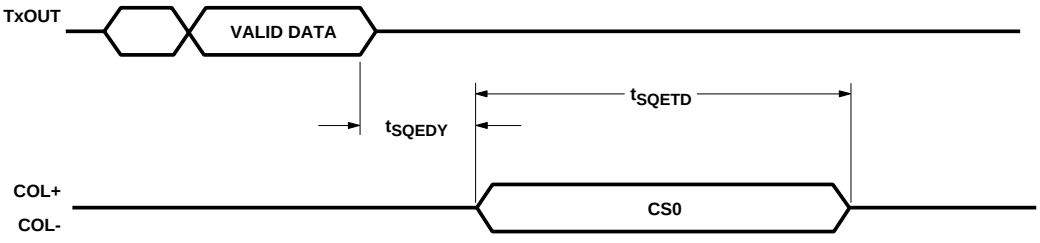


Figure 11. SQE Timing.

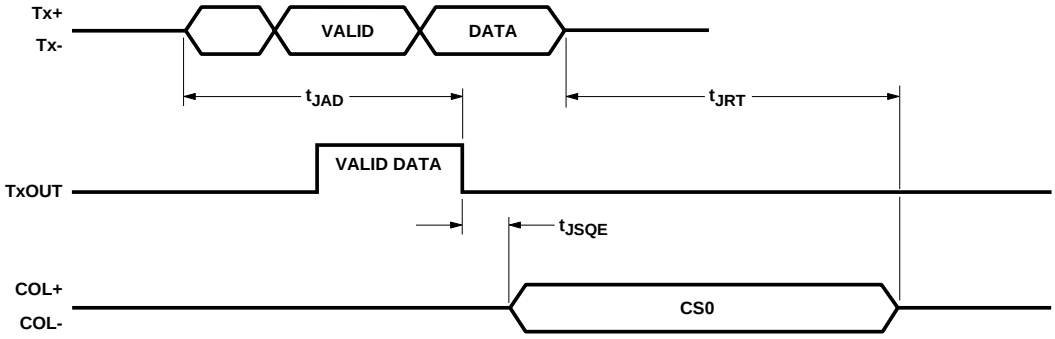


Figure 12. Jabber Timing.

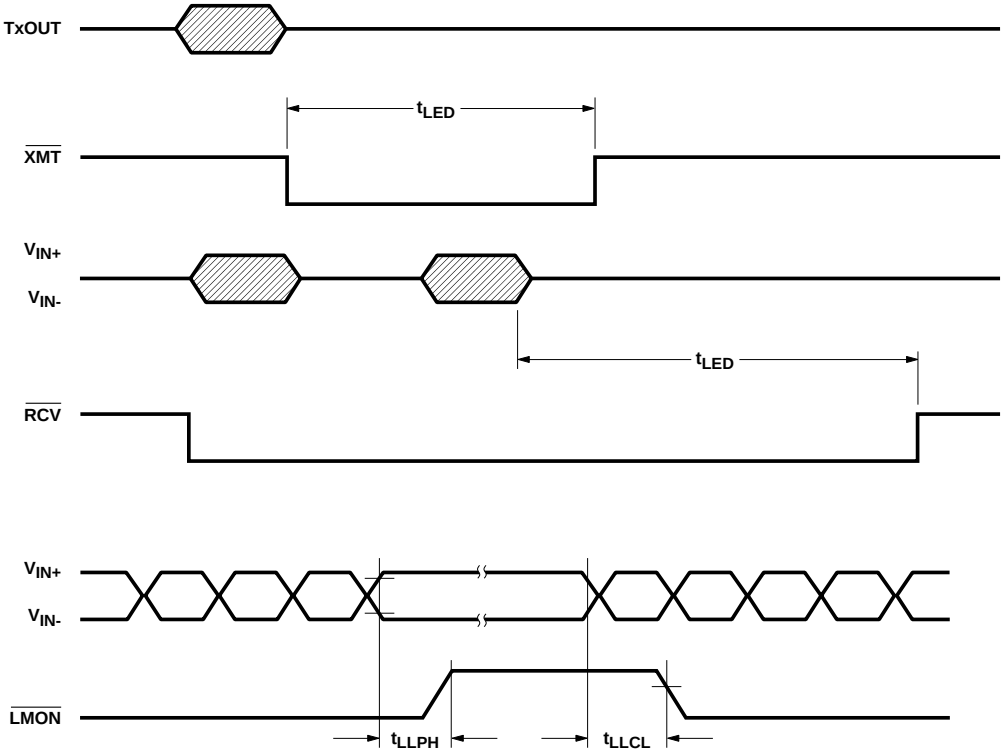


Figure 13. LED Timing.

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