HOLT INC.
INTEGRATED CIRCUITS

March 2001

HI-1567, HI-1568

MIL-STD-1553 / 1760
5V Monolithic Dual Transceivers

DESCRIPTION

The HI-1567 and HI-1568 are low power CMOS dual transceivers designed to meet the requirements of MIL-STD-1553 /1760 specifications.

The transmitter section of each channel takes complimentary CMOS / TTL digital input data and converts it to bi-phase Manchester encoded 1553 signals suitable for driving the bus isolation transformer. Separate transmitter inhibit control signals are provided for each transmitter.

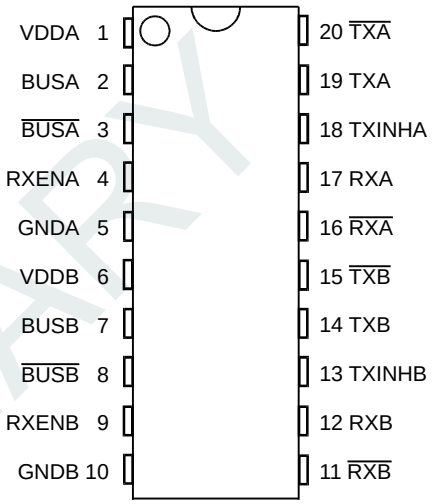
The receiver section of the each channel converts the 1553 bus bi-phase data to complimentary CMOS / TTL data suitable for inputting to a Manchester decoder. Each receiver has a separate enable input which can be used to force the output of the receiver to a logic 0 (HI-1567) or logic 1 (HI-1568).

To minimize the package size for this function, the transmitter outputs are internally connected to the receiver inputs, so that only two pins are required for connection to each coupling transformer. For designs requiring independent access to transmitter and receiver 1553 signals, please contact your Holt Sales representative.

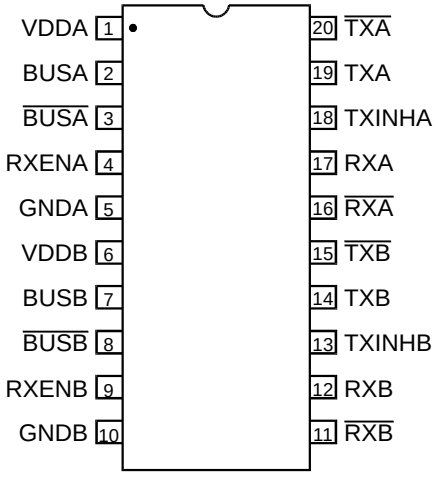
FEATURES

- Compliant to MIL-STD-1553A & B, MIL-STD-1760
- CMOS technology for low standby power
- Smallest footprint available in 20 pin plastic ESOIC (thermally enhanced SOIC) package
- Less than 1.0W maximum power dissipation
- Available in DIP, Flatpack and small outline (ESOIC) package options
- Military processing options
- Industry standard pin configurations

PIN CONFIGURATIONS



20 Pin Ceramic DIP package



20 Pin Plastic ESOIC - WB package

PIN DESCRIPTIONS

PIN	SYMBOL	FUNCTION	DESCRIPTION
1	VDDA	power supply	+5 volt power for channel A
2	BUSA	analog output	MIL-STD-1533 bus driver A, positive signal
3	$\overline{\text{BUSA}}$	analog output	MIL-STD-1553 bus driver A, negative signal
4	RXENA	digital input	Receiver A enable. If low, forces RXA and $\overline{\text{RXA}}$ low (HI-1567) or High (HI-1568)
5	GNDA	power supply	Ground for channel A
6	VDDB	power supply	+5 volt power for channel B
7	BUSB	analog output	MIL-STD-1533 bus driver B, positive signal
8	$\overline{\text{BUSB}}$	analog output	MIL-STD-1553 bus driver B, negative signal
9	RXENB	digital input	Receiver B enable. If low, forces RXB and $\overline{\text{RXB}}$ low (HI-1567) or High (HI-1568)
10	GNDB	power supply	Ground for channel B
11	$\overline{\text{RXB}}$	digital output	Receiver B output, inverted
12	RXB	digital output	Receiver B outpot, non-invertedl
13	TXINHB	digital input	Transmit inhibit, channel B. If high BUSB, $\overline{\text{BUSB}}$ disabled
14	TXB	digital input	Transmitter B digital data input, non-inverted
15	$\overline{\text{TXB}}$	digital input	Transmitter B digital data input, inverted
16	$\overline{\text{RXA}}$	digital output	Receiver A output, inverted
17	RXA	digital output	Receiver A output, non-inverted
18	TXINHA	digital input	Transmit inhibit, channel A. If high BUSA, $\overline{\text{BUSA}}$ disabled
19	TXA	digital input	Transmitter A digital data input, non-inverted
15	$\overline{\text{TXA}}$	digital input	Transmitter A digital data input, inverted

FUNCTIONAL DESCRIPTION

The HI-1567 family of data bus transceivers contain differential voltage source drivers and differential receivers. They are intended for applications using a MIL-STD-1553 A/B data bus. The device produces a trapezoidal output waveform during transmission.

TRANSMITTER

Data input to the transmitter section of these devices is from the complimentary CMOS /TTL inputs TXA/B and $\overline{\text{TXA/B}}$. This produces a nominal 30V peak to peak signal across a 140 ohm load. The transmitter is connected to the bus via a 1:2.5 transformer whose secondary is connected to two 52 ohm isolation resisters which feed the terminated 70 ohm bus. This will produce a nominal voltage on the bus of 7.5 volts peak to peak.

The transmitter is automatically inhibited and placed in the high impedance state when both TXA/B and $\overline{\text{TXA/B}}$ are either at a logic “1” or logic “0” simultaneously. A logic “1:” applied to the TXINHA/B input will force the transmitter to the high impedance state, regardless of the state of TXA/B and $\overline{\text{TXA/B}}$

RECEIVER

The receiver is transformer coupled to the bus by a 1:1 transformer. Its differential input stage drives a filter and threshold comparator. CMOS/TTL data is outputted at the RXA/B and $\overline{\text{RXA/B}}$ pins.

The receiver outputs can both be forced to a logic "0" (HI-1567) or logic “1” (HI-1568) by setting RXENA or RXENB low.

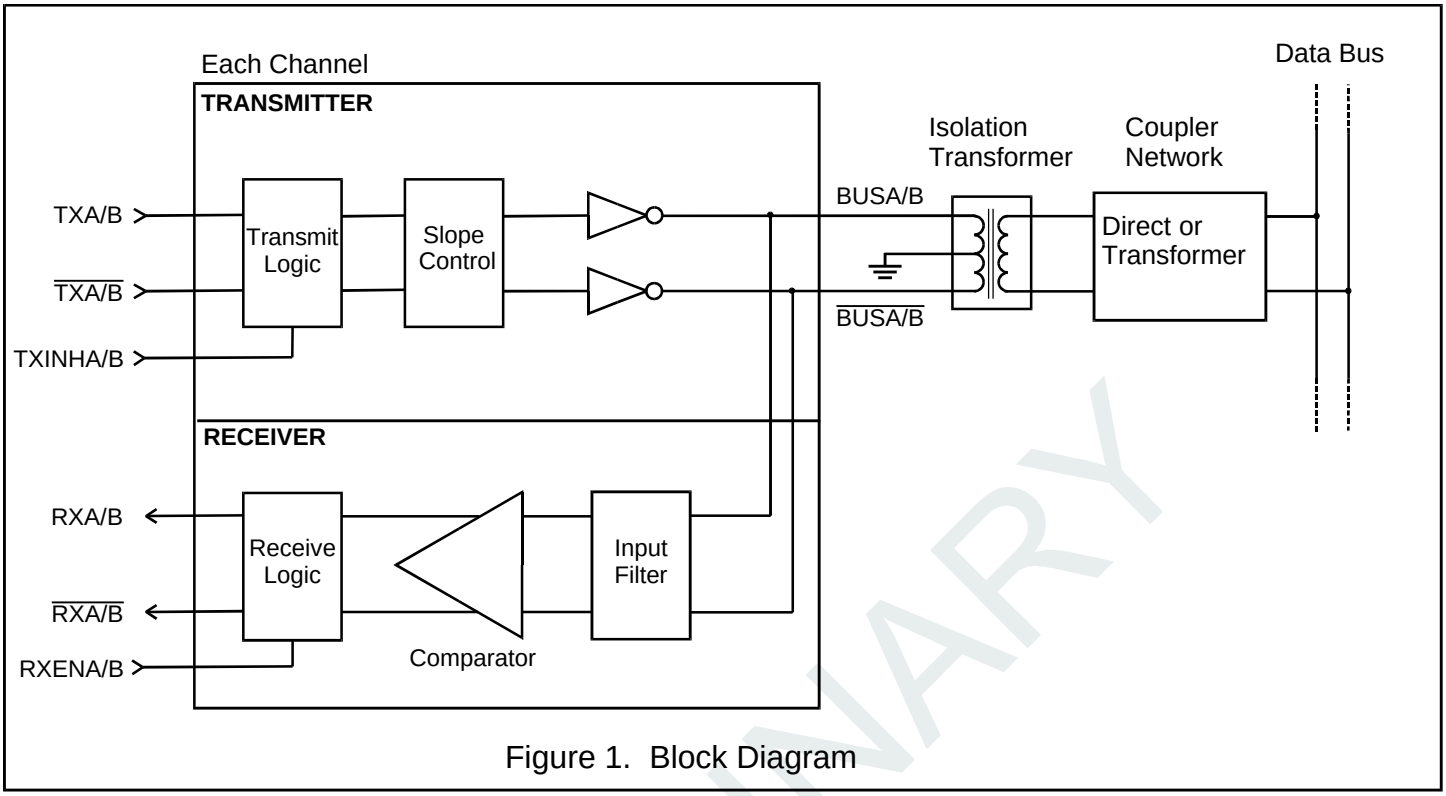
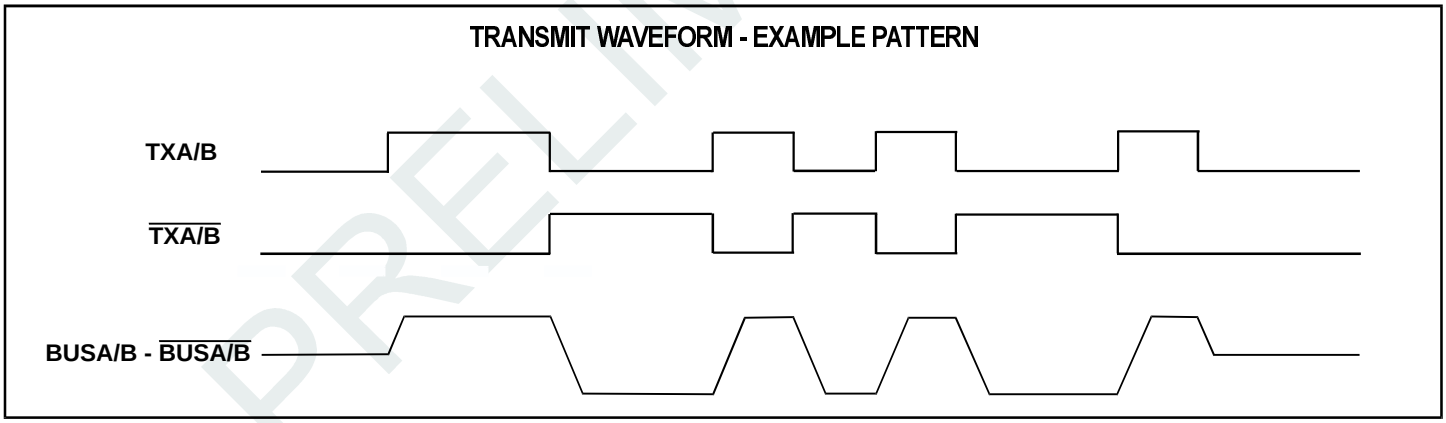
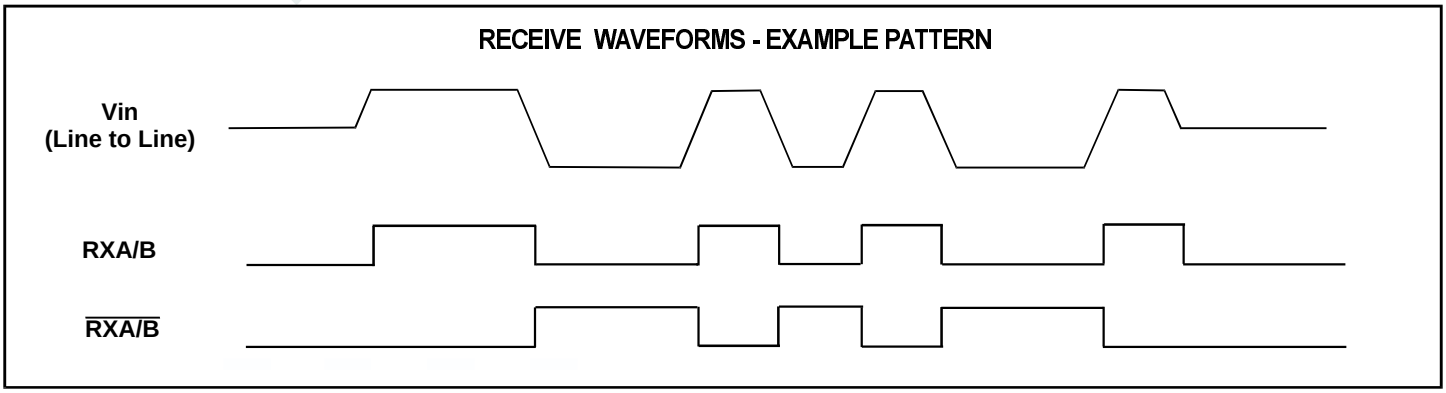


Figure 1. Block Diagram





ABSOLUTE MAXIMUM RATINGS

Supply voltage (VDD)	-0.3 V to +7 V
Logic input voltage range	-0.3 V dc to +5.5 V
Receiver differential voltage	10 Vp-p
Driver peak output current	+1.0 A
Power dissipation at 25°C ceramic DIL, derate	0.5 W 7mW/°C
Solder Temperature	275°C for 10 sec
Storage Temperature	-65°C to +150°C

RECOMMENDED OPERATING CONDITIONS

Supply Voltage

VDD..... 5V... ±5%

Temperature Range

Industrial Screening.....-40°C to +85°C
Hi-Temp Screening.....-55°C to +125°C
Military Screening.....-55°C to +125°C

NOTE: Stresses above absolute maximum ratings or outside recommended operating conditions may cause permanent damage to the device. These are stress ratings only. Operation at the limits is not recommended.

DC ELECTRICAL CHARACTERISTICS

VDD = 5.0V, V_{SS} = 0V, T_A = Operating Temperature Range (unless otherwise specified).

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Operating Voltage	VDD		4.75	5	5.25	V
Total Supply Current	ICC1	Not Transmitting			22	mA
	ICC2	Transmit one channel @ 50% duty cycle		320	340	mA
	ICC3	Transmit one channel @ 100% duty cycle		570	615	mA
Power Dissipation	PD1	Not Transmitting			0.4	W
	PD2	Transmit one channel @ 100% duty cycle			0.95	W
Min. Input Voltage (HI)	V_{IH}	Digital inputs	2.0	1.4		V
Max. Input Voltage (LO)	V_{IL}	Digital inputs		1.4	0.8	V
Min. Input Current (HI)	I_{IH}	V_{IH} = 4.9V, Digital inputs			20	µA
Max. Input Current (LO)	I_{IL}	V_{IL} = 0.1V, Digital inputs	-20			µA
Min. Output Voltage (HI)	V_{OH}	I_{OUT} = -0.4mA, Digital outputs	2.7			V
Max. Output Voltage (LO)	V_{IH}	I_{OUT} = 4.0mA, Digital outputs			0.4	V
RECEIVER (Measured at Point "V_{IN}" in Figure 2)						
Input resistance	Rin	Differential	20			kohm
Input capacitance	Cin	Differential			5	pF
Common mode rejection ratio	CMRR		40			dB
Input Level	Vin	Differential			8	Vp-p
Input common mode voltage	VICM		-5.0		5.0	V-pk
Threshold Voltage	VTH	1 MHz Sine Wave	0.56		1.2	Vp-p
TRANSMITTER (Measured at Point "A" in Figure 2)						
Output Voltage	Vout	35 ohm load	7.0		9.0	Vp-p
		140 ohm load	28.0		36.0	Vp-p
Output Noise	VON	Differential, inhibited			10.0	mVp-p
Output Dynamic Offset Voltage	Vdyn	Across 35 ohm load	-90		90	mV
		Across 140 ohm load	-360		360	mV
Output resistance	Rout	Differential, not transmitting	10			kohm
Output Capacitance	Cout	1 MHz sine wave			15	pF

AC ELECTRICAL CHARACTERISTICS

VCC = 5.0V, VSS = 0V, TA =Operating Temperature Range (unless otherwise specified).

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
RECEIVER (Measured at Point "VIN" in Figure 2)						
Receiver Delay	tDR	From input zero crossing to RXA/B or $\overline{RXA/B}$			450	ns
Receiver Enable Delay	tREN	From RXENA/B rising or falling edge to RXA/B or $\overline{RXA/B}$			40	ns
TRANSMITTER (Measured at Point "A" in Figure 2)						
Driver Delay	tDT	TXA/B, TXA/B to BUSA/B, BUSA/B			150	ns
Rise time	tr	35 ohm load	100		300	ns
Fall Time	tf	35 ohm load	100		300	ns
Inhibit Delay	tDI-H	Inhibited output			100	ns
	tDI-L	Active output			150	ns

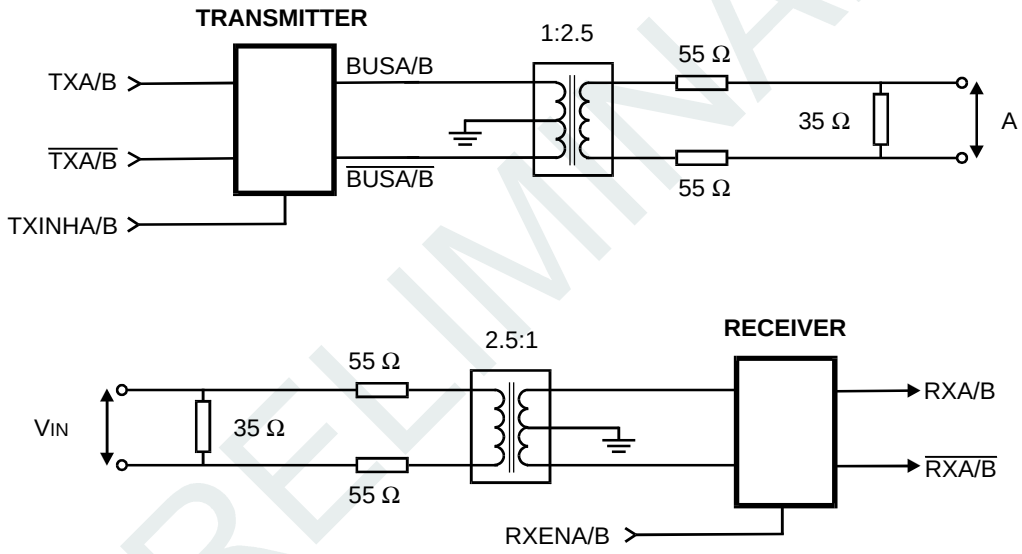


Figure 2. Test circuit

ORDERING INFORMATION

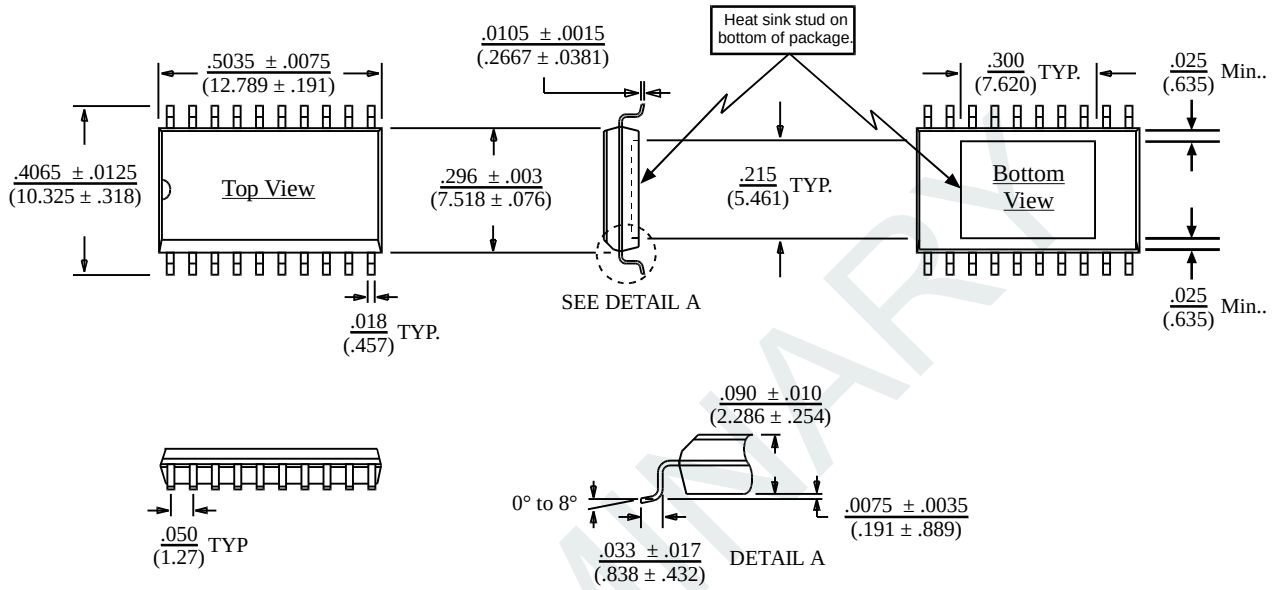
PART NUMBER	IDLE STATE	PACKAGE DESCRIPTION	TEMPERATURE RANGE	PROCESS FLOW	BURN IN	LEAD FINISH
HI-1567PSI	0	20 PIN PLASTIC ESOIC - WB	-40°C TO +85°C	I	NO	SOLDER
HI-1567PST	0	20 PIN PLASTIC ESOIC - WB	-55°C TO +125°C	T	NO	SOLDER
HI-1567CD	0	20 PIN CERAMIC SIDE BRAZED DIP	-40°C TO +85°C	I	NO	GOLD
HI-1567CDT	0	20 PIN CERAMIC SIDE BRAZED DIP	-55°C TO +125°C	T	NO	GOLD
HI-1567CDM	0	20 PIN CERAMIC SIDE BRAZED DIP	-55°C TO +125°C	M	YES	SOLDER
HI-1567CDM-03	0	20 PIN CERAMIC SIDE BRAZED DIP	-55°C TO +125°C	M	YES	SOLDER
HI-1568PSI	1	20 PIN PLASTIC ESOIC - WB	-40°C TO +85°C	I	NO	SOLDER
HI-1568PST	1	20 PIN PLASTIC ESOIC - WB	-55°C TO +125°C	T	NO	SOLDER
HI-1568CDI	1	20 PIN CERAMIC SIDE BRAZED DIP	-40°C TO +85°C	I	NO	GOLD
HI-1568CDT	1	20 PIN CERAMIC SIDE BRAZED DIP	-55°C TO +125°C	T	NO	GOLD
HI-1568CDM	1	20 PIN CERAMIC SIDE BRAZED DIP	-55°C TO +125°C	M	YES	SOLDER
HI-1568CDM-03	1	20 PIN CERAMIC SIDE BRAZED DIP	-55°C TO +125°C	M	YES	SOLDER

Legend: ESOIC - Thermally Enhanced Small Outline Package (SOIC w/built-in heat sink)
WB - Wide Body

20-PIN PLASTIC SMALL OUTLINE (ESOIC) - WB

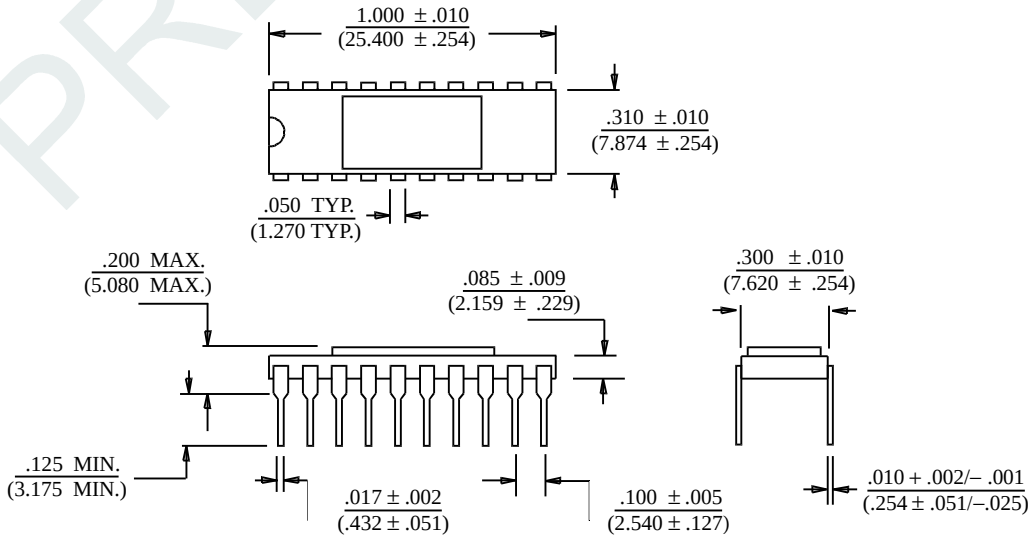
(Wide Body, Thermally Enhanced)

Package Type: 24HEW



20-PIN CERAMIC SIDE-BRAZED DIP

PACKAGE TYPE: 20C



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