

Half Amp Full Bridge Power Driver for Small 3V, 5V and 12V DC Motors

June 1997

Features

- Two Independent Controlled Complementary MOS Power Output Half H-Drivers (Full-Bridge) for Nominal 3V to 12V Power Supply Operation
- Split \pm Voltage Power Supply Option for Output Drivers
- Load Switching Capabilities to 0.5A
- Single Supply Range +2.5V to +15V
- Low Standby Current
- CMOS/TTL Compatible Input Logic
- Over-Temperature Shutdown Protection
- Over-Current Limit Protection
- Over-Current Fault Flag Output
- Direction, Braking and PWM Control

Applications

- DC Motor Driver
- Relay and Solenoid Drivers
- Stepper Motor Controller
- Air Core Gauge Instrument Driver
- Speedometer Displays
- Tachometer Displays
- Remote Power Switch
- Battery Operated Switch Circuits
- Logic and Microcontroller Operated Switch

Description

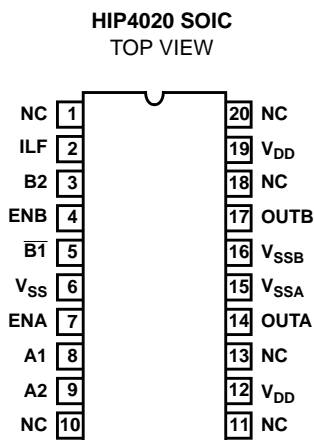
In the Functional Block Diagram of the HIP4020, the four switches and a load are arranged in an H-Configuration so that the drive voltage from terminals OUTA and OUTB can be cross-switched to change the direction of current flow in the load. This is commonly known as 4-quadrant load control. As shown in the Block Diagram, switches Q1 and Q4 are conducting or in an ON state when current flows from V_{DD} through Q1 to the load, and then through Q4 to terminal V_{SSB} ; where load terminal OUTA is at a positive potential with respect to OUTB. Switches Q1 and Q4 are operated synchronously by the control logic. The control logic switches Q3 and Q2 to an open or OFF state when Q1 and Q4 are switched ON. To reverse the current flow in the load, the switch states are reversed where Q1 and Q4 are OFF while Q2 and Q3 are ON. Consequently, current then flows from V_{DD} through Q3, through the load, and through Q2 to terminal V_{SSA} , and load terminal OUTB is then at a positive potential with respect to OUTA.

Terminals ENA and ENB are ENABLE Inputs for the Logic A and B Input Controls. The ILF output is an Over-Current Limit Fault Flag Output and indicates a fault condition for either Output A or B or both. The V_{DD} and V_{SS} are the Power Supply reference terminals for the A and B Control Logic Inputs and ILF Output. While the V_{DD} positive power supply terminal is internally connected to each bridge driver, the V_{SSA} and V_{SSB} Power Supply terminals are separate and independent from V_{SS} and may be more negative than the V_{SS} ground reference terminal. The use of level shifters in the gate drive circuitry to the NMOS (low-side) output stages allows controlled level shifting of the output drive relative to ground.

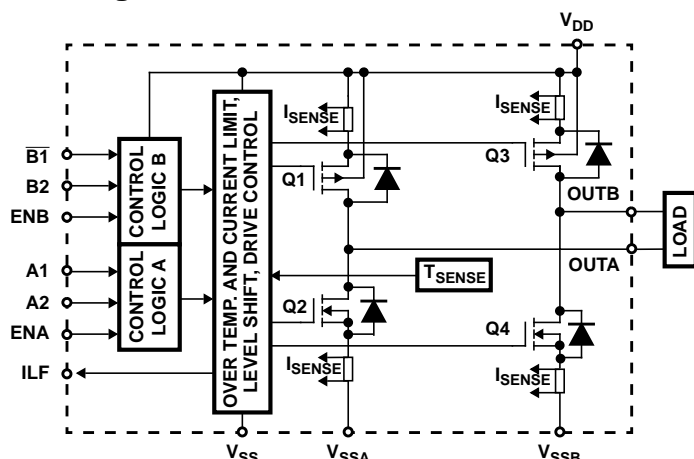
Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HIP4020IB	-40 to 85	20 Ld SOIC	M20.3

Pinout



Block Diagram



HIP4020

Absolute Maximum Ratings

Supply Voltage; V_{DD} to V_{SS} or V_{SSA} or V_{SSB} +15V
 Neg. Output Supply Voltage, (V_{SSA} , V_{SSB}) (Note 1)
 DC Logic Input Voltage (Each Input) ... ($V_{SS} - 0.5V$) to ($V_{DD} + 0.5V$)
 DC Logic Input Current (Each Input) $\pm 15mA$
 ILF Fault Output Current $\pm 15mA$
 Output Load Current, (Self Limiting, See Elec. Spec.) $\pm I_{O(LIMIT)}$

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA}
 Plastic SOIC Package 105°C/W
 Maximum Storage Temperature Range -65°C to 150°C
 Maximum Junction Temperature 150°C
 Maximum Lead Temperature (Soldering 10s) 300°C
 (Lead Tips Only)

Operating Conditions $T_A = 25^\circ C$

Typical Operating Supply Voltage Range, V_{DD} +3 to +12V
 Low Voltage Logic Retention, Min. V_{DD} +2V
 Idle Supply Current; No Load, $V_{DD} = +5V$ 0.8mA
 Typical P+N Channel $r_{DS(ON)}$, $V_{DD} = +5V$, 0.5A Load 2 Ω

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications $T_A = 25^\circ C$, $V_{DD} = +5V$, $V_{SSA} = V_{SSB} = V_{SS} = 0V$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Leakage Current	I_{LEAK}	$V_{DD} = +15V$	-	-	25	nA
Low Level Input Voltage	V_{IL}		V_{SS}	-	0.8	V
High Level Input Voltage	V_{IH}		2	-	V_{DD}	V
ILF Output Low, Sink Current	I_{OH}	$V_{OUT} = 0.4V$, $V_{DD} = +12V$	15	-	-	mA
ILF Output High, Source Current	I_{OL}	$V_{OUT} = 11.6V$, $V_{DD} = +12V$	-	-	-15	mA
Input Capacitance	C_{IN}		-	2	-	pF
P-Channel $r_{DS(ON)}$, Low Supply Voltage	$r_{DS(ON)}$	$V_{DD} = +3V$, $I_{SOURCE} = 250mA$	-	1.6	2.1	Ω
N-Channel $r_{DS(ON)}$, Low Supply Voltage	$r_{DS(ON)}$	$V_{DD} = +3V$, $I_{SINK} = 250mA$	-	1	1.5	Ω
P-Channel $r_{DS(ON)}$, High Supply Voltage	$r_{DS(ON)}$	$V_{DD} = +12V$, $I_{SOURCE} = 400mA$	-	0.6	1.2	Ω
N-Channel $r_{DS(ON)}$, High Supply Voltage	$r_{DS(ON)}$	$V_{DD} = +12V$, $I_{SINK} = 400mA$	-	0.5	1.1	Ω
OUTA, OUTB Source Current Limiting	$I_{O(LIMIT)}$	$V_{DD} = +6V$, $V_{SS} = 0V$, $V_{SSA} = V_{SSB} = -6V$	480	625	1500	mA
OUTA, OUTB Sink Current Limiting	$-I_{O(LIMIT)}$	$V_{DD} = +6V$, $V_{SS} = 0V$, $V_{SSA} = V_{SSB} = -6V$	480	800	1500	mA
Idle Supply Current; No Load	I_{DD}		-	0.8	1.5	mA
OUTA, OUTB Voltage High	V_{OH}	$I_{SOURCE} = 450mA$	4.2	4.5	-	V
OUTA, OUTB Voltage Low	V_{OL}	$I_{SINK} = 450mA$	-	0.4	0.6	V
OUTA, OUTB Voltage High	V_{OH}	$V_{DD} = +3V$, $I_{SOURCE} = 250mA$	2.415	2.6	-	V
OUTA, OUTB Voltage Low	V_{OL}	$V_{DD} = +3V$, $I_{SINK} = 250mA$	-	0.25	0.375	V
OUTA, OUTB Source Current Limiting	$I_{O(LIMIT)}$	$V_{DD} = +12V$	480	625	1500	mA
OUTA, OUTB Sink Current Limiting	$-I_{O(LIMIT)}$	$V_{DD} = +12V$	480	800	1500	mA
OUTA, OUTB Source Current Limiting	$I_{O(LIMIT)}$	$V_{DD} = +3V$	480	625	1500	mA
OUTA, OUTB Sink Current Limiting	$-I_{O(LIMIT)}$	$V_{DD} = +3V$	480	800	1500	mA
Thermal Shutdown	T_{SD}		-	145	-	$^\circ C$

HIP4020

Electrical Specifications $T_A = 25^\circ\text{C}$, $V_{DD} = +5\text{V}$, $V_{SSA} = V_{SSB} = V_{SS} = 0\text{V}$, Unless Otherwise Specified (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Response Time: V_{EN} to V_{OUT}		$I_O = 0.5\text{A}$ (Note 2)				
Turn-On: Prop Delay	t_{PLH}		-	2.5	-	μs
Rise Time	t_r		-	4	-	μs
Turn-Off: Prop Delay	t_{PHL}		-	0.1	-	μs
Fall Time	t_f		-	0.1	-	μs

NOTES:

- V_{SS} is the required common ground reference for the logic input switching. The load currents may be switched positive and negative in reference to the V_{SS} common ground by using a split supply for V_{DD} (positive) to V_{SSA} and V_{SSB} (negative). For an uneven split in the supply voltage, the Maximum Negative Output Supply Voltage for V_{SSA} and V_{SSB} is limited by the Maximum V_{DD} to V_{SSA} or V_{SSB} ratings. Since the V_{DD} pins are internally tied together, the voltage on each V_{DD} pins must be equal and common.
- Refer to the Truth Table and the V_{EN} to V_{OUT} Switching Waveforms. Current, I_O refers to I_{OUTA} or I_{OUTB} as the Output Load current. Note that ENA controls OUTA and ENB controls OUTB. Each Half H-Switch has independent control from the respective A1, A2, ENA or $\overline{B1}$, B2, ENB inputs. Refer to the Terminal Information Table for external pin connections to establish mode control switching. Figure 1 shows a typical application circuit used to control a DC Motor.

Pin Descriptions

PIN NUMBER	SYMBOL	DESCRIPTION
12, 19	V_{DD}	Positive Power Supply pins; internally common and externally connect to the same Positive Supply (V+).
15	V_{SSA}	Negative Power Supply pin; Negative or Ground return for Switch Driver A; externally connect to the Supply (V-).
16	V_{SSB}	Negative Power Supply pin; Negative or Ground return for Switch Driver B; externally connect to the Supply (V-).
6	V_{SS}	Common Ground pin for the Input Logic Control circuits. May be used as a common ground with V_{SSA} and V_{SSB} .
8, 5	A1, $\overline{B1}$	Input pins used to control the direction of output load current to/from OUTA and OUTB, respectively. When connected, A1 and $\overline{B1}$ can be controlled from the same logic signal to change the directional rotation of a motor.
9, 3	A2, B2	Input pins used to force a low state on OUTA and OUTB, respectively. When connected, A2 and B2 can be controlled from the same logic signal to activate Dynamic Braking of a motor.
7, 4	ENA, ENB	Input pins used to Enable Switch Driver A and Switch Driver B, respectively. When Low, the respective output is in a high impedance (Z) off-state. Since each Switch Driver is independently controlled, OUTA and OUTB may be a separately PWM controlled as Half H-Switch Drivers.
14, 17	OUTA, OUTB	Respectively, Switch Driver A and Switch Driver B Output pins.
2	ILF	Current Limiting Fault Output Flag pin; when in a high logic state, signifies that Switch Driver A or B or both are in a Current Limiting Fault Mode.

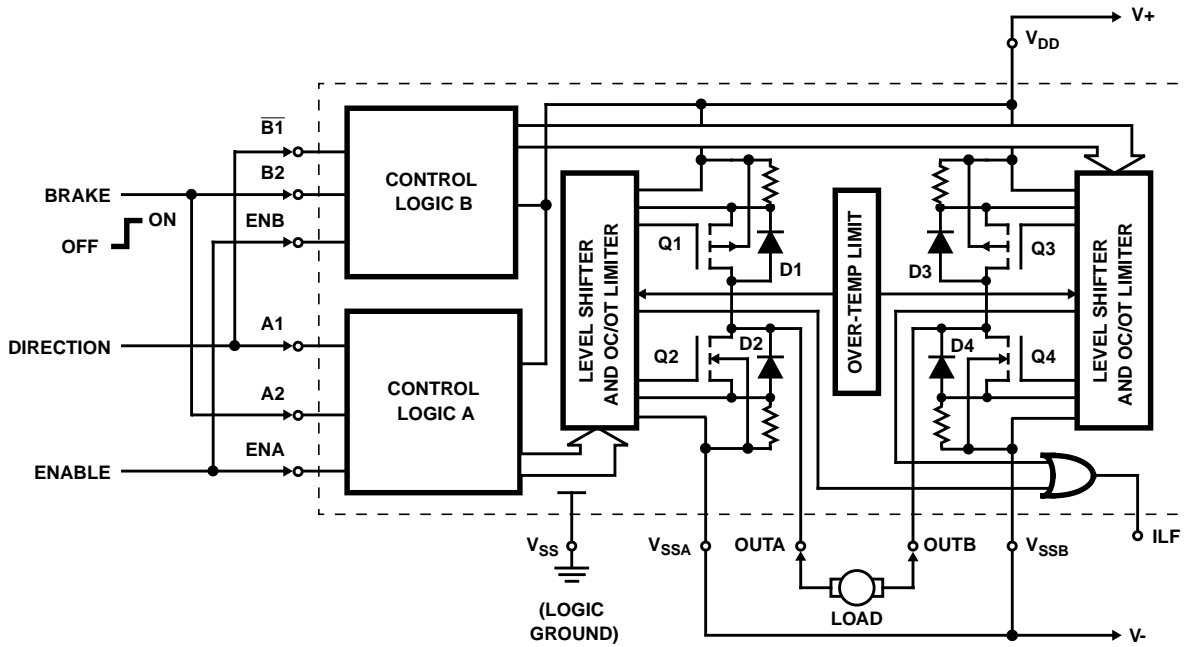
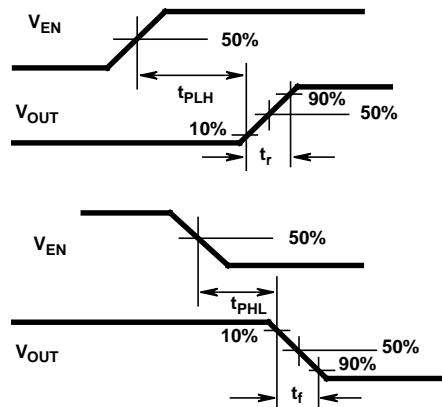


FIGURE 1. TYPICAL MOTOR CONTROL APPLICATION CIRCUIT SHOWING DIRECTIONAL AND BRAKING CONTROL

TRUTH TABLE

SWITCH DRIVER A			SWITCH DRIVER B				
INPUTS			OUTPUT	INPUTS			OUTPUT
A1	A2	ENA	OUTA	$\overline{B1}$	B2	ENB	OUTB
H	L	H	OH	L	L	H	OH
L	L	H	OL	H	L	H	OL
H	H	H	OL	L	H	H	OL
L	H	H	OL	H	H	H	OL
X	X	L	Z	X	X	L	Z

L = Low logic level; H = High logic level
 Z = High Impedance (off state)
 OH = Output High (sourcing current to the output terminal)
 OL = Output Low (sinking current from the output terminal)
 X = Don't Care



SWITCHING WAVEFORMS

FIGURE 2.

Application

The HIP4020 is designed to detect load current feedback from sampling resistors of low value in the source connections of the output drivers to V_{DD} , V_{SSA} and V_{SSB} (See Figure 1). When the sink or source current at OUTA or OUTB exceeds the preset OC (Over-Current) limiting value of 550mA typical, the current is held at the limiting value. If the OT (Over-Temperature) Shutdown Protection limit is exceeded, temperature sensing BiMOS circuits limit the junction temperature to 150°C typical.

The circuit of Figure 1 shows the Full H-Switch in a small motor-drive application. The left (A) and right (B) H-Switch's are controlled from the A and B inputs via the A and B CONTROL LOGIC to the MOS output transistors Q1, Q2, Q3 and Q4. The circuit is intended to safely start, stop, and control rotational direction for a motor requiring no more than 0.5A of supply current. The stop function includes a Dynamic Braking feature.

With the ENABLE Inputs Low, the MOS transistors Q1 and Q3 are OFF; which cuts-off supply current to OUTA and OUTB. With the BRAKE terminal Low and ENABLE Inputs High, either Q1 and Q4 or Q3 and Q2 will be driven into conduction by the DIRECTION Input Control terminal. The MOS output transistor pair chosen for conduction is determined by the logic level applied to the DIRECTION control; resulting in either clockwise (CW) or counter-clockwise (CCW) shaft rotation.

When the BRAKE terminal is switched high (while holding the ENABLE input high), the gates of both Q2 and Q4 are driven high. Current flowing through Q2 (from the motor terminal OUTA) at the moment of Dynamic Braking will continue to flow through Q2 to the V_{SSA} and V_{SSB} external connection, and then continue through diode D4 to the motor terminal OUTB. As such, the resistance of the motor winding (and the series-connected path) dissipates the kinetic energy stored in the system. Reversing rotation, current

flowing through Q4 (from the motor terminal OUTB), at the moment of Dynamic Braking, would continue to flow through Q4 to the V_{SSB} and V_{SSA} tie, and then continue through diode D2 to the motor terminal OUTA, to dissipate the stored kinetic energy as previously described.

Where V_{DD} to V_{SS} are the Power Supply reference terminals for the Control Logic, the lowest practical supply voltage for proper logic control should be no less than 2.0V. The V_{SSA} and V_{SSB} terminals are separate and independent from V_{SS} and may be more negative than the V_{SS} ground reference terminal. However, the maximum supply level from V_{DD} to V_{SSA} or V_{SSB} must not be greater than the Absolute Maximum Supply Voltage rating.

Terminals A1, $\overline{B1}$, A2, B2, ENA and ENB are internally connected to protection circuits intended to guard the CMOS gate-oxides against damage due to electrostatic discharge. (See Figure 3) Inputs ENA, ENB, A1, $\overline{B1}$, A2 and B2 have CD74HCT4000 Logic Interface Protection and Level Converters for TTL or CMOS Input Logic. These inputs are designed to typically provide ESD protection up to 2kV. However, these devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

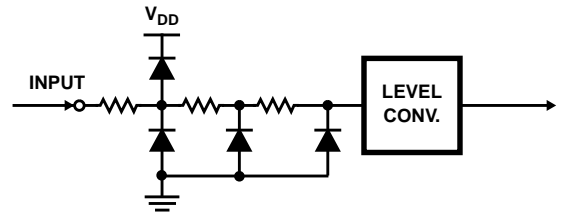


FIGURE 3. LOGIC INPUT ESD INTERFACE PROTECTION

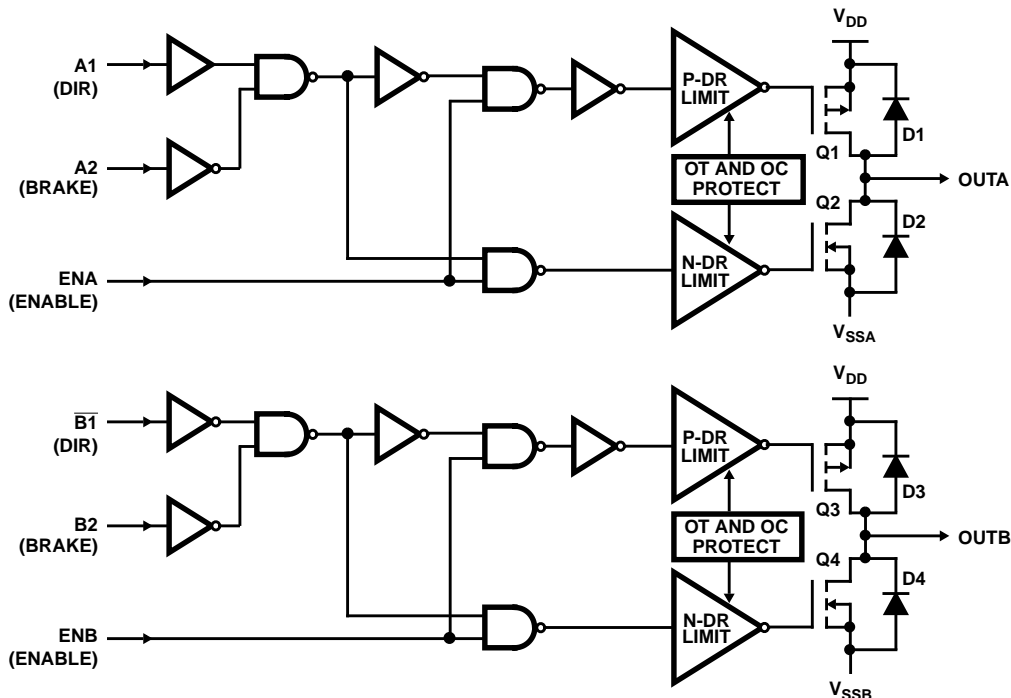


FIGURE 4. EQUIVALENT CONTROL LOGIC A AND B SHOWN DRIVING THE OUTA AND OUTB OUTPUT DRIVERS

Typical Performance Curves

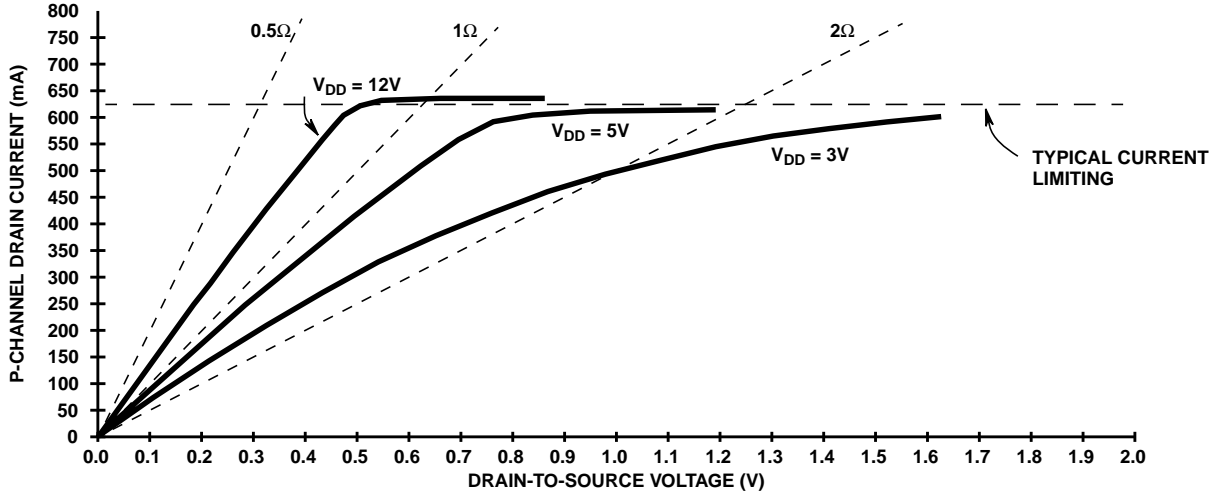


FIGURE 5. TYPICAL CHARACTERISTIC OF THE P-MOSFET OUTPUT DRIVER DRAIN CURRENT vs DRAIN-TO-SOURCE VOLTAGE, $T_{AMBIENT} = 25^{\circ}C$

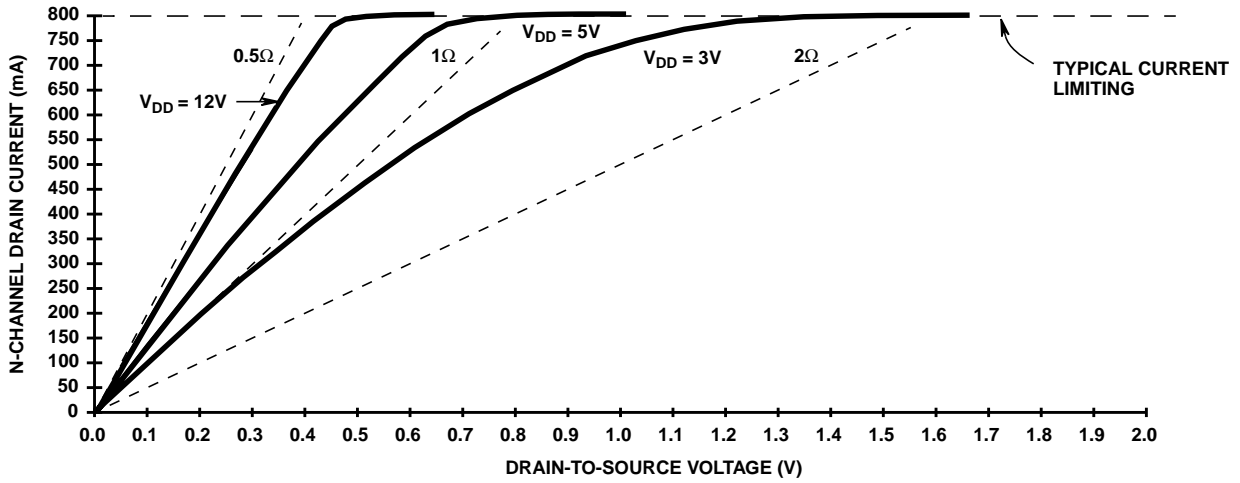


FIGURE 6. TYPICAL CHARACTERISTIC OF THE N-MOSFET OUTPUT DRIVER DRAIN CURRENT vs DRAIN-TO-SOURCE VOLTAGE, $T_{AMBIENT} = 25^{\circ}C$

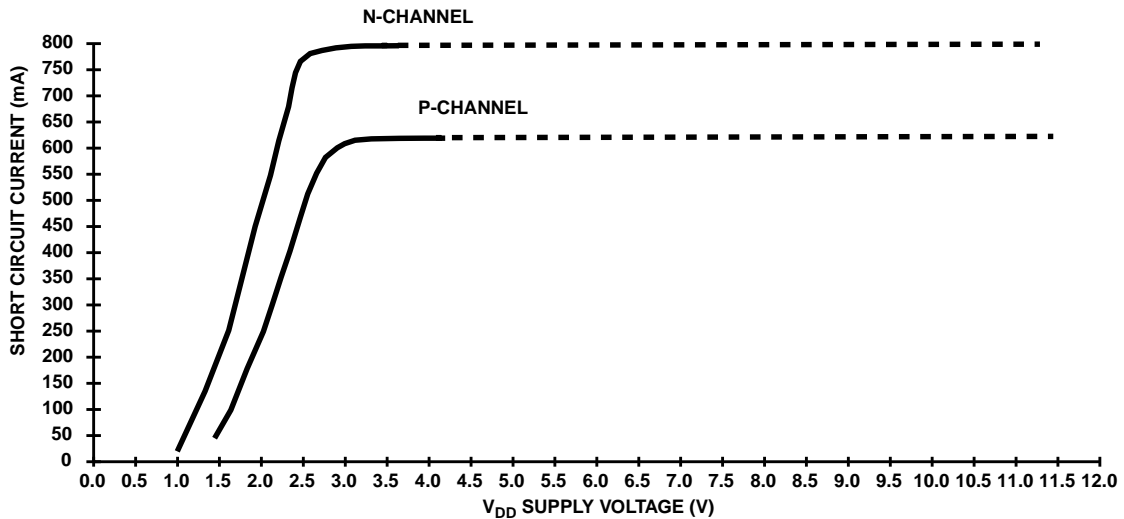


FIGURE 7. TYPICAL CHARACTERISTIC OF THE P AND N OUTPUT DRIVER SHORT CIRCUIT CURRENT vs SUPPLY VOLTAGE, $T_{AMBIENT} = 25^{\circ}C$

Typical Performance Curves (Continued)

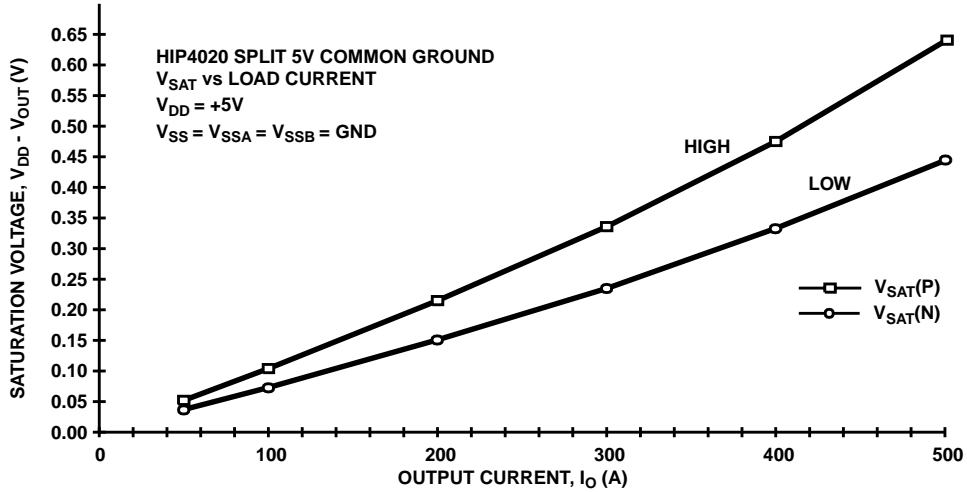


FIGURE 8. TYPICAL CHARACTERISTIC OF SATURATION VOLTAGE vs OUTPUT CURRENT USING A +5V SUPPLY, $T_{AMBIENT} = 25^{\circ}C$

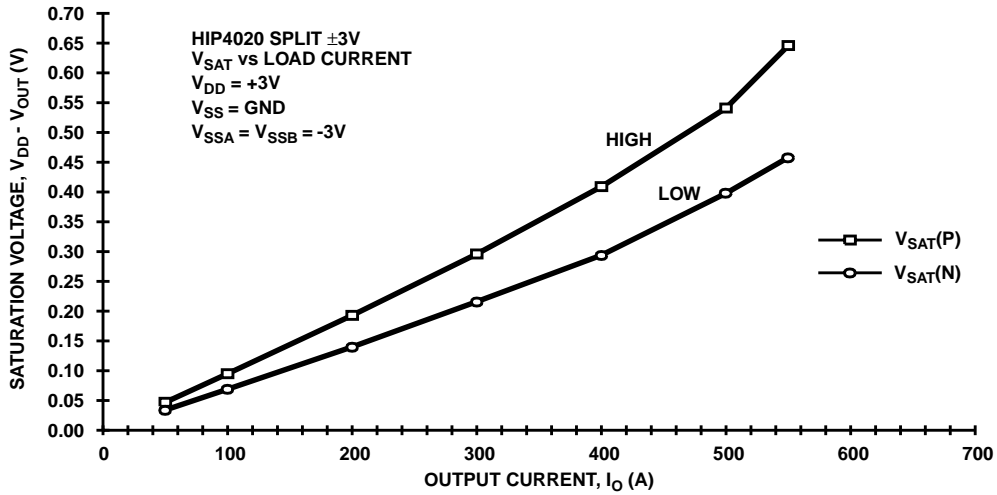


FIGURE 9. TYPICAL CHARACTERISTIC OF SATURATION VOLTAGE vs OUTPUT CURRENT USING A ±3V SPLIT SUPPLY, OUTPUT REFERENCE EQUAL LOGIC GROUND, $T_{AMBIENT} = 25^{\circ}C$

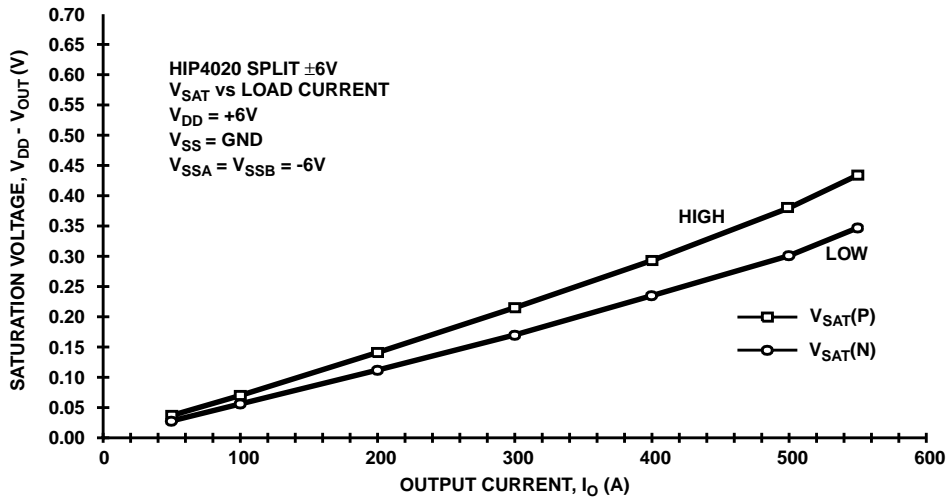
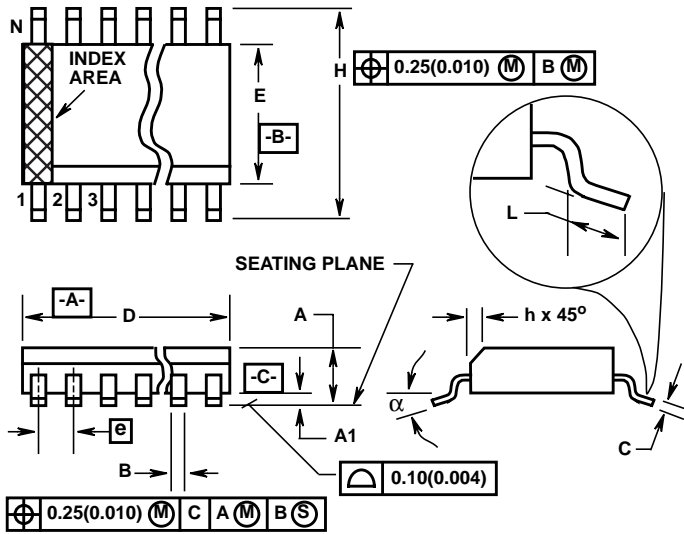


FIGURE 10. TYPICAL CHARACTERISTIC OF SATURATION VOLTAGE vs OUTPUT CURRENT USING A ±6V SPLIT SUPPLY, OUTPUT REFERENCE EQUAL LOGIC GROUND, $T_{AMBIENT} = 25^{\circ}C$

Small Outline Plastic Packages (SOIC)



**M20.3 (JEDEC MS-013-AC ISSUE C)
20 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE**

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.4961	0.5118	12.60	13.00	3
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	20		20		7
alpha	0°	8°	0°	8°	-

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Rev. 0 12/93

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