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April 1, 2003

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# HM62V8512C Series

4 M SRAM (512-kword × 8-bit)



ADE-203-1210D (Z)  
Rev. 4.0  
Aug. 5, 2002

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## Description

The Hitachi HM62V8512C is a 4-Mbit static RAM organized 512-kword × 8-bit. It realizes higher density, higher performance and low power consumption by employing CMOS process technology (6-transistor memory cell). The device, packaged in a 525-mil SOP (foot print pitch width) or 400-mil TSOP TYPE II is available for high density mounting. The HM62V8512C is suitable for battery backup system.

## Features

- Single 3.0 V supply: 2.7 V to 3.6 V
- Access time: 55 ns (max)
- Power dissipation
  - Active: 6.0 mW/MHz (typ)
  - Standby: 2.4  $\mu$ W (typ)
- Completely static memory. No clock or timing strobe required
- Equal access and cycle times
- Common data input and output: Three state output
- Directly LV-TTL compatible: All inputs
- Battery backup operation

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## HM62V8512C Series

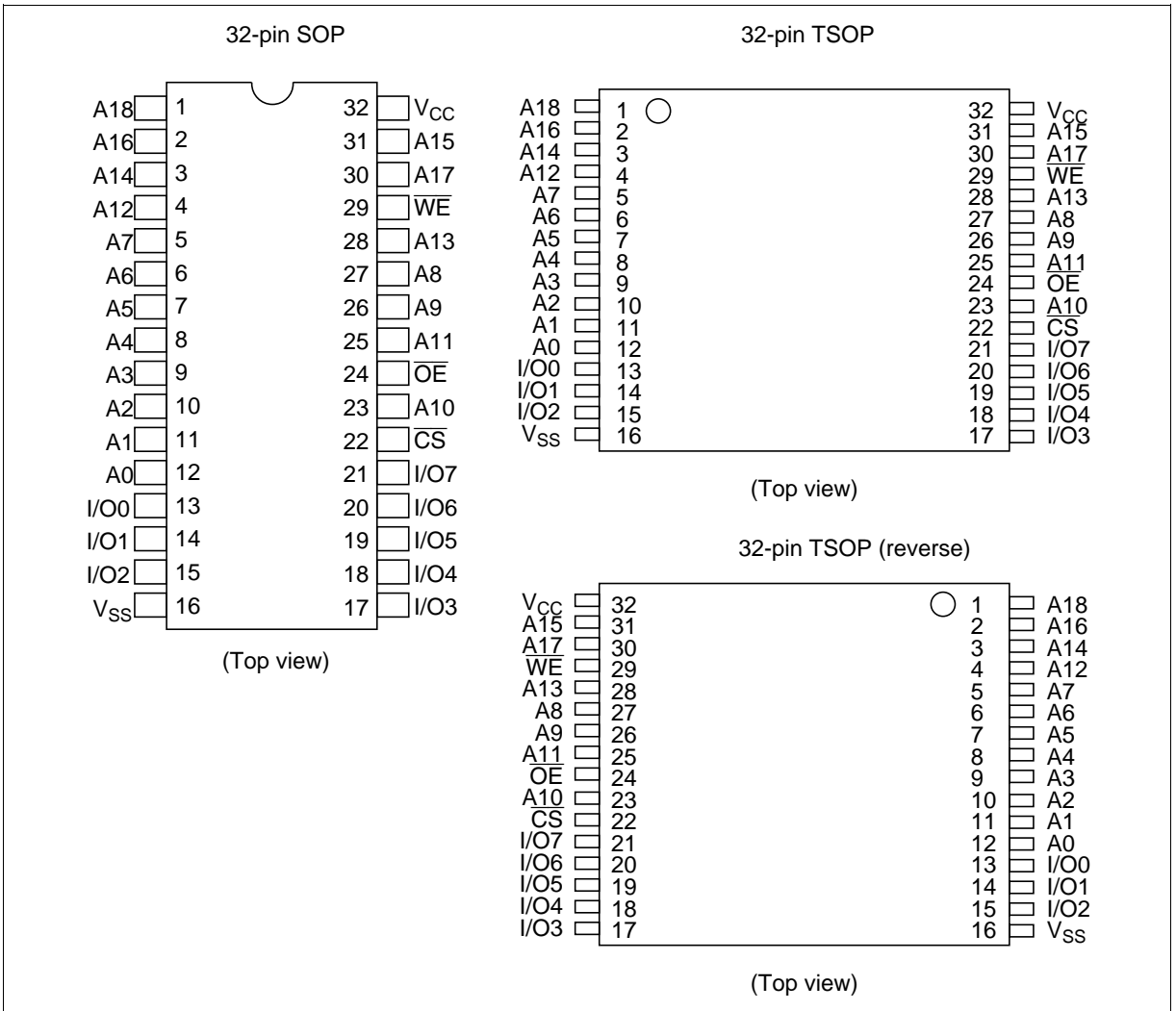
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### Ordering Information

Type No.	Access time	Package
HM62V8512CLFP-5	55 ns	525-mil 32-pin plastic SOP (FP-32D)
HM62V8512CLFP-5SL	55 ns	
HM62V8512CLTT-5	55 ns	400-mil 32-pin plastic TSOP II (TTP-32D)
HM62V8512CLTT-5SL	55 ns	
HM62V8512CLRR-5	55 ns	400-mil 32-pin plastic TSOP II reverse (TTP-32DR)
HM62V8512CLRR-5SL	55 ns	

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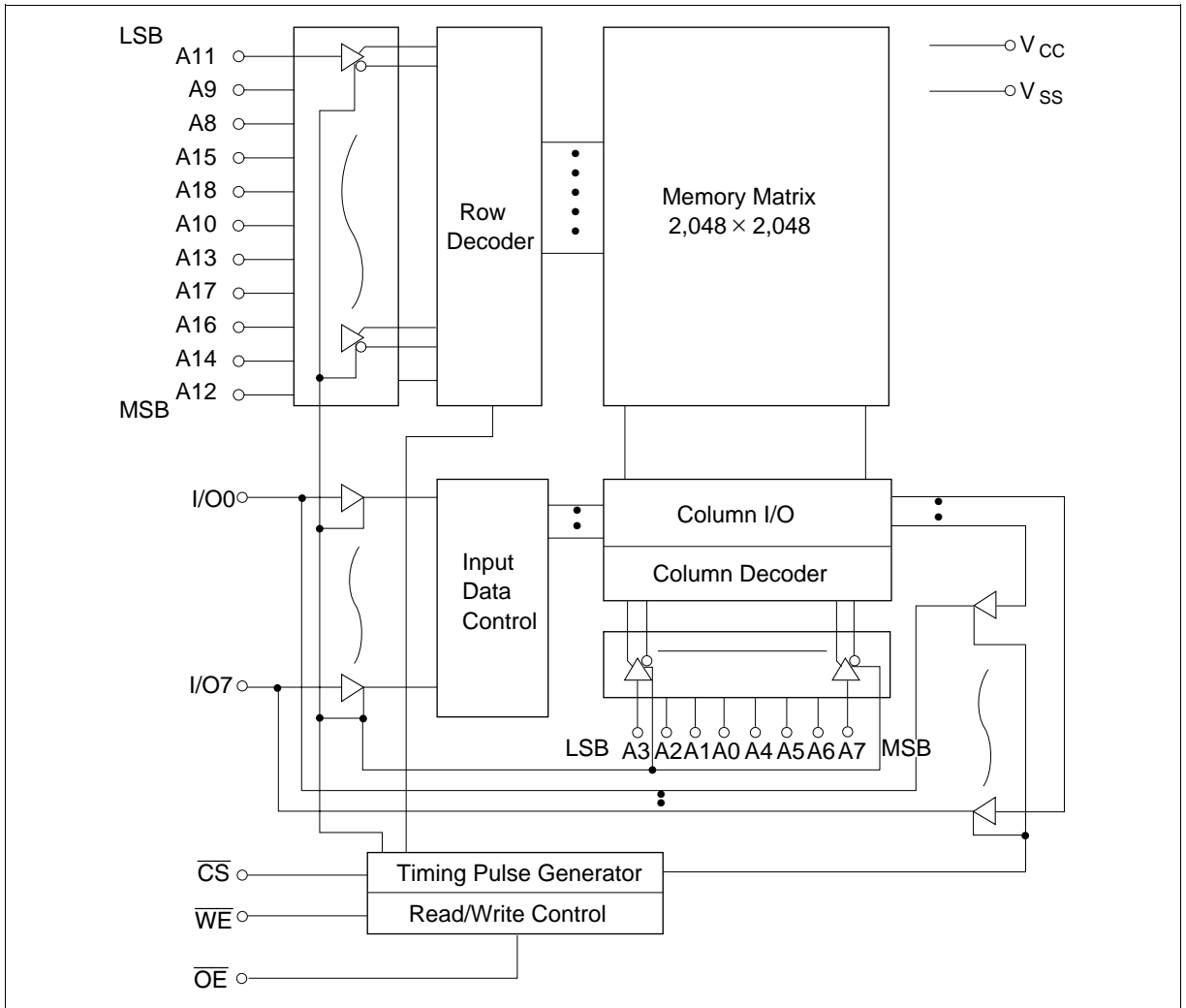
Pin Arrangement



Pin Description

Pin name	Function
A0 to A18	Address input
I/O0 to I/O7	Data input/output
CS	Chip select
OE	Output enable
WE	Write enable
V <sub>CC</sub>	Power supply
V <sub>SS</sub>	Ground

## Block Diagram



**Function Table**

$\overline{WE}$	$\overline{CS}$	$\overline{OE}$	Mode	$V_{CC}$ current	Dout pin	Ref. cycle
x	H	x	Not selected	$I_{SB}, I_{SB1}$	High-Z	—
H	L	H	Output disable	$I_{CC}$	High-Z	—
H	L	L	Read	$I_{CC}$	Dout	Read cycle
L	L	H	Write	$I_{CC}$	Din	Write cycle (1)
L	L	L	Write	$I_{CC}$	Din	Write cycle (2)

Note: x: H or L

**Absolute Maximum Ratings**

Parameter	Symbol	Value	Unit
Power supply voltage	$V_{CC}$	-0.5 to +4.6	V
Voltage on any pin relative to $V_{SS}$	$V_T$	-0.5* <sup>1</sup> to $V_{CC} + 0.5$ * <sup>2</sup>	V
Power dissipation	$P_T$	1.0	W
Operating temperature	$T_{opr}$	-20 to +70	°C
Storage temperature	$T_{stg}$	-55 to +125	°C
Storage temperature under bias	$T_{bias}$	-20 to +85	°C

Notes: 1.  $V_T$  min: -3.0 V for pulse half-width  $\leq$  30 ns.

2. Maximum voltage is 4.6 V.

**Recommended DC Operating Conditions ( $T_a = -20$  to  $+70^\circ\text{C}$ )**

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	$V_{CC}$	2.7	3.0	3.6	V
	$V_{SS}$	0	0	0	V
Input high voltage	$V_{IH}$	2.0	—	$V_{CC} + 0.3$	V
Input low voltage	$V_{IL}$	-0.3* <sup>1</sup>	—	0.8	V

Note: 1.  $V_{IL}$  min: -3.0 V for pulse half-width  $\leq$  30 ns.

## DC Characteristics

Parameter	Symbol	Min	Typ* <sup>1</sup>	Max	Unit	Test conditions
Input leakage current	$ I_{Li} $	—	—	1	$\mu\text{A}$	$V_{in} = V_{SS}$ to $V_{CC}$
Output leakage current	$ I_{Lo} $	—	—	1	$\mu\text{A}$	$\overline{CS} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$ , $V_{IO} = V_{SS}$ to $V_{CC}$
Operating power supply current: DC	$I_{CC}$	—	5	10	mA	$\overline{CS} = V_{IL}$ , others = $V_{IH}/V_{IL}$ , $I_{IO} = 0$ mA
Operating power supply current	$I_{CC1}$	—	8	25	mA	Min cycle, duty = 100% $\overline{CS} = V_{IL}$ , others = $V_{IH}/V_{IL}$ , $I_{IO} = 0$ mA
	$I_{CC2}$	—	2	5	mA	Cycle time = 1 $\mu\text{s}$ , duty = 100% $I_{IO} = 0$ mA, $\overline{CS} \leq 0.2$ V $V_{IH} \geq V_{CC} - 0.2$ V, $V_{IL} \leq 0.2$ V
Standby power supply current: DC	$I_{SB}$	—	0.1	0.3	mA	$\overline{CS} = V_{IH}$
Standby power supply current (1): DC	$I_{SB1}$	—	0.5* <sup>2</sup>	20* <sup>2</sup>	$\mu\text{A}$	$V_{in} \geq 0$ V, $\overline{CS} \geq V_{CC} - 0.2$ V
			0.5* <sup>3</sup>	10* <sup>3</sup>	$\mu\text{A}$	
Output low voltage	$V_{OL}$	—	—	0.4	V	$I_{OL} = 2.1$ mA
				0.2	V	$I_{OL} = 100$ $\mu\text{A}$
Output high voltage	$V_{OH}$	$V_{CC} - 0.2$	—	—	V	$I_{OH} = -100$ $\mu\text{A}$
					2.4	V

Notes: 1. Typical values are at  $V_{CC} = 3.0$  V,  $T_a = +25^\circ\text{C}$  and specified loading, and not guaranteed.

2. This characteristics is guaranteed only for L version.

3. This characteristics is guaranteed only for L-SL version.

## Capacitance ( $T_a = +25^\circ\text{C}$ , $f = 1$ MHz)

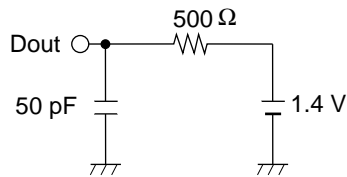
Parameter	Symbol	Typ	Max	Unit	Test conditions
Input capacitance* <sup>1</sup>	$C_{in}$	—	8	pF	$V_{in} = 0$ V
Input/output capacitance* <sup>1</sup>	$C_{IO}$	—	10	pF	$V_{IO} = 0$ V

Note: 1. This parameter is sampled and not 100% tested.

**AC Characteristics** ( $T_a = -20$  to  $+70^\circ\text{C}$ ,  $V_{CC} = 2.7$  V to 3.6 V, unless otherwise noted.)

**Test Conditions**

- Input pulse levels: 0.4 V to 2.4 V
- Input rise and fall time: 5 ns
- Input timing reference levels: 1.4 V
- Output timing reference level: 1.4 V/1.4 V
- Output load: See figure (Including scope & jig)



**Read Cycle**

Parameter	Symbol	HM62V8512C		Unit	Notes
		Min	Max		
Read cycle time	$t_{RC}$	55	—	ns	
Address access time	$t_{AA}$	—	55	ns	
Chip select access time	$t_{CO}$	—	55	ns	
Output enable to output valid	$t_{OE}$	—	30	ns	
Chip selection to output in low-Z	$t_{LZ}$	10	—	ns	2
Output enable to output in low-Z	$t_{OLZ}$	5	—	ns	2
Chip deselection to output in high-Z	$t_{HZ}$	0	20	ns	1, 2
Output disable to output in high-Z	$t_{OHZ}$	0	20	ns	1, 2
Output hold from address change	$t_{OH}$	10	—	ns	

## Write Cycle

Parameter	Symbol	HM62V8512C		Unit	Notes
		-5			
		Min	Max		
Write cycle time	$t_{WC}$	55	—	ns	
Chip selection to end of write	$t_{CW}$	50	—	ns	4
Address setup time	$t_{AS}$	0	—	ns	5
Address valid to end of write	$t_{AW}$	50	—	ns	
Write pulse width	$t_{WP}$	40	—	ns	3, 12
Write recovery time	$t_{WR}$	0	—	ns	6
$\overline{WE}$ to output in high-Z	$t_{WHZ}$	0	20	ns	1, 2, 7
Data to write time overlap	$t_{DW}$	25	—	ns	
Data hold from write time	$t_{DH}$	0	—	ns	
Output active from output in high-Z	$t_{OW}$	5	—	ns	2
Output disable to output in high-Z	$t_{OHZ}$	0	20	ns	1, 2, 7

Notes: 1.  $t_{HZ}$ ,  $t_{OHZ}$  and  $t_{WHZ}$  are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.

2. This parameter is sampled and not 100% tested.

3. A write occurs during the overlap ( $t_{WP}$ ) of a low  $\overline{CS}$  and a low  $\overline{WE}$ . A write begins at the later transition of  $\overline{CS}$  going low or  $\overline{WE}$  going low. A write ends at the earlier transition of  $\overline{CS}$  going high or  $\overline{WE}$  going high.  $t_{WP}$  is measured from the beginning of write to the end of write.

4.  $t_{CW}$  is measured from  $\overline{CS}$  going low to the end of write.

5.  $t_{AS}$  is measured from the address valid to the beginning of write.

6.  $t_{WR}$  is measured from the earlier of  $\overline{WE}$  or  $\overline{CS}$  going high to the end of write cycle.

7. During this period, I/O pins are in the output state so that the input signals of the opposite phase to the outputs must not be applied.

8. If the  $\overline{CS}$  low transition occurs simultaneously with the  $\overline{WE}$  low transition or after the  $\overline{WE}$  transition, the output remain in a high impedance state.

9.  $Dout$  is the same phase of the write data of this write cycle.

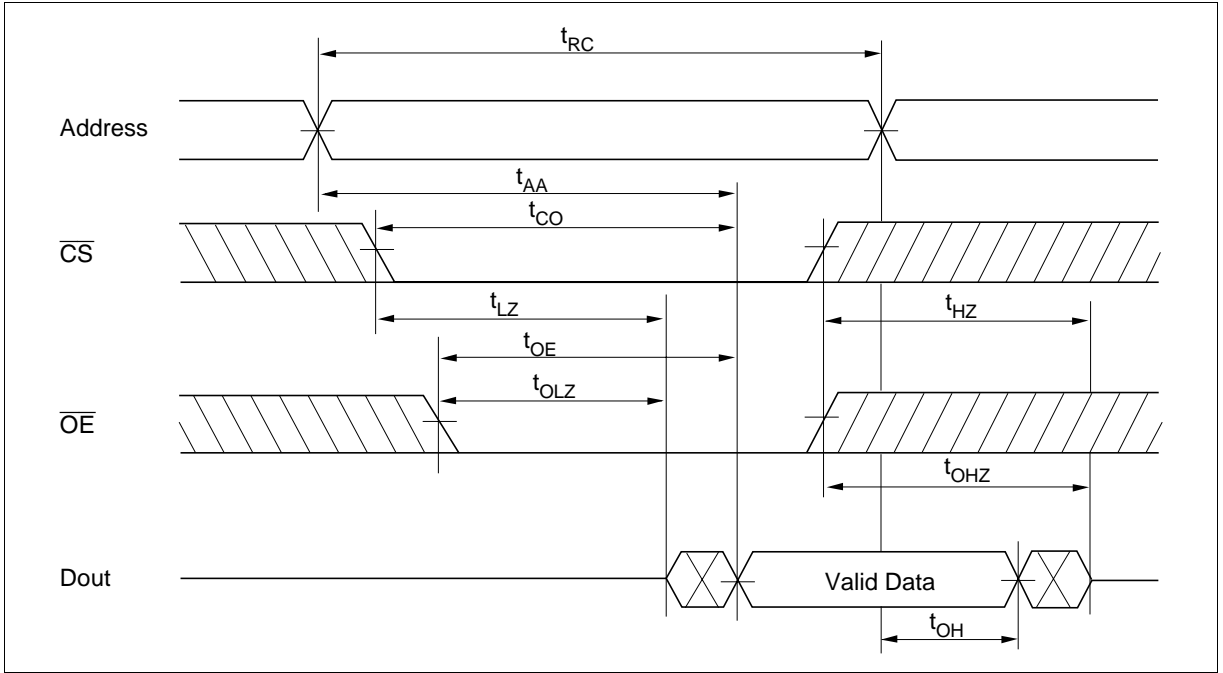
10.  $Dout$  is the read data of next address.

11. If  $\overline{CS}$  is low during this period, I/O pins are in the output state. Therefore, the input signals of the opposite phase to the outputs must not be applied to them.

12. In the write cycle with  $\overline{OE}$  low fixed,  $t_{WP}$  must satisfy the following equation to avoid a problem of data bus contention.  $t_{WP} \geq t_{DW} \text{ min} + t_{WHZ} \text{ max}$

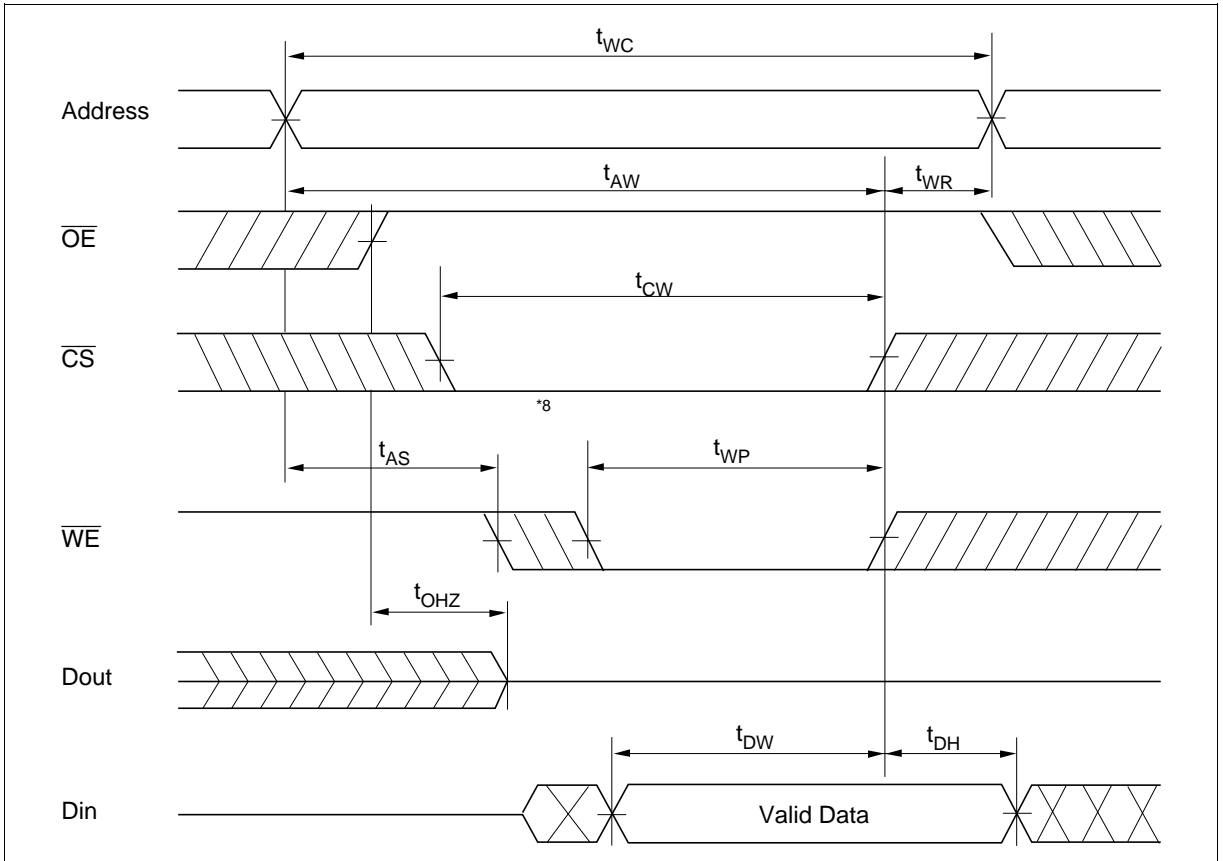
Timing Waveforms

Read Timing Waveform ( $\overline{WE} = V_{IH}$ )

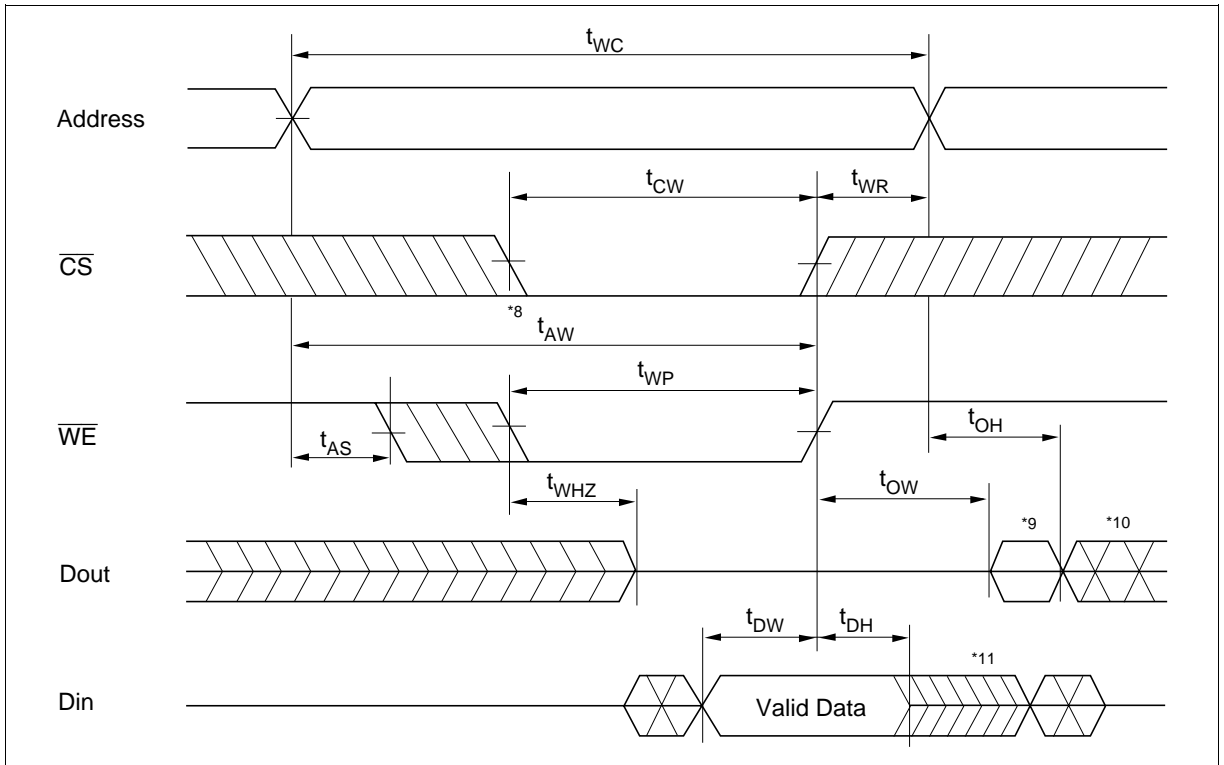


# HM62V8512C Series

## Write Timing Waveform (1) ( $\overline{OE}$ Clock)



Write Timing Waveform (2) ( $\overline{OE}$  Low Fixed)



## Low $V_{CC}$ Data Retention Characteristics ( $T_a = -20$ to $+70^\circ\text{C}$ )

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions*3
$V_{CC}$ for data retention	$V_{DR}$	2	—	—	V	$\overline{CS} \geq V_{CC} - 0.2 \text{ V}$ , $V_{in} \geq 0 \text{ V}$
Data retention current	$I_{CCDR}$	—	$0.5^{*4}$	$20^{*1}$	$\mu\text{A}$	$V_{CC} = 3.0 \text{ V}$ , $V_{in} \geq 0 \text{ V}$ $\overline{CS} \geq V_{CC} - 0.2 \text{ V}$
		—	$0.5^{*4}$	$10^{*2}$	$\mu\text{A}$	
Chip deselect to data retention time	$t_{CDR}$	0	—	—	ns	See retention waveform
Operation recovery time	$t_R$	$t_{RC}^{*5}$	—	—	ns	

Notes: 1. For L-version and  $10 \mu\text{A}$  (max.) at  $T_a = -20$  to  $+40^\circ\text{C}$ .

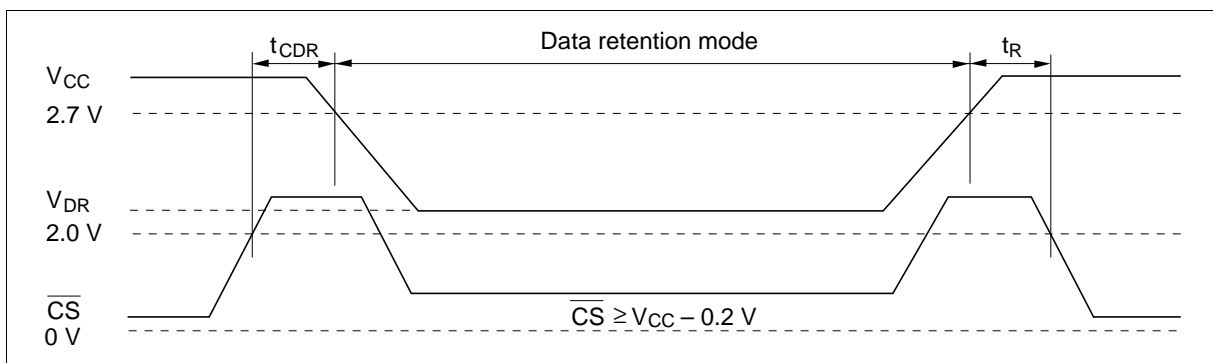
2. For L-SL-version and  $3 \mu\text{A}$  (max.) at  $T_a = -20$  to  $+40^\circ\text{C}$ .

3.  $\overline{CS}$  controls address buffer,  $\overline{WE}$  buffer,  $\overline{OE}$  buffer, and  $D_{in}$  buffer. In data retention mode,  $V_{in}$  levels (address,  $\overline{WE}$ ,  $\overline{OE}$ , I/O) can be in the high impedance state.

4. Typical values are at  $V_{CC} = 3.0 \text{ V}$ ,  $T_a = +25^\circ\text{C}$  and specified loading, and not guaranteed.

5.  $t_{RC}$  = read cycle time.

## Low $V_{CC}$ Data Retention Timing Waveform ( $\overline{CS}$ Controlled)

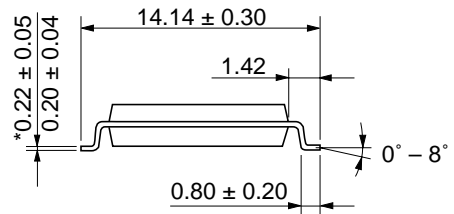
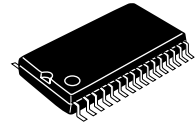
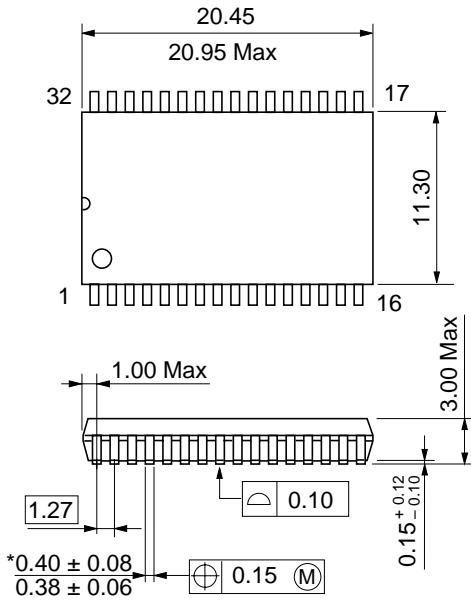


Package Dimensions

HM62V8512CLFP Series (FP-32D)

As of January, 2002

Unit: mm



\*Dimension including the plating thickness  
Base material dimension

Hitachi Code	FP-32D
JEDEC	Conforms
JEITA	—
Mass (reference value)	1.3 g

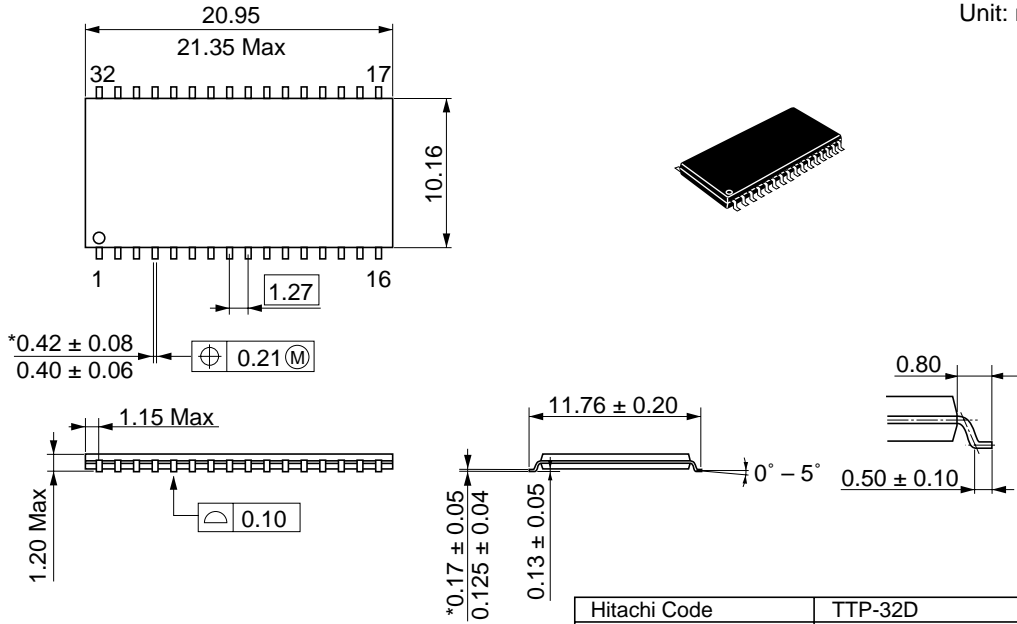
# HM62V8512C Series

## Package Dimensions (cont.)

### HM62V8512CLTT Series (TTP-32D)

As of January, 2002

Unit: mm



\*Dimension including the plating thickness  
Base material dimension

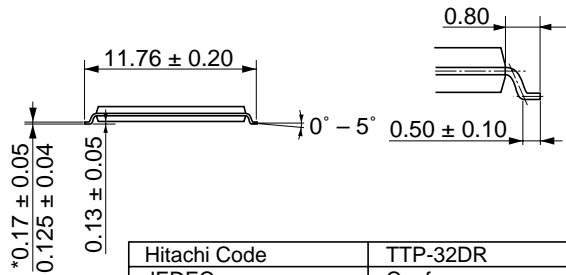
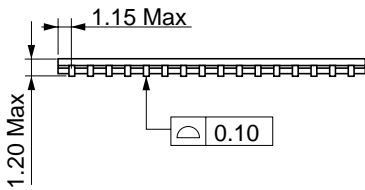
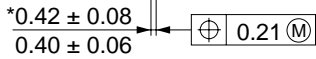
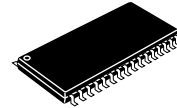
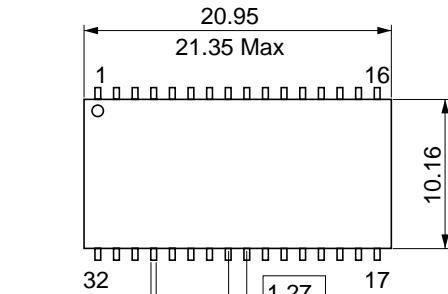
Hitachi Code	TTP-32D
JEDEC	Conforms
JEITA	—
Mass (reference value)	0.51 g

Package Dimensions (cont.)

HM62V8512CLRR Series (TTP-32DR)

As of January, 2002

Unit: mm



\*Dimension including the plating thickness  
Base material dimension

Hitachi Code	TTP-32DR
JEDEC	Conforms
JEITA	—
Mass (reference value)	0.51 g

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