

DATA SHEET

HSTL16918

9-bit to 18-bit HSTL-to-LVTTL
memory address latch

Product data

2001 Jun 16

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FEATURES

- Inputs meet JEDEC HSTL Std. JESD 8–6, and outputs meet Level III specifications
- ESD classification testing is done to JEDEC Standard JESD22. Protection exceeds 2000 V to HBM per method A114.
- Latch-up testing is done to JEDEC Standard JESD78, which exceeds 100 mA.
- Packaged in 48-pin plastic thin shrink small outline package (TSSOP48)

DESCRIPTION

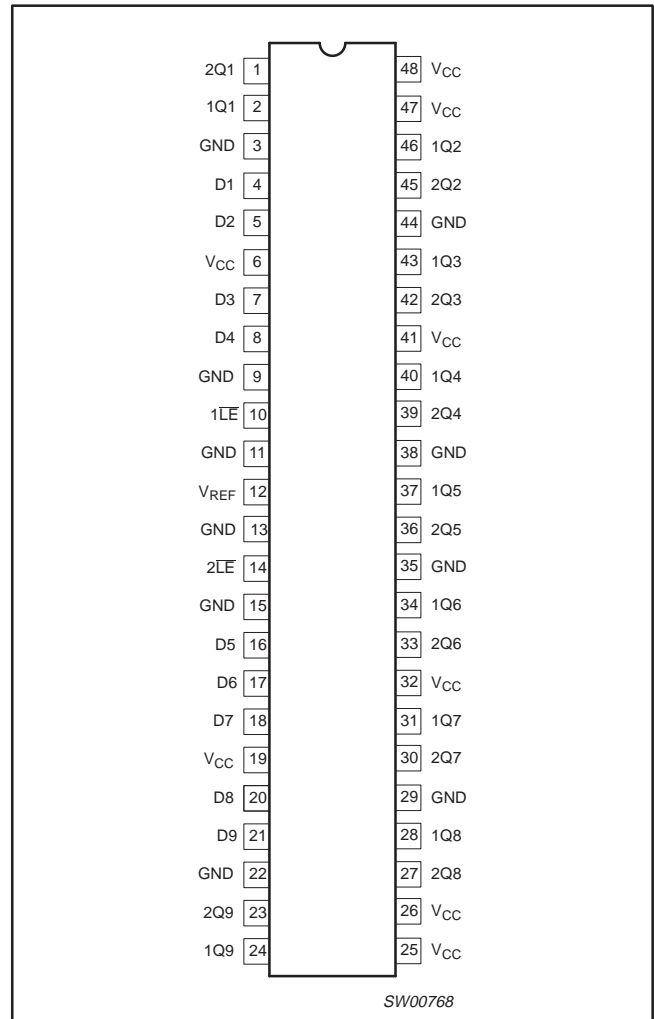
The HSTL16918 is a 9-bit to 18-bit D-type latch designed for 3.15 to 3.45 V V_{CC} operation. The D inputs accept HSTL levels and the Q outputs provide LVTTL levels.

The HSTL16918 is particularly suitable for driving an address bus to two banks of memory. Each bank of nine outputs is controlled with its own latch-enable (\overline{LE}) input.

Each of the nine D inputs is tied to the inputs of two D-type latches that provide true data (Q) at the outputs. While \overline{LE} is LOW the Q outputs of the corresponding nine latches follow the D inputs. When \overline{LE} is taken HIGH, the Q outputs are latched at the levels set up at the D inputs.

The HSTL16918 is characterized for operation from 0 to +70 °C.

PIN CONFIGURATION



ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DWG NUMBER
48-pin plastic thin shrink small outline package (TSSOP48)	0 to +70 °C	HSTL16918DGG	SOT362-1

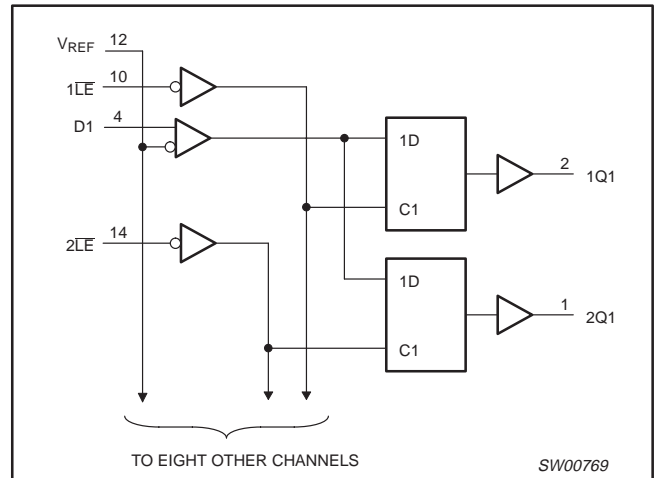
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PIN DESCRIPTION

PIN	SYMBOL	FUNCTION
4, 5, 7, 8, 16, 17, 18, 20, 21	D[1-9]	Inputs
2, 46, 43, 40, 37, 34, 31, 28, 24	1Q[1-9]	Outputs
1, 45, 42, 39, 36, 33, 30, 27, 23	2Q[1-9]	
10	1LE	Latch enable
14	2LE	
12	V _{REF}	Reference voltage
6, 19, 25, 26, 32, 41, 47, 48	V _{CC}	Supply voltage
3, 9, 11, 13, 15, 22, 29, 35, 38, 44	GND	Ground

LOGIC DIAGRAM (positive logic)



FUNCTION TABLE

INPUTS		OUTPUT Q
LE	D	
L	H	H
L	L	L
H	X	Q ₀ ¹

NOTE:

- Output level before the indicated steady-state input conditions were established.

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ABSOLUTE MAXIMUM RATINGS¹

Over operating free-air temperature range (unless otherwise noted).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	Supply voltage range		-0.5 to +4.6	V
V_I	Input voltage range ²		-0.5 to $V_{CC} + 0.5$	V
V_O	Output voltage range ²		-0.5 to $V_{CC} + 0.5$	V
I_{IK}	Input clamp current	$V_I < 0$	-50	mA
I_{OK}	Output clamp current ³	$V_O < 0$ or $V_O > V_{CC}$	±50	mA
I_O	Continuous output current	$V_O = 0$ to V_{CC}	±50	mA
	Continuous current through each V_{CC} or GND		±100	mA
θ_{JA}	Package thermal impedance ⁴		89	°C/W
T_{stg}	Storage temperature range		-65 to +150	°C

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- This current flows only when the output is in the high state and $V_O > V_{CC}$.
- The package thermal impedance is calculated in accordance with JESD 51.

RECOMMENDED OPERATING CONDITIONS¹

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		3.15		3.45	V
V_{REF}	Reference voltage		0.68	0.75	0.9	V
V_I	Input voltage		0		1.5	V
V_{IH}	AC high-level input voltage	All inputs	$V_{REF} + 200$ mV			V
V_{IL}	AC low-level input voltage	All inputs			$V_{REF} - 200$ mV	V
V_{IH}	DC high-level input voltage	All inputs	$V_{REF} + 100$ mV			V
V_{IL}	DC low-level input voltage	All inputs			$V_{REF} - 100$ mV	V
I_{OH}	High-level output current				-24	mA
I_{OL}	Low-level output current				24	mA
T_{amb}	Operating free-air temperature range		0		+70	°C

NOTE:

- All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

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ELECTRICAL CHARACTERISTICS

Over recommended operating free-air temperature range (unless otherwise noted).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ ¹	Max	
V_{IK}		$V_{CC} = 3.15\text{ V}; I_I = -18\text{ mA}$			-1.2	V
V_{OH}		$V_{CC} = 3.15\text{ V}; I_{OH} = -24\text{ mA}$	2.4			V
V_{OL}		$V_{CC} = 3.15\text{ V}; I_{OL} = 24\text{ mA}$			0.5	V
I_I	Control inputs	$V_{CC} = 3.45\text{ V}; V_I = 0\text{ or }1.5\text{ V}$			± 5	μA
	Data inputs	$V_{CC} = 3.45\text{ V}; V_I = 0\text{ or }1.5\text{ V}$			± 5	μA
	V_{REF}	$V_{CC} = 3.45\text{ V}; V_{REF} = 0.68\text{ V or }0.9\text{ V}$			90	μA
I_{CC}		$V_{CC} = 3.45\text{ V}; V_I = 0\text{ or }1.5\text{ V}$		50	100	mA
C_I	Control inputs	$V_{CC} = 0\text{ or }3.3\text{ V}; V_I = 0\text{ or }3.3\text{ V}$		2		pF
	Data inputs	$V_{CC} = 0\text{ or }3.3\text{ V}; V_I = 0\text{ or }3.3\text{ V}$		2.5		pF
C_O	Outputs	$V_{CC} = 0\text{ V}; V_O = 0\text{ V}$		4		pF

NOTE:1. All typical values are at $V_{CC} = 3.3\text{ V}; T_{amb} = 25\text{ }^\circ\text{C}$.**TIMING REQUIREMENTS**

Over recommended operating free-air temperature range (unless otherwise noted).

SYMBOL	PARAMETER	TEST CONDITIONS	$V_{CC} = 3.3\text{ V} \pm 0.15\text{ V}$		UNIT
			Min	Max	
t_w	Pulse duration	LE LOW (Figure 1)	3		ns
t_{su}	Setup time	D before $\overline{LE} \uparrow$ (Figure 2)	2		ns
t_h	Hold time	D after $\overline{LE} \uparrow$ (Figure 2)	1		ns
t_{ldr}	Data race condition time ¹	D after $\overline{LE} \downarrow$		0	ns

NOTE:1. This is the maximum time after \overline{LE} switches LOW that the data input can return to the latched state from the opposite state without producing a glitch on the output.**SWITCHING CHARACTERISTICS**Over recommended operating free-air temperature range; $V_{REF} = 0.75\text{ V}$.

SYMBOL	PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 3.3\text{ V} \pm 0.15\text{ V}$		UNIT
				Min	Max	
t_{pd}	Propagation delay (Figure 3)	D	Q	1.9	3.4	ns
		\overline{LE}	Q	1.9	4.2	ns

SIMULTANEOUS SWITCHING CHARACTERISTICSOver recommended operating free-air temperature range; $V_{REF} = 0.75\text{ V}$

SYMBOL	PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 3.3\text{ V} \pm 0.15\text{ V}$		UNIT
				Min	Max	
t_{pd}	Propagation delay; all outputs switching (Figure 3)	D	Q	1.9	4.4	ns
		\overline{LE}	Q	1.9	5.2	ns

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VOLTAGE WAVEFORMS

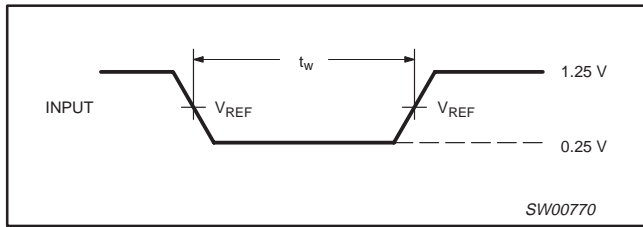
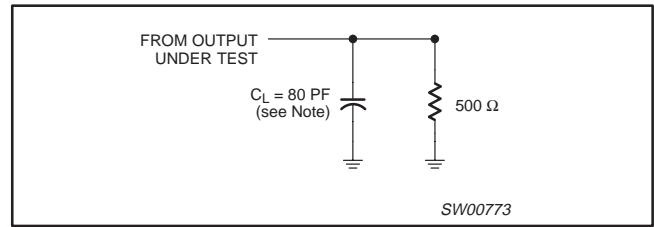


Figure 1. Pulse duration

LOAD CIRCUIT



NOTE: C_L includes probe and jig capacitance.

Figure 4. Load circuit

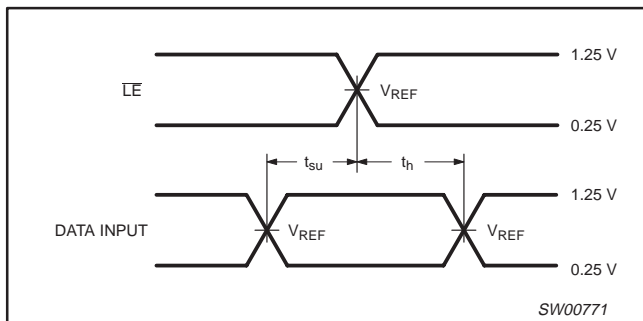


Figure 2. Setup and Hold times

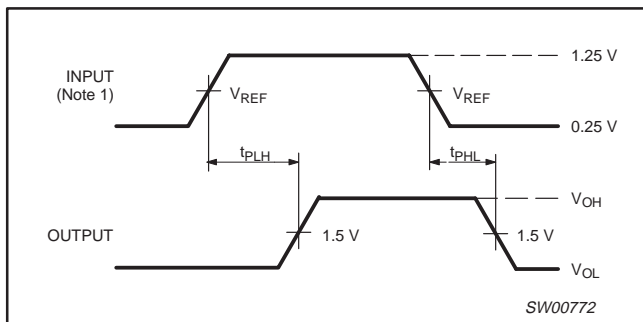


Figure 3. Propagation delay times

NOTES:

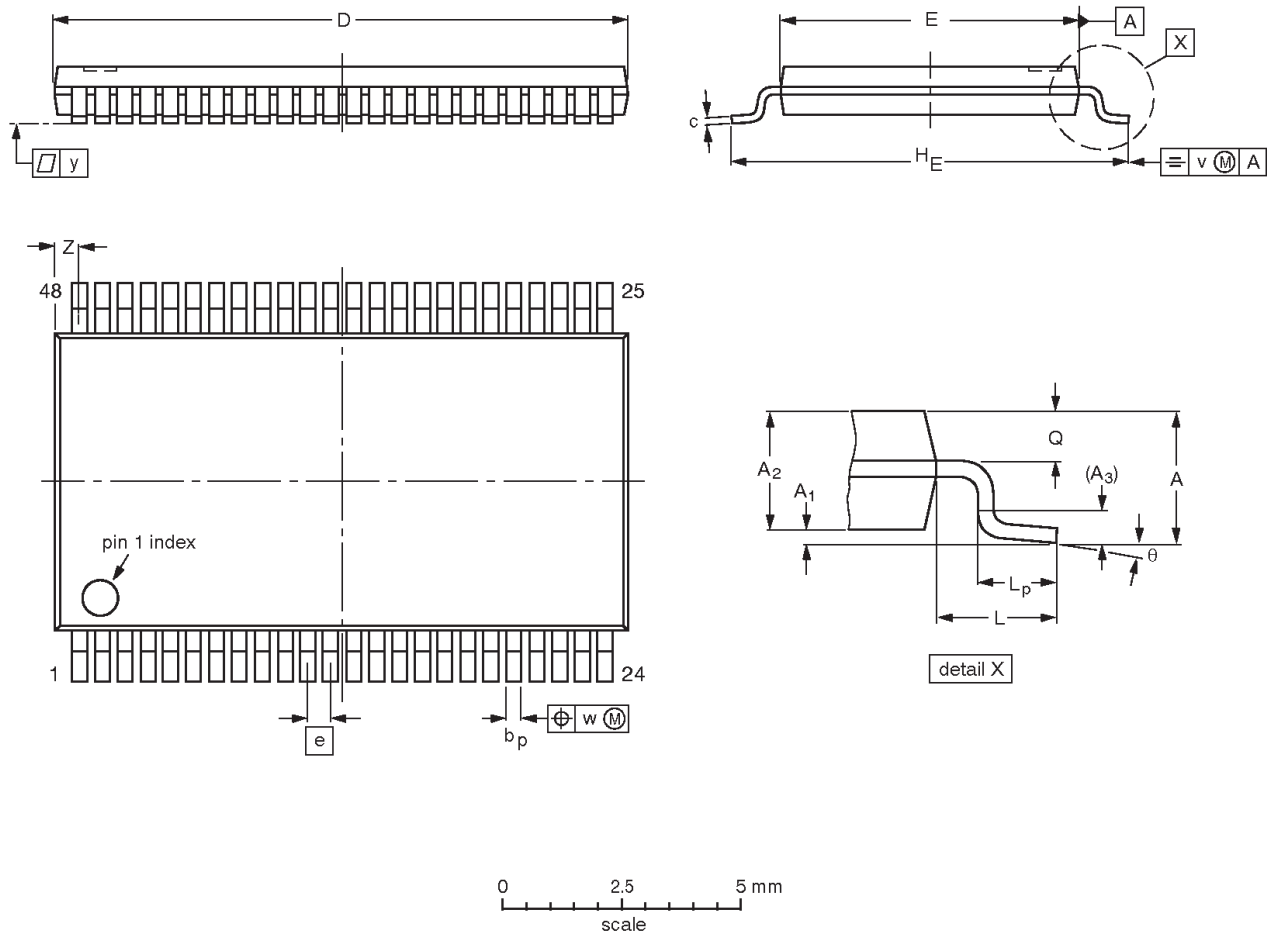
1. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 1 ns, t_f ≤ 1 ns.
2. The outputs are measured one at a time with one transition per measurement.
3. t_{P_{HL}} and t_{P_{LH}} are the same as t_{pd}.

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TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm

SOT362-1



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	12.6 12.4	6.2 6.0	0.5	8.3 7.9	1	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.8 0.4	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT362-1		MO-153				-95-02-10 99-12-27

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Data sheet status

Data sheet status ^[1]	Product status ^[2]	Definitions
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

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