

32-Channel LCD Driver with Separate Backplane Output

Ordering Information

| Device | Package Options | | |
|--------|-------------------------------|-------------------------------------|--------------------|
| | 44 Lead Quad Plastic Gullwing | 44 J-Lead Quad Plastic Chip Carrier | Die in waffle pack |
| HV66 | HV66PG | HV66PJ | HV66X |

Features

- Processed with HVCMOS® technology
- 32 push-pull CMOS output up to 32V
- Low power level shifting
- Source/sink current minimum 1mA
- Shift register speed 5MHz
- Latched data outputs
- Bidirectional shift register (DIR)
- Backplane output

Absolute Maximum Ratings¹

| | |
|-------------------------------------------------------------|--------------------------|
| Supply voltage, V_{DD}^2 | -0.5V to +7.0V |
| Output voltage, V_{PP}^2 | -0.5V to +35V |
| Logic input levels ² | -0.5V to $V_{DD} + 0.5V$ |
| Ground current ³ | 1.5A |
| Continuous total power dissipation ⁴ | 1200mW |
| Operating temperature range | -40°C to +85°C |
| Storage temperature range | -65°C to +125°C |
| Lead temperature 1.6mm (1/16 inch) from case for 10 seconds | 260°C |

Notes:

1. Device will survive (but operation may not be specified or guaranteed) at these extremes.
2. All voltages are referenced to V_{SS} .
3. Duty cycle is limited by the total power dissipated in the package.
4. For operation above 25°C ambient derate linearly to 85°C at 20mW/°C.

General Description

Not recommended for new designs.

The HV66 is a low-voltage serial to high-voltage parallel converter with push-pull outputs. This device has been designed for use as a driver circuit for LCD displays. It can also be used in any application requiring multiple output high-voltage current sourcing and sinking capabilities. The inputs are fully CMOS compatible.

The device consists of a 32-bit shift register, 32 latches, and control logic to perform blanking and polarity control of the outputs. HVout1 is connected to the first stage of the shift register. Data is shifted through the shift register on the logic rising transition of the clock. A DIR pin causes data shifting counterclockwise when grounded and clockwise when connected to V_{DD} . A data output buffer is provided for cascading devices. This output reflects the current status of the last bit of the shift register. Operation of the shift register is not affected by the LE (latch enable), BL (blank) or the POL (polarity) inputs. Transfer of data from the shift register to the latch occurs when the LE (latch enable) input is high. The data in the latch is stored after LE transitions from high to low.

The blank signal, BL, when pulled low, will set all outputs to the same state as the BP_{OUT} . If this signal is left open then the BL defaults to a high state.

Electrical Characteristics (over recommended operating conditions unless noted)

DC Characteristics ($V_{DD} = 5V$, $V_{PP} = 32V$, $V_{SS} = GND$)

| Symbol | Parameter | Min | Max | Units | Conditions |
|------------|--------------------------------------|----------|-----|---------|--------------------------------------------|
| I_{DD} | V_{DD} supply current | | 15 | mA | $V_{DD} = V_{DD\ max}$ $f_{CLK} = 5MHz$ |
| I_{PPQ} | High voltage supply current | | 0.5 | mA | Outputs high |
| | | | 0.5 | mA | Outputs low |
| I_{DDQ} | Quiescent V_{DD} supply current | | 0.5 | mA | All $V_{IN} = V_{SS}$ or V_{DD} |
| V_{OH} | High-level output | Q | 22 | V | $I_O = 1mA$, $V_{PP} = 24V$ |
| | | Data out | 4.6 | V | $I_O = -100\mu A$ |
| V_{OL} | Low-level output | Q | 2 | V | $I_O = 1mA$ |
| | | Data out | 0.4 | V | $I_O = 100\mu A$ |
| I_{IH} | High-level logic input current | | 1 | μA | $V_{IH} = V_{DD}$ |
| I_{IL} | Low-level logic input current | | -1 | μA | $V_{IL} = 0V$ |
| V_{OLBP} | Low-level output voltage, backplane | | 3 | V | $I_O = 10mA$ |
| V_{OHBP} | High-level output voltage, backplane | 29 | | V | $I_O = -10mA$ |

AC Characteristics ($V_{DD} = 5V$, $V_{PP} = 32V$, $T_C = 25^\circ C$), logic input rises/fall time = 10ns.

| Symbol | Parameter | Min | Max | Units | Conditions |
|---------------------|---------------------------------------------|-----|------|---------|---------------|
| f_{CLK} | Clock frequency | | 5 | MHz | |
| t_W | Clock width high or low | 100 | | ns | |
| t_{SU} | Data set-up time before clock rises | 25 | | ns | |
| t_H | Data hold time after clock rises | 50 | | ns | |
| t_{ON}, t_{OFF} | Time from latch enable or POL to HV_{OUT} | | 500 | ns | $C_L = 20pF$ |
| t_{ON}, t_{OFF} | Time from POL to BP output | | 500 | ns | $C_L = 20pF$ |
| t_{DHL} | Delay time clock to data high to low | | 200 | ns | $C_L = 10pF$ |
| t_{DLH} | Delay time clock to data low to high | | 200 | ns | $C_L = 10pF$ |
| t_{DLE} | Delay time clock to LE low to high | 50 | | ns | |
| t_{WLE} | Width of LE pulse | 100 | | ns | |
| t_{SLE} | LE set-up time before clock rises | 50 | | ns | |
| t_{BR}, t_{BF} | BP_{OUT} rise/fall time | 10 | 1000 | μs | $C_L = 350nF$ |
| $ t_{BR} - t_{BF} $ | BP_{OUT} rise and fall difference | | 100 | μs | $C_L = 350nF$ |

Recommended Operating Conditions

| Symbol | Parameter | Min | Max | Units |
|-----------|-----------------------------------------|-----|----------|------------|
| V_{DD} | Logic supply voltage | 4.5 | 5.5 | V |
| V_{PP} | Output voltage* | 0 | 32 | V |
| V_{IH} | High-level input voltage | 2.4 | V_{DD} | V |
| V_{IL} | Low-level input voltage | 0 | 0.8 | V |
| f_{CLK} | Clock frequency | 0 | 5 | MHz |
| T_A | Operating free-air temperature | -40 | +85 | $^\circ C$ |
| I_{OD} | Allowable current through output diodes | | 200 | mA |

Notes:

*Output will not switch below 12V.

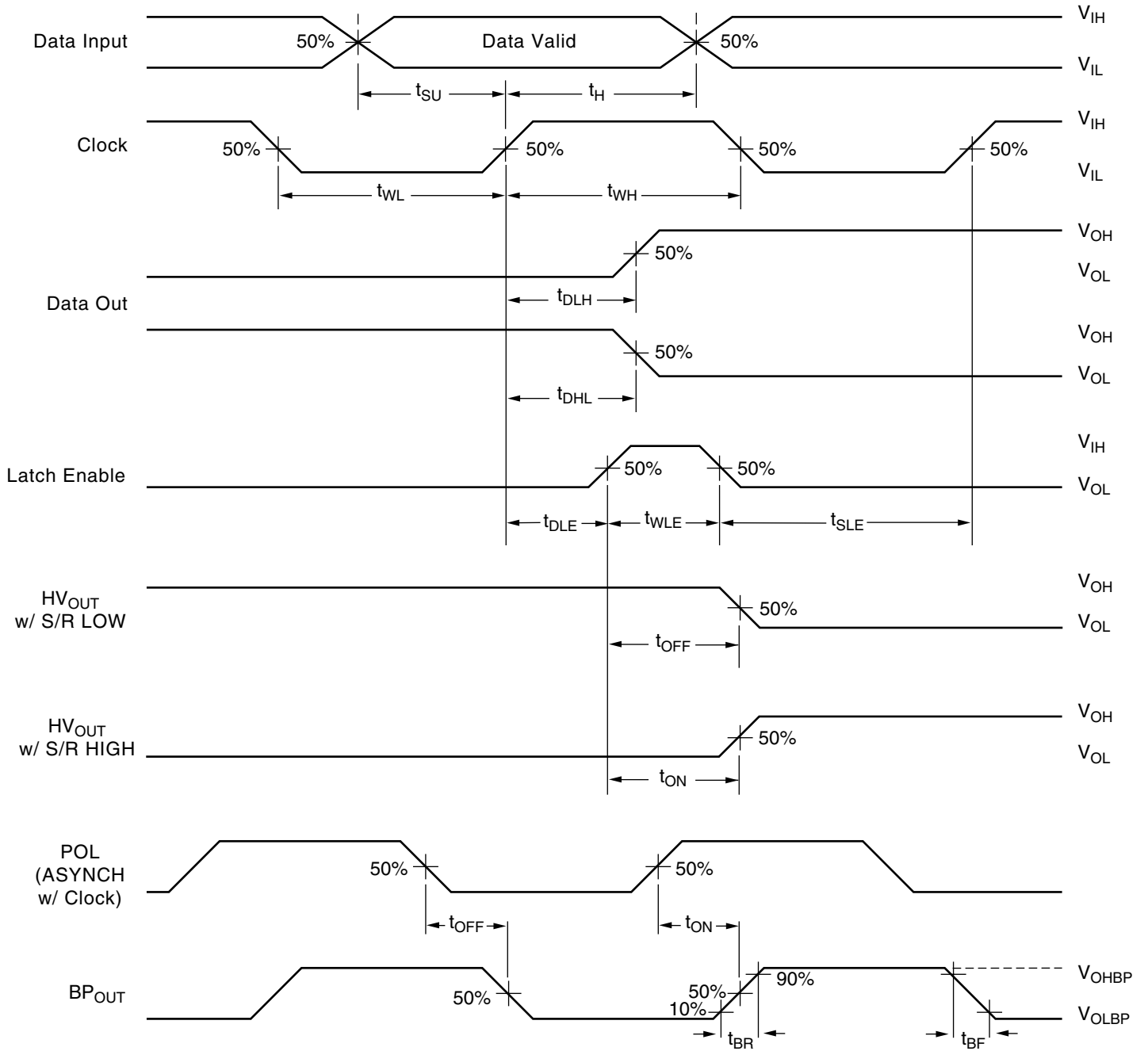
Power-up sequence should be the following:

1. Connect ground.
2. Apply V_{DD} .
3. Set all inputs (Data, CLK, Enable, etc.) to a known state.
4. Apply V_{PP} .

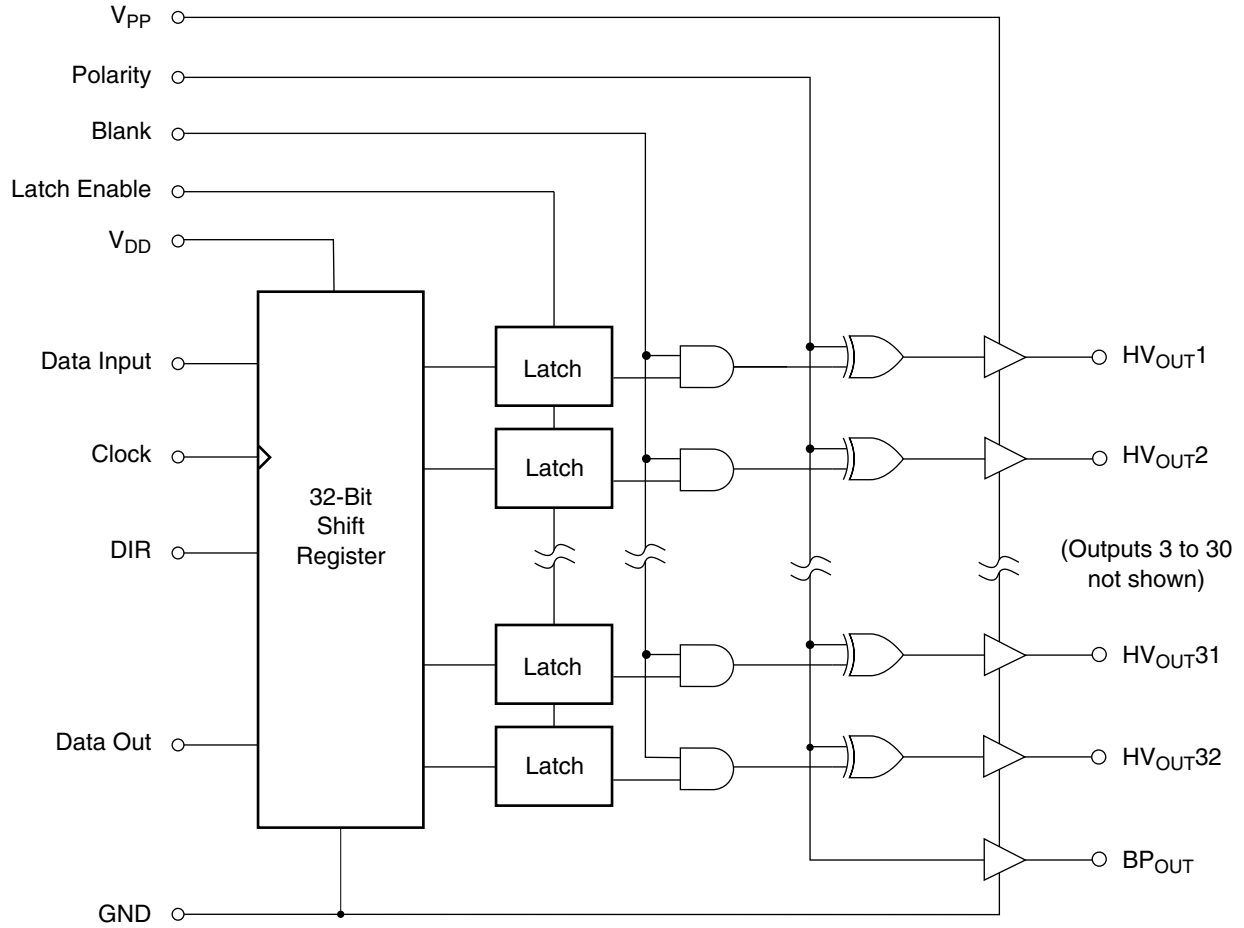
Power-down sequence should be the reverse of the above.

The V_{PP} should not drop below V_{DD} during operation.

Switching Waveforms



Functional Block Diagram



Function Table

| Function | Inputs | | | | | | Outputs | | | | | |
|------------------|--------|--------|----|----|-----|-----|-----------------------------------|------------------|----------------|-------------------|-----------------|---------------------|
| | Data | CLK | LE | BL | POL | DIR | Shift Reg 1 | Shift Reg 2...32 | HV Outputs 1 | HV Outputs 2...32 | Data Out 2...32 | BP _{OUT} * |
| Load S/R | H or L | ↑ | L | H | H | X | H or L | *...* | $\overline{*}$ | $\overline{*...}$ | * | H |
| Load latches | X | H or L | L | H | H | X | * | *...* | $\overline{*}$ | $\overline{*...}$ | * | H |
| | X | H or L | L | H | L | X | * | *...* | * | *...* | * | L |
| Transparent Mode | L | ↑ | H | H | H | X | L | *...* | H | *...* | * | H |
| | H | ↑ | H | H | H | X | H | *...* | L | *...* | * | H |
| | L | ↑ | H | H | L | X | L | *...* | L | *...* | * | L |
| | H | ↑ | H | H | L | X | H | *...* | H | *...* | * | L |
| R/L Shift | X | ↑ | X | H | X | H | Q _n → Q _{n+1} | * | *...* | Q ₃₂ | | |
| | X | ↑ | X | H | X | L | Q _n → Q _{n-1} | * | *...* | Q ₁ | | |
| Blank | X | X | X | L | L | X | * | *...* | L | L...L | * | L |
| Control | X | X | X | L | H | X | * | *...* | H | H...H | * | H |

Notes:
 H = high level, L = low level, X = irrelevant, ↑ = low-to-high transition.
 * = dependent on previous stage's state before the last CLK or last LE high.

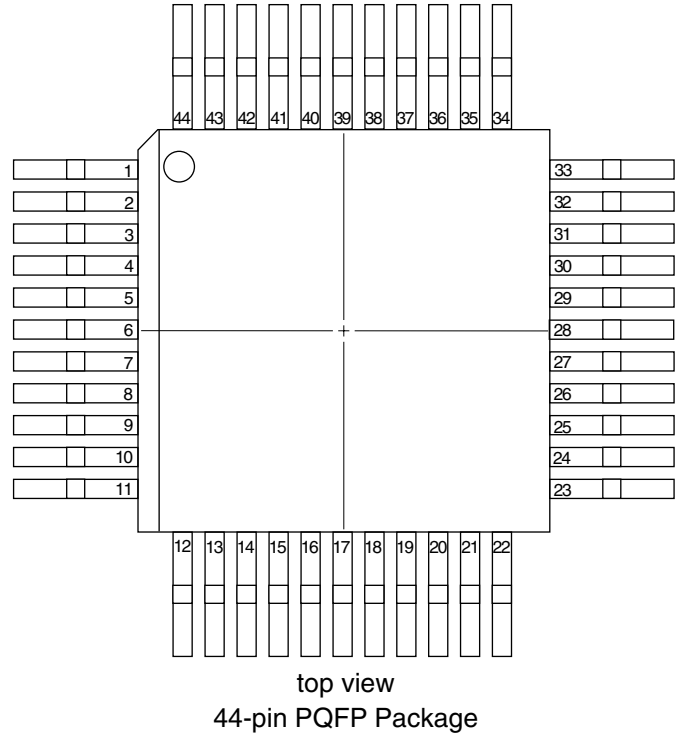
Pin Configuration

HV66 44 Pin Plastic Gullwing (QFP) Package

| Pin | Function | Pin | Function |
|-----|-------------------------|-----|-------------------------|
| 1 | HV _{OUT} 22/11 | 23 | Data Out |
| 2 | HV _{OUT} 21/12 | 24 | GND |
| 3 | HV _{OUT} 20/13 | 25 | N/C |
| 4 | HV _{OUT} 19/14 | 26 | BL |
| 5 | HV _{OUT} 18/15 | 27 | POL |
| 6 | HV _{OUT} 17/16 | 28 | LE |
| 7 | HV _{OUT} 16/17 | 29 | V _{DD} |
| 8 | HV _{OUT} 15/18 | 30 | Clock |
| 9 | HV _{OUT} 14/19 | 31 | DIR |
| 10 | HV _{OUT} 13/20 | 32 | Data In |
| 11 | HV _{OUT} 12/21 | 33 | V _{PP} |
| 12 | HV _{OUT} 11/22 | 34 | BP Out |
| 13 | HV _{OUT} 10/23 | 35 | HV _{OUT} 32/1 |
| 14 | HV _{OUT} 9/24 | 36 | HV _{OUT} 31/2 |
| 15 | HV _{OUT} 8/25 | 37 | HV _{OUT} 30/3 |
| 16 | HV _{OUT} 7/26 | 38 | HV _{OUT} 29/4 |
| 17 | HV _{OUT} 6/27 | 39 | HV _{OUT} 28/5 |
| 18 | HV _{OUT} 5/28 | 40 | HV _{OUT} 27/6 |
| 19 | HV _{OUT} 4/29 | 41 | HV _{OUT} 26/7 |
| 20 | HV _{OUT} 3/30 | 42 | HV _{OUT} 25/8 |
| 21 | HV _{OUT} 2/31 | 43 | HV _{OUT} 24/9 |
| 22 | HV _{OUT} 1/32 | 44 | HV _{OUT} 23/10 |

Note:
Pin designation for DIR = H/L
Example: for DIR = H, Pin 1 is HV_{OUT} 22
for DIR = L, Pin 1 is HV_{OUT} 11

Package Outline

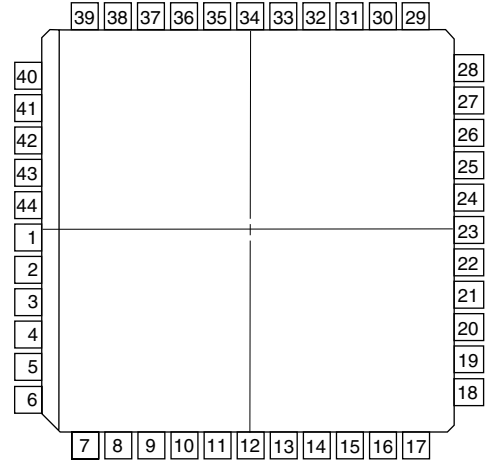


Pin Configuration

Package Outline

HV66
44 Pin J-Lead Package

| Pin | Function | Pin | Function |
|-----|-------------------------|-----|-------------------------|
| 1 | HV _{OUT} 17/16 | 23 | LE |
| 2 | HV _{OUT} 16/17 | 24 | V _{DD} |
| 3 | HV _{OUT} 15/18 | 25 | Clock |
| 4 | HV _{OUT} 14/19 | 26 | DIR |
| 5 | HV _{OUT} 13/20 | 27 | Data In |
| 6 | HV _{OUT} 12/21 | 28 | V _{PP} |
| 7 | HV _{OUT} 11/22 | 29 | BP Out |
| 8 | HV _{OUT} 10/23 | 30 | HV _{OUT} 32/1 |
| 9 | HV _{OUT} 9/24 | 31 | HV _{OUT} 31/2 |
| 10 | HV _{OUT} 8/25 | 32 | HV _{OUT} 30/3 |
| 11 | HV _{OUT} 7/26 | 33 | HV _{OUT} 29/4 |
| 12 | HV _{OUT} 6/27 | 34 | HV _{OUT} 28/5 |
| 13 | HV _{OUT} 5/28 | 35 | HV _{OUT} 27/6 |
| 14 | HV _{OUT} 4/29 | 36 | HV _{OUT} 26/7 |
| 15 | HV _{OUT} 3/30 | 37 | HV _{OUT} 25/8 |
| 16 | HV _{OUT} 2/31 | 38 | HV _{OUT} 24/9 |
| 17 | HV _{OUT} 1/32 | 39 | HV _{OUT} 23/10 |
| 18 | Data Out | 40 | HV _{OUT} 22/11 |
| 19 | GND | 41 | HV _{OUT} 21/12 |
| 20 | N/C | 42 | HV _{OUT} 20/13 |
| 21 | BL | 43 | HV _{OUT} 19/14 |
| 22 | POL | 44 | HV _{OUT} 18/15 |



top view
 44-pin PLCC

Note:
 1. Pin designation for DIR = H/L
 Example: for DIR = H, Pin 1 = HV_{OUT} 17
 for DIR = L, Pin 1 = HV_{OUT} 16



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