Document Title

512K x8 bit 5.0V Low Power CMOS slow SRAM

Revision History

Revision No	History	Draft Date	Remark
04	Revision History Insert	Jul.06.2000	Final
05	Revised - Change Iccdr Value : 15uA => 20uA	Aug.04.2000	Final
06	Marking Information Add Revised - E.T (-25~85°C), I.T (-40~85°C) Part Insert - AC Test Condition Add : 5pF Test Load	Dec.04.2000	Final
07	Changed Logo - HYUNDAI -> hynix - Marking Information Change	Apr.30.2001	Final

DESCRIPTION

The HY628400A is a high-speed, low power and 4M bits CMOS SRAM organized as 512K words by 8 bits. The HY628400A uses Hynix's high performance twin tub CMOS process technology and was designed for high-speed and low power circuit technology. It is particularly well suited for use in high-density and low power system applications. This device has a data retention mode that guarantees data to remain valid at the minimum power supply voltage of 2.0V.

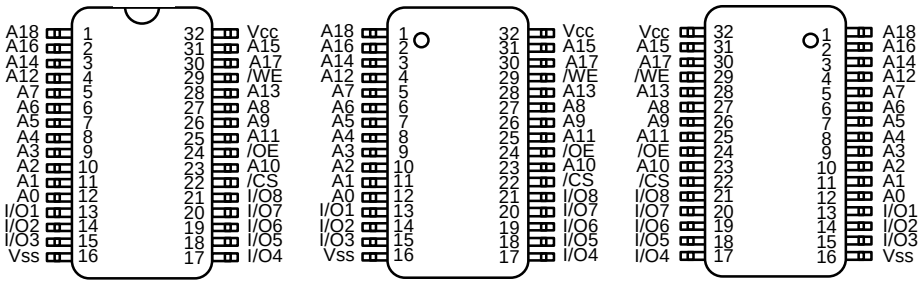
FEATURES

- Fully static operation and Tri-state outputs
- TTL compatible inputs and outputs
- Low power consumption
- Battery backup(L/LL-part)
  -. 2.0V(min) data retention
- Standard pin configuration
  -. 32pin 525mil SOP
  -. 32pin 400mil TSOP-II
  (Standard and Reversed)

Product No.	Voltage (V)	Speed (ns)	Operation Current/Icc(mA)	Standby Current(uA)		Temperature (°C)
				L	LL	
HY628400A	4.5~5.5	55/70/85	10	100	30	0~70
HY628400A-E	4.5~5.5	55/70/85	10	100	50	-25~85
HY628400A-I	4.5~5.5	55/70/85	10	100	50	-40~85

Note 1. Current value is max.

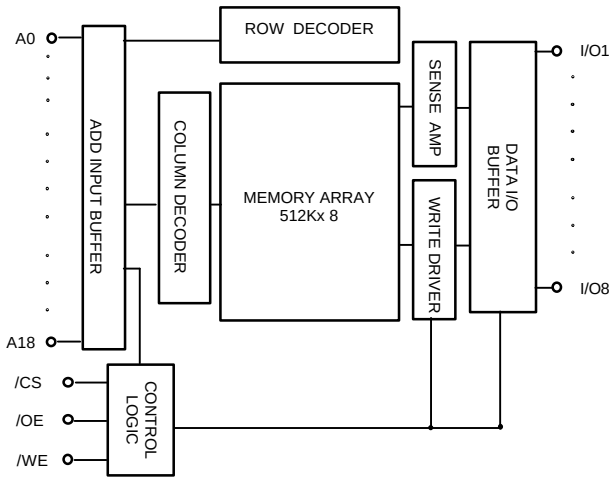
PIN CONNECTION



PIN DESCRIPTION

Pin Name	Pin Function
/CS	Chip Select
/WE	Write Enable
/OE	Output Enable
A0 ~ A18	Address Inputs
I/O1 ~ I/O8	Data Inputs/Outputs
Vcc	Power(4.5~5.5V)
Vss	Ground

BLOCK DIAGRAM



ORDERING INFORMATION

Part No.	Speed	Power	Temp	Package
HY628400ALG	55/70/85	L-part	0-70°C	SOP
HY628400ALLG	55/70/85	LL-part	0-70°C	SOP
HY628400ALG-E	55/70/85	L-part	-25-85°C	SOP
HY628400ALLG-E	55/70/85	LL-part	-25-85°C	SOP
HY628400ALG-I	55/70/85	L-part	-40-85°C	SOP
HY628400ALLG-I	55/70/85	LL-part	-40-85°C	SOP
HY628400ALT2	55/70/85	L-part	0-70°C	TSOP-II (Standard)
HY628400ALLT2	55/70/85	LL-part	0-70°C	TSOP-II (Standard)
HY628400ALT2-E	55/70/85	L-part	-25-85°C	TSOP-II (Standard)
HY628400ALLT2-E	55/70/85	LL-part	-25-85°C	TSOP-II (Standard)
HY628400ALT2-I	55/70/85	L-part	-40-85°C	TSOP-II (Standard)
HY628400ALLT2-I	55/70/85	LL-part	-40-85°C	TSOP-II (Standard)
HY628400ALR2	55/70/85	L-part	0-70°C	TSOP-II (Reversed)
HY628400ALLR2	55/70/85	LL-part	0-70°C	TSOP-II (Reversed)
HY628400ALR2-E	55/70/85	L-part	-25-85°C	TSOP-II (Reversed)
HY628400ALLR2-E	55/70/85	LL-part	-25-85°C	TSOP-II (Reversed)
HY628400ALR2-I	55/70/85	L-part	-40-85°C	TSOP-II (Reversed)
HY628400ALLR2-I	55/70/85	LL-part	-40-85°C	TSOP-II (Reversed)

ABSOLUTE MAXIMUM RATING (1)

Symbol	Parameter		Rating	Unit
Vcc, VIN, VOUT	Power Supply, Input/Output Voltage		-0.5 to 7.0	V
TA	Operating Temperature	HY628400A	0 to 70	°C
		HY628400A-E	-25 to 85	°C
		HY628400A-I	-40 to 85	°C
TSTG	Storage Temperature		-65 to 150	°C
PD	Power Dissipation		1.0	W
IOUT	Data Output Current		50	MA
TSOLDER	Lead Soldering Temperature & Time		260 •10	°C•sec

Note
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and the functional operation of the device under these or any other conditions above those indicated in the operation of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect reliablity.

TRUTH TABLE

/CS	/WE	/OE	MODE	I/O OPERATION	Power
H	X	X	Deselected	High-Z	Standby
L	H	H	Output Disabled	High-Z	Active
L	H	L	Read	Data Out	Active
L	L	X	Write	Data In	Active

Note :
1. H=VIH, L=VIL, X=don't care (VIH or VIL)

RECOMMENDED DC OPERATING CONDITION

T_A = 0¡ Éto 70¡ É(Normal)/-25°C to 85°C (Extended) /-40°C to 85°C (Industrial), unless otherwise specified.

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
Vss	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2	-	Vcc+0.5	V
V_{IL}	Input Low Voltage	-0.5(1)	-	0.8	V

Note :
1. V_{IL} = -1.5V for pulse width less than 30ns and not 100% tested.

DC ELECTRICAL CHARACTERISTICS

T_A = 0¡ Éto 70¡ É(Normal)/-25°C to 85°C (Extended) /-40°C to 85°C (Industrial), unless otherwise specified.

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
I_{LI}	Input Leakage Current	Vss ≤ V_{IN} ≤ Vcc		-1	-	1	UA
I_{LO}	Output Leakage Current	Vss ≤ V_{OUT} ≤ Vcc, /CS = V_{IH} or /OE = V_{IH} or /WE = V_{IL}		-1	-	1	UA
Icc	Operating Power Supply Current	/CS = V_{IL}, V_{IN} = V_{IH} or V_{IL}, $I_{I/O}$ = 0mA		-		10	MA
I_{CC1}	Average Operating Current	/CS = V_{IL} Min Duty Cycle = 100%, V_{IN} = V_{IH} or V_{IL}, $I_{I/O}$ = 0mA		-		60	MA
I_{SB}	TTL Standby Current (TTL Input)	/CS = V_{IH} V_{IN} = V_{IH} or V_{IL}		-		2	MA
I_{SB1}	Standby Current (CMOS Input)	/CS ≥ Vcc - 0.2V, V_{IN} ≥ Vcc - 0.2V or V_{IN} ≤ Vss + 0.2V	L	-	-	100	uA
			LL	-	-	30	uA
			L-E/I	-	-	100	uA
			LL-E/I	-	-	50	uA
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		-	-	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -1mA		2.4	-	-	V

Note : Typical values are at Vcc = 5.0V, T_A = 25°C

CAPACITANCE

Temp = 25°C, f= 1.0MHz

Symbol	Parameter	Condition	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Output Capacitance	$V_{I/O}$ = 0V	8	pF

Note : This parameter is sampled and not 100% tested

AC CHARACTERISTICS

TA = 0¡ Éto 70¡ É(Normal)/-25°C to 85°C (Extended) /-40°C to 85°C (Industrial), unless otherwise specified.

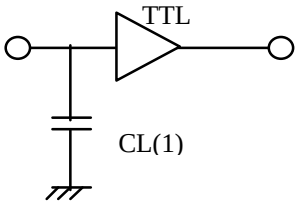
#	Symbol	Parameter	55ns		70ns		85ns		Unit
			Min.	Max.	Min.	Max.	Min	Max.	
	READ CYCLE								
1	tRC	Read Cycle Time	55	-	70	-	85	-	ns
2	tAA	Address Access Time	-	55	-	70	-	85	ns
3	tACS	Chip Select Access Time	-	55	-	70	-	85	ns
4	tOE	Output Enable to Output Valid	-	25	-	40	-	45	ns
5	tCLZ	Chip Select to Output in Low Z	10	-	10	-	10	-	ns
6	tOLZ	Output Enable to Output in Low Z	5	-	5	-	5	-	ns
7	tCHZ	Chip Deselecting to Output in High Z	0	20	0	25	0	30	ns
8	tOHZ	Out Disable to Output in High Z	0	20	0	25	0	30	ns
9	tOH	Output Hold from Address Change	10	-	10	-	10	-	ns
	WRITE CYCLE								
10	tWC	Write Cycle Time	55	-	70	-	85	-	ns
11	tCW	Chip Selection to End of Write	45	-	60	-	70	-	ns
12	tAW	Address Valid to End of Write	45	-	60	-	70	-	ns
13	tAS	Address Set-up Time	0	-	0	-	0	-	ns
14	tWP	Write Pulse Width	40	-	50	-	55	-	ns
15	tWR	Write Recovery Time	0	-	0	-	0	-	ns
16	tWHZ	Write to Output in High Z	0	20	0	25	0	30	ns
17	tDW	Data to Write Time Overlap	25	-	30	-	40	-	ns
18	tDH	Data Hold from Write Time	0	-	0	-	0	-	ns
19	tOW	Output Active from End of Write	5	-	5	-	5	-	ns

AC TEST CONDITIONS

TA = 0¡ Éto 70¡ É(Normal)/-25°C to 85°C (Extended) /-40°C to 85°C (Industrial), unless otherwise specified.

Parameter		Value
Input Pulse Level		0.8V to 2.4V
Input Rise and Fall Time		5ns
Input and Output Timing Reference Level		1.5V
Output Load	tCLZ,tOLZ,tCHZ,tOHZ,tWHZ	CL = 5pF + 1TTL Load
	Others	CL = 100pF + 1TTL Load

AC TEST LOADS

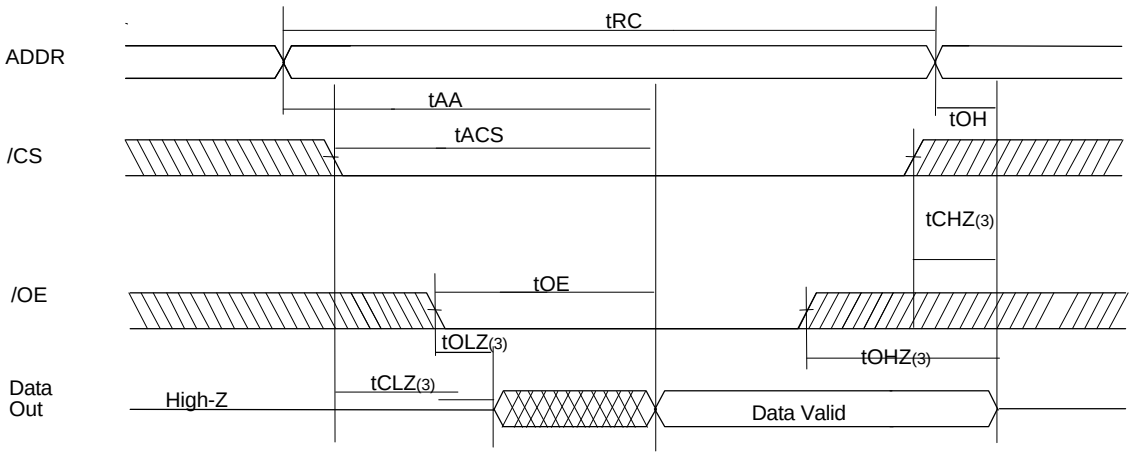


Note

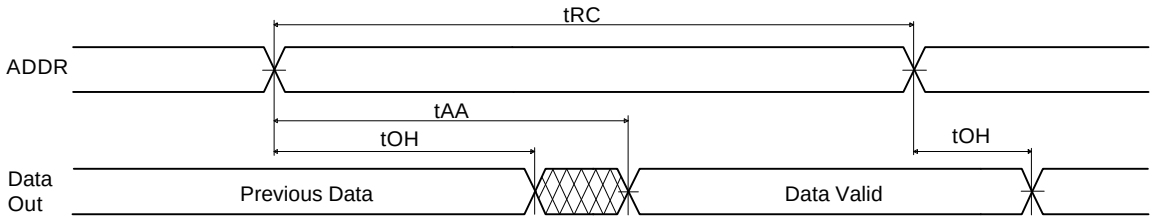
1. Including jig and scope capacitance

TIMING DIAGRAM

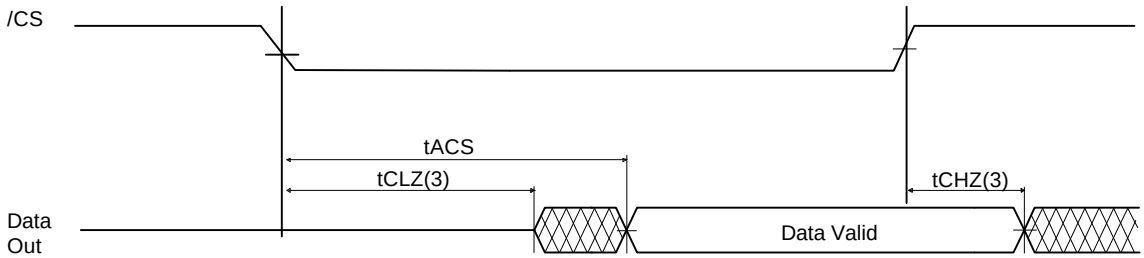
READ CYCLE 1(Note 1,4)



READ CYCLE 2(Note 1,2,4)

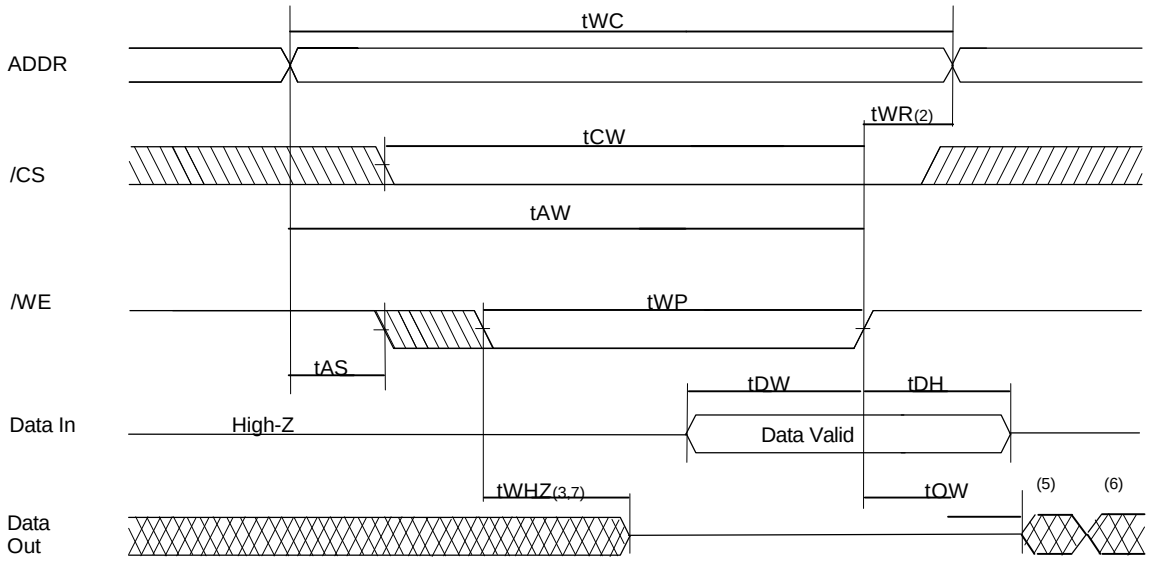


READ CYCLE 3(Note 1,2,4)

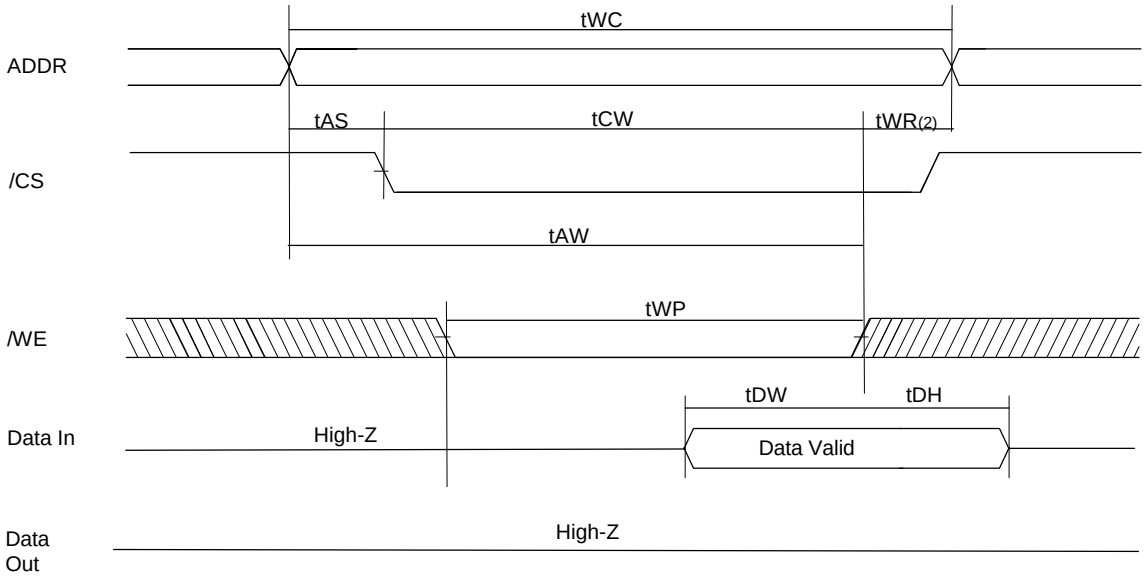


Notes:
1. A read occurs during the overlap of a low /OE, a high /WE and a low /CS.
2. /OE = V_{IL}
3. Transition is measured ± 200mV from steady state voltage.
   This parameter is sampled and not 100% tested.
4. /CS in high for the standby, low for active

WRITE CYCLE 1(1,4,5,8) (/WE Controlled)



WRITE CYCLE 2 (Note 1,4,5,8) (/CS Controlled)



Notes:
1. A write occurs during the overlap of a low /WE and a low /CS.
2. tWR is measured from the earlier of /CS or /WE going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the output must not be applied.
4. If the /CS low transition occur simultaneously with the /WE low transition or after the /WE transition, outputs remain in a high impedance state.
5. Q(data out) is the same phase with the write data of this write cycle.
6. Q(data out) is the read data of the next address.
7. Transition is measured + 200mV from steady state. This parameter is sampled and not 100% tested.
8. /CS in high for the standby, low for active

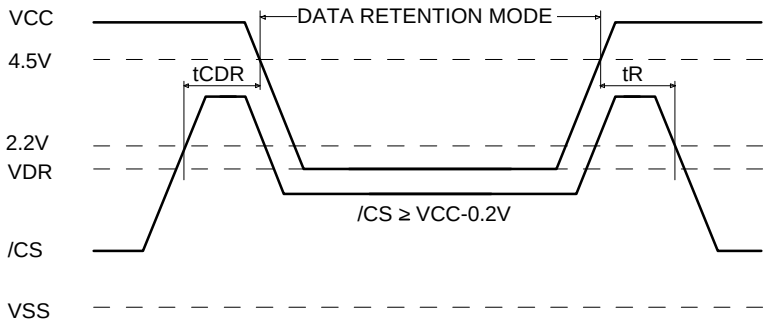
DATA RETENTION ELECTRIC CHARATERISTIC

T_A = 0°C to 70°C (Normal)/-25°C to 85°C (Extended) /-40°C to 85°C (Industrial), unless otherwise specified.

Symbol	Parameter	Test Condition		Min	Typ	Max	Unit
V_{DR}	Vcc for Data Retention	/CS ≥ Vcc - 0.2V, V_{IN} ≥ Vcc - 0.2V or V_{IN} ≤ Vss + 0.2V		2.0	-	-	V
I_{CCDR}	Data Retention Current	Vcc = 3.0V, /CS1≥Vcc - 0.2V, V_{IN} ≥ Vcc - 0.2V or V_{IN} ≤ Vss + 0.2V	L	-	-	50	uA
			LL	-	-	20	uA
			L-E/I	-	-	50	uA
			LL-E/I	-	-	30	uA
tCDR	Chip Deselect to Data Retention Time			0	-	-	ns
tR	Operating Recovery Time			tRC (2)	-	-	ns

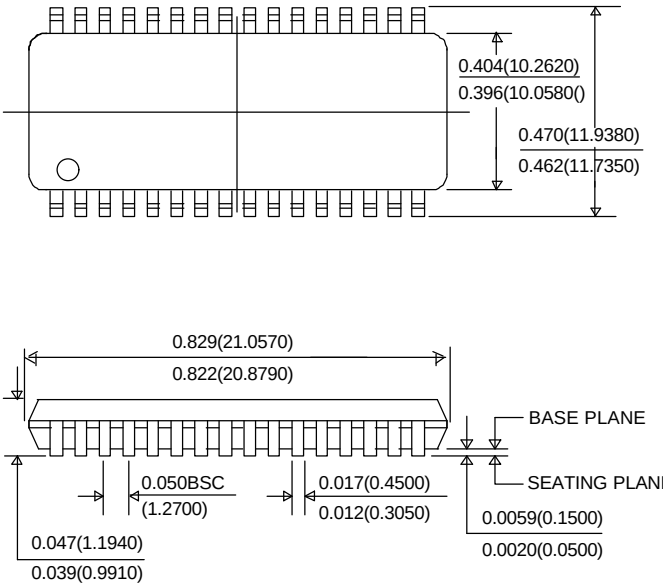
Notes:
1. Typical values are at the condition of T_A = 25°C.
2. tRC is read cycle time.

DATA RETENTION TIMING DIAGRAM



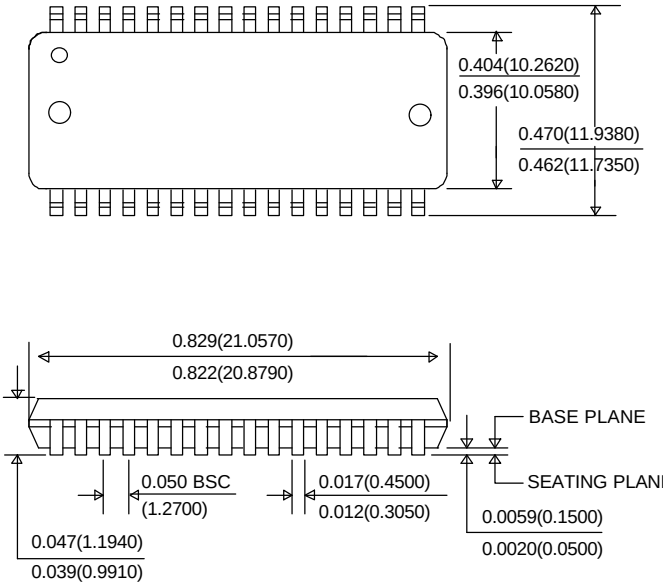
PACKAGE INFORMATION

32pin 400mil Thin Small Outline Package Standard(T2)



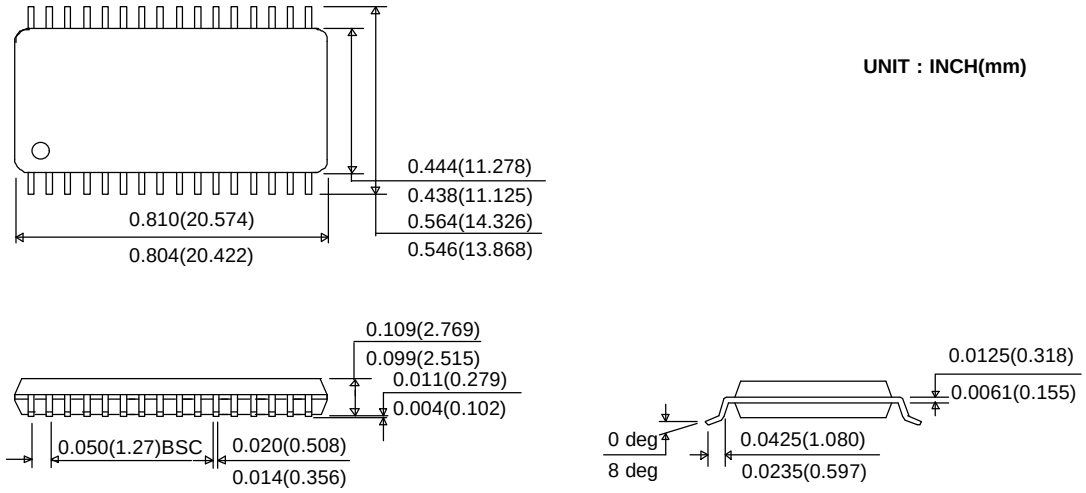
UNIT : INCH(mm) MAX. / MIN.

32pin 400mil Thin Small Outline Package Reversed(R2)

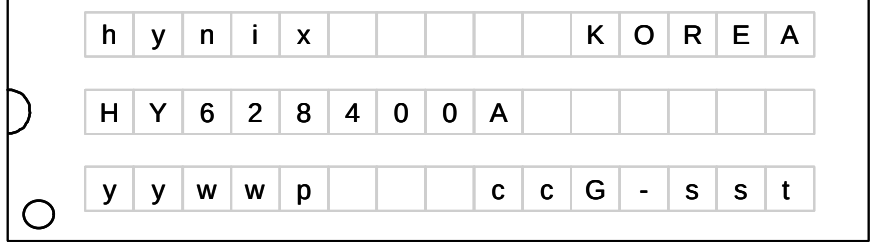
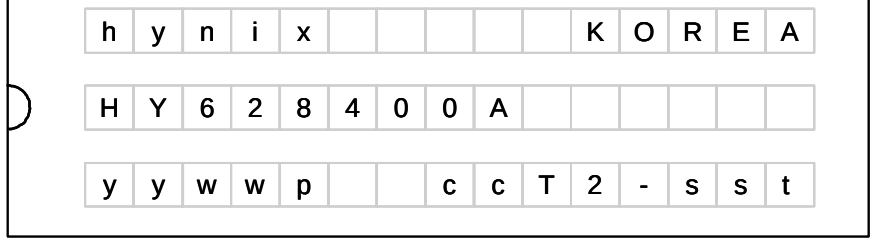


UNIT : INCH(mm) MAX. / MIN.

32pin 525mil Small Outline Package(G)



MARKING INFORMATION

Package	Marking Example
SOP	
TSOP-II	

Index

- **hynix** : hynix Logo
- **KOREA** : Origin Country
- **HY628400A** : Part Name
- **yy** : Year (ex : 00 = year 2000, 01 = year 2001)
- **ww** : Work Week (ex : 12 = ww12)
- **p** : Process Code
- **cc** : Power Consumption
  - L : Low Power
  - LL : Low Low Power
- **G / T2** : Package Type
  - G : SOP
  - T2 : TSOP-II
- **ss** : Speed
  - 55 : 55ns
  - 70 : 70ns
- **t** : Temperature
  - Blank : Commercial (0 ~ 70 °C)
  - E : Extended (-25 ~ 85 °C)
  - I : Industrial (-40 ~ 85 °C)

Note

- Capital Letter : Fixed Item
- Small Letter : Non-fixed Item (Except hynix)

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