256M(8Mx32) GDDR SDRAM

HY5DU573222AFM

Revision History

Revision No.	History	Draft Date	Remark
0.1	Defined target spec.	Dec.2002	
0.2	1) Defined IDD specification 2) Changed VDD_min value of HY5DU573222AFM-36 from 2.375V to 2.2V 3) Changed AC parameters value of HY5DU573222AFM-28/33 - tRCDRD/tRP : from 6 tCK to 5 tCK - tDAL : from 9 tCK to 8 tCK - tRFC : from 19 tCK to 17 tCK 4) Changed tCK_max value of HY5DU573222AFM-33/36/4 from 6ns to 10ns 5) Typo corrected	Mar. 2003	
0.3	1) Changed VDD_min value of HY5DU573222AFM-33 from 2.375V to 2.2V 2) Changed VDD_min value of HY5DU573222AFM-36 from 2.2V to 2.375V	Apr. 2003	
0.4	1) Changed CAS Latency of HY5DU573222AFM-28 from CL5 to CL4 2) Changed VDD_min value of HY5DU573222AFM-28/25 from 2.66V to 2.55V 3) Changed VDD_max value of HY5DU573222AFM-28/25 from 2.94V to 2.95V	June 2003	
0.5	Changed tRAS_max Value from 120K to 100K in All Frequency	Aug. 2003	

DESCRIPTION

The Hynix HY5DU573222AFM is a 268,435,456-bit CMOS Double Data Rate(DDR) Synchronous DRAM which consists of two 128Mbit(x32) - Multi-chip-, ideally suited for the point-to-point applications which requires high bandwidth.

The Hynix 8Mx32 DDR SDRAMs offer fully synchronous operations referenced to both rising and falling edges of the clock. While all addresses and control inputs are latched on the rising edges of the CK (falling edges of the /CK), Data, Data strobes and Write data masks inputs are sampled on both rising and falling edges of it. The data paths are internally pipelined and 2-bit prefetched to achieve very high bandwidth. All input and output voltage levels are compatible with SSTL_2.

FEATURES

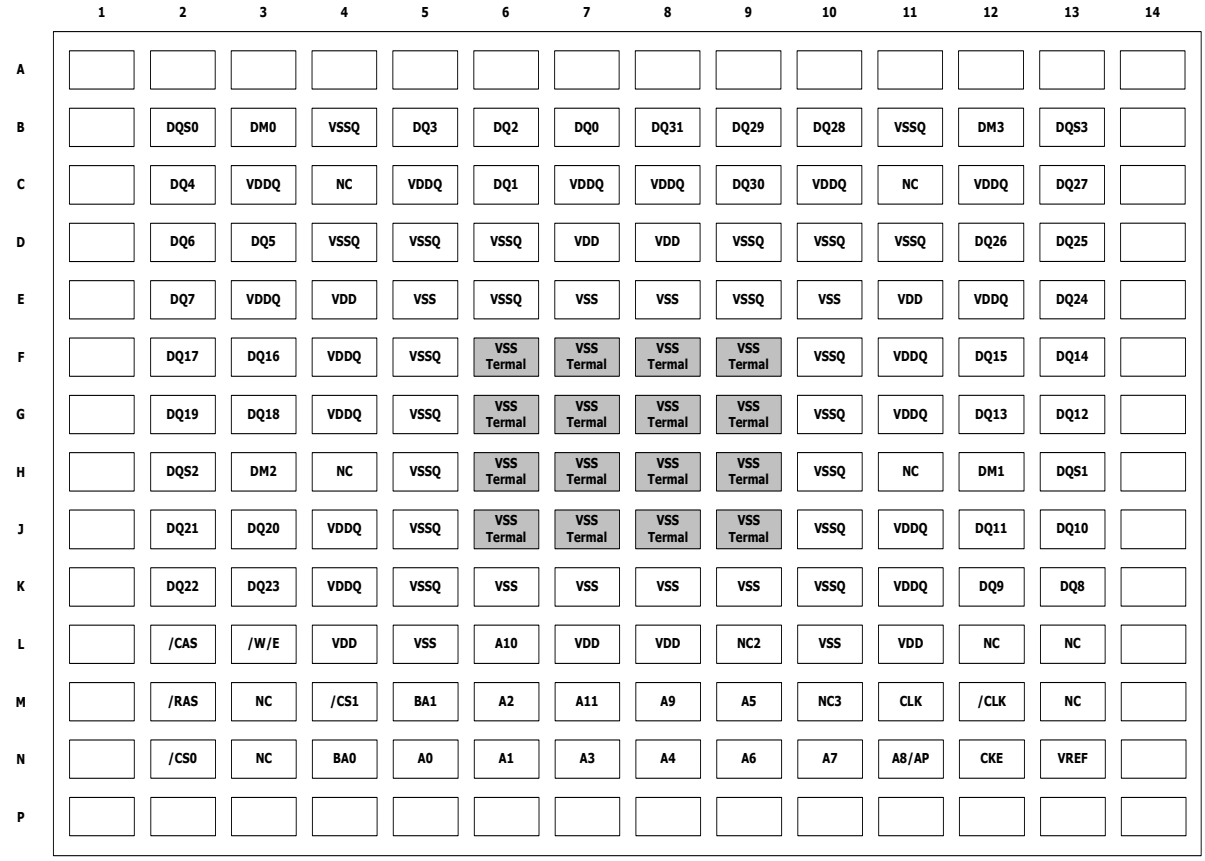
- 2.5V +/- 5% V_{DD} and V_{DDQ} power supply supports 300/275/250MHz
- 2.8V VDD and VDDQ wide range min/max power supply supports 400/350Mhz
- All inputs and outputs are compatible with SSTL_2 interface
- 12mm x 12mm, 144ball FBGA with 0.8mm pin pitch
- Fully differential clock inputs (CK, /CK) operation
- The signals of Chip select control the each chip with CS0 and CS1, individually.
- Double data rate interface
- Source synchronous - data transaction aligned to bidirectional data strobe (DQS0 ~ DQS3)
- Data outputs on DQS edges when read (edged DQ) Data inputs on DQS centers when write (centered DQ)
- Data(DQ) and Write masks(DM) latched on the both rising and falling edges of the data strobe
- All addresses and control inputs except Data, Data strobes and Data masks latched on the rising edges of the clock
- Write mask byte controls by DM (DM0 ~ DM3)
- Programmable /CAS Latency 5 and 4,3 supported
- Programmable Burst Length 2 / 4 / 8 with both sequential and interleave mode
- Internal 4 bank operations with single pulsed /RAS
- tRAS Lock-Out function supported
- Auto refresh and self refresh supported
- 4096 refresh cycles / 32ms

  (Both chips do refresh operation, simultaneously)
- Half strength and Matched Impedance driver option controlled by EMRS

ORDERING INFORMATION

Part No.	Power Supply	Clock Frequency	Max Data Rate	interface	Package
HY5DU573222AFM-25	V_{DD} 2.8V V_{DDQ} 2.8V	400MHz	800Mbps/pin	SSTL_2	12mmx12mm 144Ball FBGA
HY5DU573222AFM-28		350MHz	700Mbps/pin		
HY5DU573222AFM-33	V_{DD} 2.5V V_{DDQ} 2.5V	300MHz	600Mbps/pin		
HY5DU573222AFM-36		275MHz	550Mbps/pin		
HY5DU573222AFM-4		250MHz	500Mbps/pin		

PIN CONFIGURATION (Top View)



	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A														
B		DQS0	DM0	VSSQ	DQ3	DQ2	DQ0	DQ31	DQ29	DQ28	VSSQ	DM3	DQS3	
C		DQ4	VDDQ	NC	VDDQ	DQ1	VDDQ	VDDQ	DQ30	VDDQ	NC	VDDQ	DQ27	
D		DQ6	DQ5	VSSQ	VSSQ	VSSQ	VDD	VDD	VSSQ	VSSQ	VSSQ	DQ26	DQ25	
E		DQ7	VDDQ	VDD	VSS	VSSQ	VSS	VSS	VSSQ	VSS	VDD	VDDQ	DQ24	
F		DQ17	DQ16	VDDQ	VSSQ	VSS Termal	VSS Termal	VSS Termal	VSS Termal	VSSQ	VDDQ	DQ15	DQ14	
G		DQ19	DQ18	VDDQ	VSSQ	VSS Termal	VSS Termal	VSS Termal	VSS Termal	VSSQ	VDDQ	DQ13	DQ12	
H		DQS2	DM2	NC	VSSQ	VSS Termal	VSS Termal	VSS Termal	VSS Termal	VSSQ	NC	DM1	DQS1	
J		DQ21	DQ20	VDDQ	VSSQ	VSS Termal	VSS Termal	VSS Termal	VSS Termal	VSSQ	VDDQ	DQ11	DQ10	
K		DQ22	DQ23	VDDQ	VSSQ	VSS	VSS	VSS	VSS	VSSQ	VDDQ	DQ9	DQ8	
L		/CAS	/W/E	VDD	VSS	A10	VDD	VDD	NC2	VSS	VDD	NC	NC	
M		/RAS	NC	/CS1	BA1	A2	A11	A9	A5	NC3	CLK	/CLK	NC	
N		/CS0	NC	BA0	A0	A1	A3	A4	A6	A7	A8/AP	CKE	VREF	
P														

Note :
1. Outer ball, A1~A14, P1~P14, A1~P1, A14~P14 are depopulated.
2. Ball L9(NC2) is reserved for A12.
3. Ball M10(NC3) is reserved for BA2.

ROW and COLUMN ADDRESS TABLE

Items	8Mx32
Organization	1M x 32 x 4banks x 2chip
Row Address	A0 ~ A11
Column Address	A0 ~ A7
Bank Address	BA0, BA1
Auto Precharge Flag	A8
Refresh	4K
Chip Selection	CS0, CS1

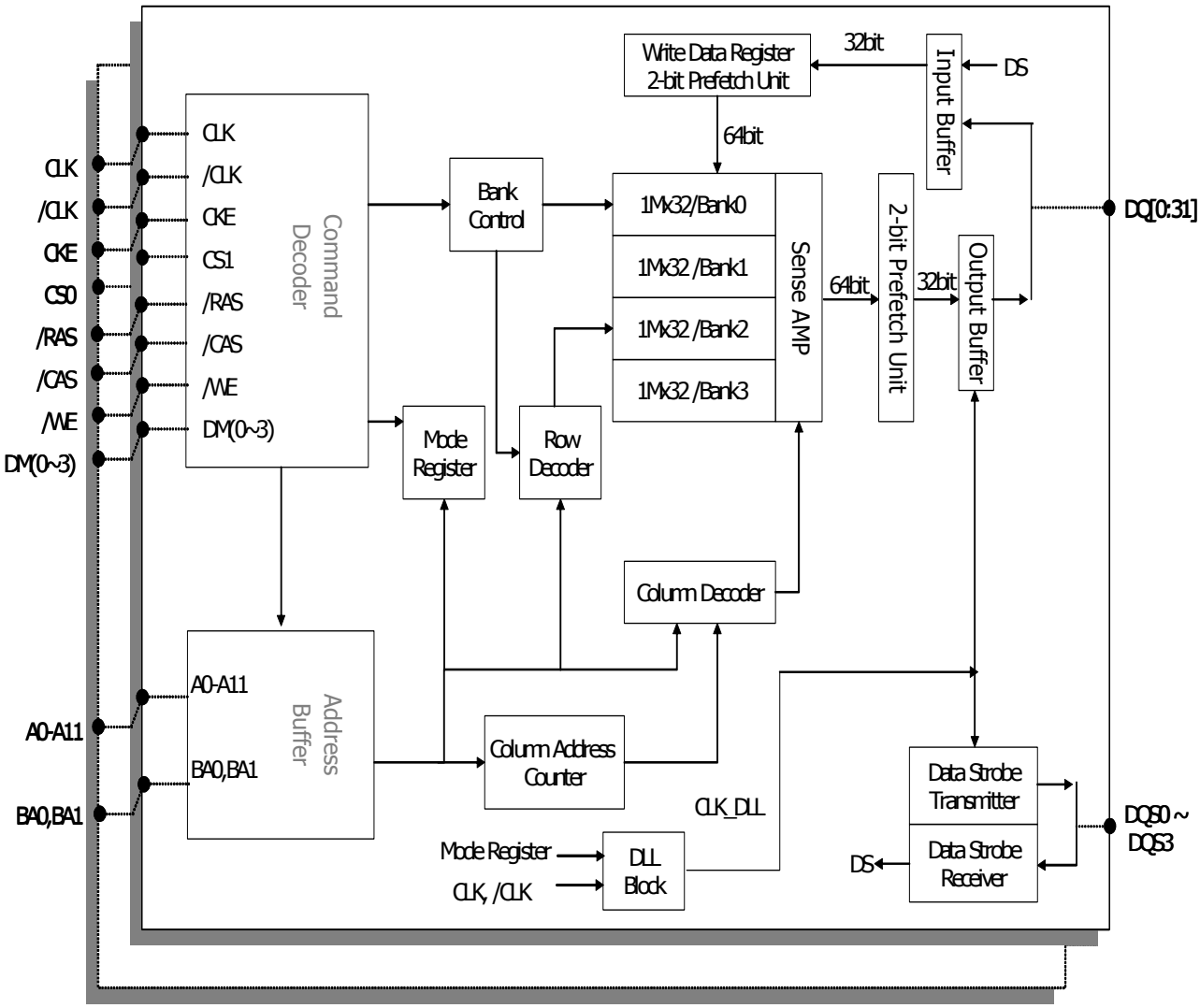
Note:
1. 8Mx32 DDR is composed of two 4Mx32 DDR.
2. Multi-chip(8Mx32 DDR) is controlled by CS0 and CS1, individually.

PIN DESCRIPTION

PIN	TYPE	DESCRIPTION
CK, /CK	Input	Clock: CK and /CK are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of /CK. Output (read) data is referenced to the crossings of CK and /CK (both directions of crossing).
CKE	Input	Clock Enable: CKE HIGH activates, and CKE LOW deactivates internal clock signals, and device input buffers and output drivers. Taking CKE LOW provides PRECHARGE POWER DOWN and SELF REFRESH operation (all banks idle), or ACTIVE POWER DOWN (row ACTIVE in any bank). CKE is synchronous for POWER DOWN entry and exit, and for SELF REFRESH entry. CKE is asynchronous for SELF REFRESH exit, and for output disable. CKE must be maintained high throughout READ and WRITE accesses. Input buffers, excluding CK, /CK and CKE are disabled during POWER DOWN. Input buffers, excluding CKE are disabled during SELF REFRESH. CKE is an SSTL_2 input, but will detect an LVCMOS LOW level after Vdd is applied.
/CS0, /CS1	Input	Chip Select : Enables or disables all inputs except CK, /CK, CKE, DQS and DM. All commands are masked when CS0 or CS1 is registered high. CS0 or CS1 provides for external bank selection on systems with multiple banks. CS0 and CS1 are considered part of the command code. When it is the operationg state of MRS, Power up sequence, EMRS, it should be enabled in pairs. Except this case, it can be operated, individually.
BA0, BA1	Input	Bank Address Inputs: BA0 and BA1 define to which bank an ACTIVE, Read, Write or PRECHARGE command is being applied.
A0 ~ A11	Input	Address Inputs: Provide the row address for ACTIVE commands, and the column address and AUTO PRECHARGE bit for READ/WRITE commands, to select one location out of the memory array in the respective bank. A8 is sampled during a precharge command to determine whether the PRECHARGE applies to one bank (A8 LOW) or all banks (A8 HIGH). If only one bank is to be precharged, the bank is selected by BA0, BA1. The address inputs also provide the op code during a MODE REGISTER SET command. BA0 and BA1 define which mode register is loaded during the MODE REGISTER SET command (MRS or EMRS).
/RAS, /CAS, /WE	Input	Command Inputs: /RAS, /CAS and /WE (along with /CS) define the command being entered.
DM0 ~ DM3	Input	Input Data Mask: DM(0~3) is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading. DM0 corresponds to the data on DQ0-Q7; DM1 corresponds to the data on DQ8-Q15; DM2 corresponds to the data on DQ16-Q23; DM3 corresponds to the data on DQ24-Q31.
DQS0~DQS3	I/O	Data Strobe: Output with read data, input with write data. Edge aligned with read data, centered in write data. Used to capture write data. DQS0 corresponds to the data on DQ0-Q7; DQS1 corresponds to the data on DQ8-Q15; DQS2 corresponds to the data on DQ16-Q23; DQS3 corresponds to the data on DQ24-Q31
DQ0 ~ DQ31	I/O	Data input / output pin : Data Bus
VDD/VSS	Supply	Power supply for internal circuits and input buffers.
VDDQ/VSSQ	Supply	Power supply for output buffers for noise immunity.
VREF	Supply	Reference voltage for inputs for SSTL interface.
NC	NC	No connection.

FUNCTIONAL BLOCK DIAGRAM

(4Banks x 1Mbit x 32 I/O) x 2Chips Double Data Rate Synchronous DRAM



SIMPLIFIED COMMAND TRUTH TABLE

Command		CKEn-1	CKEn	CS0/ CS1	RAS	CAS	WE	ADDR	A8/ AP	BA	Note
Extended Mode Register Set		H	X	L	L	L	L	OP code			1,2,6
Mode Register Set		H	X	L	L	L	L	OP code			1,2,6
Device Deselect		H	X	H	X	X	X	X			1
No Operation				L	H	H	H				
Bank Active		H	X	L	L	H	H	RA		V	1
Read		H	X	L	H	L	H	CA	L	V	1,7
Read with Autoprecharge									H		1,3,7
Write		H	X	L	H	L	L	CA	L	V	1,7
Write with Autoprecharge									H		1,4,7
Precharge All Banks		H	X	L	L	H	L	X	H	X	1,5
Precharge selected Bank									L	V	1
Read Burst Stop		H	X	L	H	H	L	X			1
Auto Refresh		H	H	L	L	L	H	X			1
Self Refresh	Entry	H	L	L	L	L	H	X			1,6
	Exit	L	H	H	X	X	X				1,6
				L	H	H	H				
Precharge Power Down Mode	Entry	H	L	H	X	X	X	X			1,6
				L	H	H	H				1,6
	Exit	L	H	H	X	X	X				1,6
				L	H	H	H				1,6
Active Power Down Mode	Entry	H	L	H	X	X	X	X			1,6
				L	V	V	V				1,6
	Exit	L	H	X							1,6

(H=Logic High Level, L=Logic Low Level, X=Don't Care, V=Valid Data Input, OP Code=Operand Code, NOP=No Operation)

Note :

1. DM(0~3) states are Don't Care. Refer to below Write Mask Truth Table.
2. OP Code(Operand Code) consists of A0~A11 and BA0~BA1 used for Mode Register setting during Extended MRS or MRS. Before entering Mode Register Set mode, all banks must be in a precharge state and MRS command can be issued after tRP period from Prechagre command.
3. If a Read with Autoprecharge command is detected by memory component in CK(n), then there will be no command presented to activated bank until CK(n+BL/2+tRP).
4. If a Write with Autoprecharge command is detected by memory component in CK(n), then there will be no command presented to activated bank until CK(n+BL/2+1+tDPL+tRP). Last Data-In to Prechage delay(tDPL) which is also called Write Recovery Time (tWR) is needed to guarantee that the last data has been completely written.
5. If A8/AP is High when Precharge command being issued, BA0/BA1 are ignored and all banks are selected to be precharged.
6. Both of CS0 & CS1 should be enabled simultaneously.

WRITE MASK TRUTH TABLE

Function	CKEn-1	CKEn	/CS0, /CS1, /RAS, /CAS, /WE	DM(0~3)	ADDR	A8/ AP	BA	Note
Data Write	H	X	X	L	X			1,2
Data-In Mask	H	X	X	H	X			1,2

Note :

1. Write Mask command masks burst write data with reference to DQS(0~3) and it is not related with read data.
2. DM0 corresponds to the data on DQ0-Q7; DM1 corresponds to the data on DQ8-Q15; DM2 corresponds to the data on DQ16-Q23; DM3 corresponds to the data on DQ24-Q31.

OPERATION COMMAND TRUTH TABLE - I

Current State	/CS0 /CS1	/RAS	/CAS	/WE	Address	Command	Action
IDLE	H	X	X	X	X	DSEL	NOP or power down[3]
	L	H	H	H	X	NOP	NOP or power down[3]
	L	H	H	L	X	BST	ILLEGAL[4]
	L	H	L	H	BA, CA, AP	READ/READAP	ILLEGAL[4]
	L	H	L	L	BA, CA, AP	WRITE/WRITEAP	ILLEGAL[4]
	L	L	H	H	BA, RA	ACT	Row Activation
	L	L	H	L	BA, AP	PRE/PALL	NOP
	L	L	L	H	X	AREF/SREF	Auto Refresh or Self Refresh[5]
	L	L	L	L	OPCODE	MRS *12	Mode Register Set
ROW ACTIVE	H	X	X	X	X	DSEL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	X	BST	ILLEGAL[4]
	L	H	L	H	BA, CA, AP	READ/READAP*13	Begin read : optional AP[6]
	L	H	L	L	BA, CA, AP	WRITE/WRITEAP*13	Begin write : optional AP[6]
	L	L	H	H	BA, RA	ACT	ILLEGAL[4]
	L	L	H	L	BA, AP	PRE/PALL	Precharge[7]
	L	L	L	H	X	AREF/SREF	ILLEGAL[11]
	L	L	L	L	OPCODE	MRS	ILLEGAL[11]
READ	H	X	X	X	X	DSEL	Continue burst to end
	L	H	H	H	X	NOP	Continue burst to end
	L	H	H	L	X	BST	Terminate burst
	L	H	L	H	BA, CA, AP	READ/READAP*13	Term burst, new read:optional AP[8]
	L	H	L	L	BA, CA, AP	WRITE/WRITEAP	ILLEGAL
	L	L	H	H	BA, RA	ACT	ILLEGAL[4]
	L	L	H	L	BA, AP	PRE/PALL	Term burst, precharge
	L	L	L	H	X	AREF/SREF	ILLEGAL[11]
	L	L	L	L	OPCODE	MRS	ILLEGAL[11]
WRITE	H	X	X	X	X	DSEL	Continue burst to end
	L	H	H	H	X	NOP	Continue burst to end
	L	H	H	L	X	BST	ILLEGAL[4]
	L	H	L	H	BA, CA, AP	READ/READAP*13	Term burst, new read:optional AP[8]
	L	H	L	L	BA, CA, AP	WRITE/WRITEAP*13	Term burst, new write:optional AP

OPERATION COMMAND TRUTH TABLE - II

Current State	/CS0 /CS1	/RAS	/CAS	/WE	Address	Command	Action
WRITE	L	L	H	H	BA, RA	ACT	ILLEGAL[4]
	L	L	H	L	BA, AP	PRE/PALL	Term burst, precharge
	L	L	L	H	X	AREF/SREF	ILLEGAL[11]
	L	L	L	L	OPCODE	MRS	ILLEGAL[11]
READ WITH AUTOPRE-CHARGE	H	X	X	X	X	DSEL	Continue burst to end
	L	H	H	H	X	NOP	Continue burst to end
	L	H	H	L	X	BST	ILLEGAL
	L	H	L	H	BA, CA, AP	READ/READAP	ILLEGAL[10]
	L	H	L	L	BA, CA, AP	WRITE/WRITEAP	ILLEGAL[10]
	L	L	H	H	BA, RA	ACT	ILLEGAL[4,10]
	L	L	H	L	BA, AP	PRE/PALL	ILLEGAL[4,10]
	L	L	L	H	X	AREF/SREF	ILLEGAL[11]
	L	L	L	L	OPCODE	MRS	ILLEGAL[11]
WRITE AUTOPRE-CHARGE	H	X	X	X	X	DSEL	Continue burst to end
	L	H	H	H	X	NOP	Continue burst to end
	L	H	H	L	X	BST	ILLEGAL
	L	H	L	H	BA, CA, AP	READ/READAP	ILLEGAL[10]
	L	H	L	L	BA, CA, AP	WRITE/WRITEAP	ILLEGAL[10]
	L	L	H	H	BA, RA	ACT	ILLEGAL[4,10]
	L	L	H	L	BA, AP	PRE/PALL	ILLEGAL[4,10]
	L	L	L	H	X	AREF/SREF	ILLEGAL[11]
	L	L	L	L	OPCODE	MRS	ILLEGAL[11]
PRE-CHARGE	H	X	X	X	X	DSEL	NOP-Enter IDLE after tRP
	L	H	H	H	X	NOP	NOP-Enter IDLE after tRP
	L	H	H	L	X	BST	ILLEGAL[4]
	L	H	L	H	BA, CA, AP	READ/READAP	ILLEGAL[4,10]
	L	H	L	L	BA, CA, AP	WRITE/WRITEAP	ILLEGAL[4,10]
	L	L	H	H	BA, RA	ACT	ILLEGAL[4,10]
	L	L	H	L	BA, AP	PRE/PALL	NOP-Enter IDLE after tRP
	L	L	L	H	X	AREF/SREF	ILLEGAL[11]
	L	L	L	L	OPCODE	MRS	ILLEGAL[11]

OPERATION COMMAND TRUTH TABLE - III

Current State	/CS0 /CS1	/RAS	/CAS	/WE	Address	Command	Action
ROW ACTIVATING	H	X	X	X	X	DSEL	NOP - Enter ROW ACT after tRCD
	L	H	H	H	X	NOP	NOP - Enter ROW ACT after tRCD
	L	H	H	L	X	BST	ILLEGAL[4]
	L	H	L	H	BA, CA, AP	READ/READAP	ILLEGAL[4,10]
	L	H	L	L	BA, CA, AP	WRITE/WRITEAP	ILLEGAL[4,10]
	L	L	H	H	BA, RA	ACT	ILLEGAL[4,9,10]
	L	L	H	L	BA, AP	PRE/PALL	ILLEGAL[4,10]
	L	L	L	H	X	AREF/SREF	ILLEGAL[11]
	L	L	L	L	OPCODE	MRS	ILLEGAL[11]
WRITE RECOVERING	H	X	X	X	X	DSEL	NOP - Enter ROW ACT after tWR
	L	H	H	H	X	NOP	NOP - Enter ROW ACT after tWR
	L	H	H	L	X	BST	ILLEGAL[4]
	L	H	L	H	BA, CA, AP	READ/READAP	ILLEGAL
	L	H	L	L	BA, CA, AP	WRITE/WRITEAP	ILLEGAL
	L	L	H	H	BA, RA	ACT	ILLEGAL[4,10]
	L	L	H	L	BA, AP	PRE/PALL	ILLEGAL[4,11]
	L	L	L	H	X	AREF/SREF	ILLEGAL[11]
	L	L	L	L	OPCODE	MRS	ILLEGAL[11]
WRITE RECOVERING WITH AUTOPRE-CHARGE	H	X	X	X	X	DSEL	NOP - Enter precharge after tDPL
	L	H	H	H	X	NOP	NOP - Enter precharge after tDPL
	L	H	H	L	X	BST	ILLEGAL[4]
	L	H	L	H	BA, CA, AP	READ/READAP	ILLEGAL[4,8,10]
	L	H	L	L	BA, CA, AP	WRITE/WRITEAP	ILLEGAL[4,10]
	L	L	H	H	BA, RA	ACT	ILLEGAL[4,10]
	L	L	H	L	BA, AP	PRE/PALL	ILLEGAL[4,11]
	L	L	L	H	X	AREF/SREF	ILLEGAL[11]
	L	L	L	L	OPCODE	MRS	ILLEGAL[11]
REFRESHING	H	X	X	X	X	DSEL	NOP - Enter IDLE after tRC
	L	H	H	H	X	NOP	NOP - Enter IDLE after tRC
	L	H	H	L	X	BST	ILLEGAL[11]
	L	H	L	H	BA, CA, AP	READ/READAP	ILLEGAL[11]

OPERATION COMMAND TRUTH TABLE - IV

Current State	/CS0 /CS1	/RAS	/CAS	/WE	Address	Command	Action
WRITE	L	H	L	L	BA, CA, AP	WRITE/WRITEAP	ILLEGAL[11]
	L	L	H	H	BA, RA	ACT	ILLEGAL[11]
	L	L	H	L	BA, AP	PRE/PALL	ILLEGAL[11]
	L	L	L	H	X	AREF/SREF	ILLEGAL[11]
	L	L	L	L	OPCODE	MRS	ILLEGAL[11]
MODE REGISTER ACCESSING	H	X	X	X	X	DSEL	NOP - Enter IDLE after tMRD
	L	H	H	H	X	NOP	NOP - Enter IDLE after tMRD
	L	H	H	L	X	BST	ILLEGAL[11]
	L	H	L	H	BA, CA, AP	READ/READAP	ILLEGAL[11]
	L	H	L	L	BA, CA, AP	WRITE/WRITEAP	ILLEGAL[11]
	L	L	H	H	BA, RA	ACT	ILLEGAL[11]
	L	L	H	L	BA, AP	PRE/PALL	ILLEGAL[11]
	L	L	L	H	X	AREF/SREF	ILLEGAL[11]
	L	L	L	L	OPCODE	MRS	ILLEGAL[11]

Note :

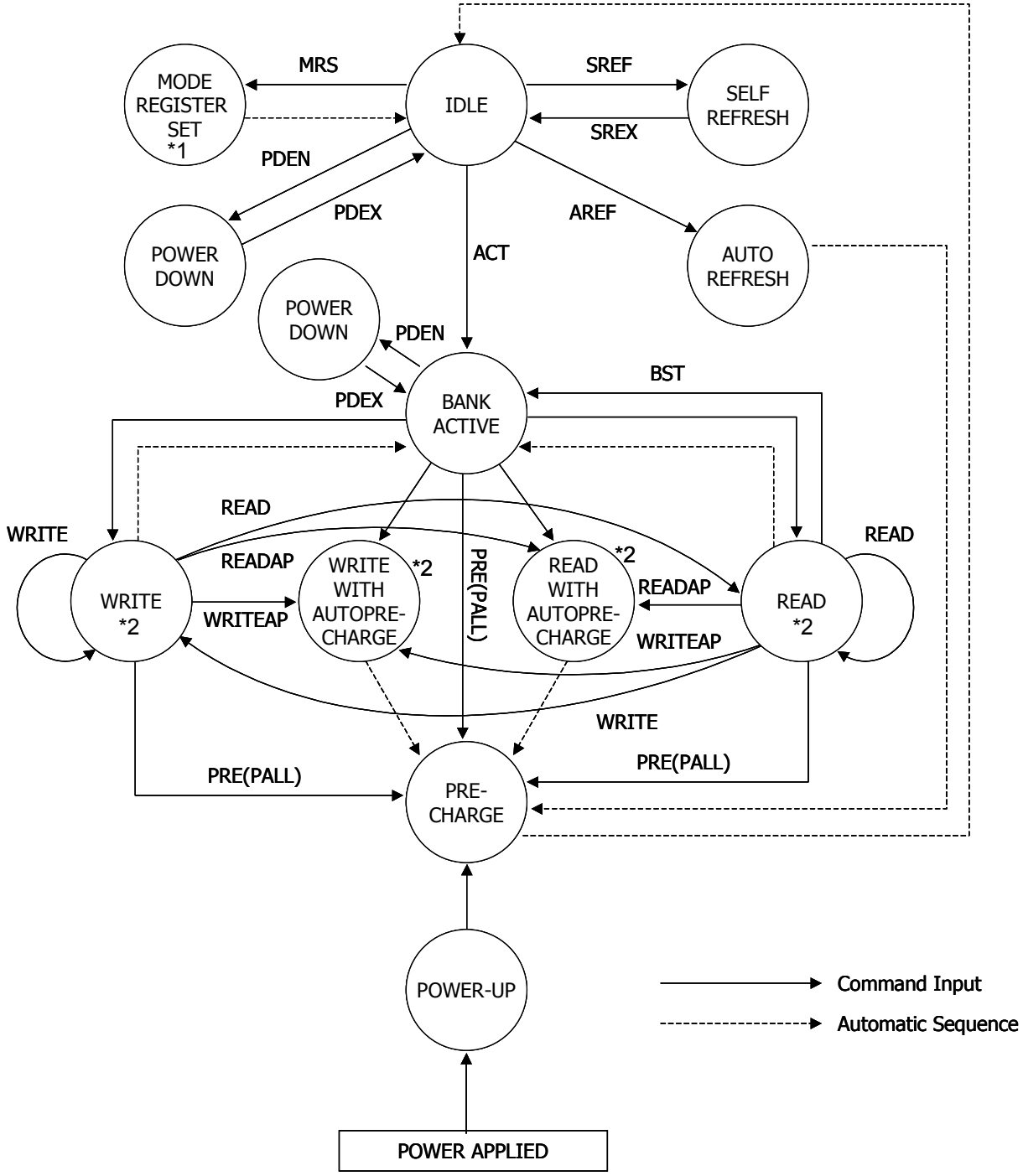
1. H - Logic High Level, L - Logic Low Level, X - Don't Care, V - Valid Data Input,
   BA - Bank Address, AP - AutoPrecharge Address, CA - Column Address, RA - Row Address, NOP - NO Operation.
2. All entries assume that CKE was active(high level) during the preceding clock cycle.
3. If both banks are idle and CKE is inactive(low level), then in power down mode.
4. Illegal to bank in specified state. Function may be legal in the bank indicated by Bank Address(BA) depending on the state of that bank.
5. If both banks are idle and CKE is inactive(low level), then self refresh mode.
6. Illegal if tRCD is not met.
7. Illegal if tRAS is not met.
8. Must satisfy bus contention, bus turn around, and/or write recovery requirements.
9. Illegal if tRRD is not met.
10. Illegal for single bank, but legal for other banks in multi-bank devices.
11. Illegal for all banks.
12. Both of CS0 & CS1 should be enabled in pairs.
13. One of CS0 & CS1 should be enabled, individually.

CKE FUNCTION TRUTH TABLE

Current State	CKEn-1	CKEn	/CS0 /CS1	/RAS	/CAS	/WE	/ADD	Action
SELF REFRESH[1]	H	X	X	X	X	X	X	INVALID
	L	H	H	X	X	X	X	Exit self refresh, enter idle after tSREX*
	L	H	L	H	H	H	X	Exit self refresh, enter idle after tSREX*
	L	H	L	H	H	L	X	ILLEGAL
	L	H	L	H	L	X	X	ILLEGAL
	L	H	L	L	X	X	X	ILLEGAL
	L	L	X	X	X	X	X	NOP, continue self refresh
POWER DOWN[2]	H	X	X	X	X	X	X	INVALID
	L	H	H	X	X	X	X	Exit power down, enter idle*
	L	H	L	H	H	H	X	Exit power down, enter idle*
	L	H	L	H	H	L	X	ILLEGAL
	L	H	L	H	L	X	X	ILLEGAL
	L	H	L	L	X	X	X	ILLEGAL
	L	L	X	X	X	X	X	NOP, continue power down mode
ALL BANKS IDLE[4]	H	H	X	X	X	X	X	See operation command truth table
	H	L	L	L	L	H	X	Enter self refresh*
	H	L	H	X	X	X	X	Exit power down*
	H	L	L	H	H	H	X	Exit power down*
	H	L	L	H	H	L	X	ILLEGAL
	H	L	L	H	L	X	X	ILLEGAL
	H	L	L	L	H	X	X	ILLEGAL
	H	L	L	L	L	L	X	ILLEGAL
	L	L	X	X	X	X	X	NOP
ANY STATE OTHER THAN ABOVE	H	H	X	X	X	X	X	See operation command truth table
	H	L	X	X	X	X	X	ILLEGAL[5]
	L	H	X	X	X	X	X	INVALID
	L	L	X	X	X	X	X	INVALID

Note :
When CKE=L, all DQ and DQS(0~3) must be in Hi-Z state.
1. CKE and /CS must be kept high for a minimum of 200 stable input clocks before issuing any command.
2. All command can be stored after 2 clocks from low to high transition of CKE.
3. Illegal if CK is suspended or stopped during the power down mode.
4. Self refresh can be entered only from the all banks idle state.
5. Disabling CK may cause malfunction of any bank which is in active state.
6. * Both CSO & CSI should be emabled, simultaneouly.

SIMPLIFIED STATE DIAGRAM



Note:
*1.Both of CS0 and CS1 should be enabled in pairs.
*2.Both of CS0 and CS1 should be enabled, individually.

POWER-UP SEQUENCE AND DEVICE INITIALIZATION

DDR SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. Except for CKE, inputs are not recognized as valid until after VREF is applied. CKE is an SSTL_2 input, but will detect an LVCMOS LOW level after VDD is applied. Maintaining an LVCMOS LOW level on CKE during power-up is required to guarantee that the DQ and DQS outputs will be in the High-Z state, where they will remain until driven in normal operation (by a read access). After all power supply and reference voltages are stable, and the clock is stable, the DDR SDRAM requires a 200us delay prior to applying an executable command.

Once the 200us delay has been satisfied, a DESELECT or NOP command should be applied, and CKE should be brought HIGH. Following the NOP command, a PRECHARGE ALL command should be applied. Next a EXTENDED MODE REGISTER SET command should be issued for the Extended Mode Register, to enable the DLL, then a MODE REGISTER SET command should be issued for the Mode Register, to reset the DLL, and to program the operating parameters. After the DLL reset, tXSRD(DLL locking time) should be satisfied for read command. After the Mode Register set command, a PRECHARGE ALL command should be applied, placing the device in the all banks idle state.

Once in the idle state, two AUTO REFRESH cycles must be performed. Additionally, a MODE REGISTER SET command for the Mode Register, with the reset DLL bit deactivated low (i.e. to program operating parameters without resetting the DLL) must be performed. Following these cycles, the DDR SDRAM is ready for normal operation.

1. Apply power - VDD, VDDQ, VTT, VREF in the following power up sequencing and attempt to maintain CKE at LVCMOS low state. (All the other input pins may be undefined.

No power sequencing is specified during power up or power down given the following cirteria :

- VDD and VDDQ are driven from a single power converter output.
- VTT is limited to 1.44V (reflecting VDDQ(max)/2 + 50mV VREF variation + 40mV VTT variation).
- VREF tracks VDDQ/2.
- A minimum resistance of 42 ohms (22 ohm series resistor + 22 ohm parallel resistor - 5% tolerance) limits the input current from the VTT supply into any pin.

If the above criteria cannot be met by the system design, then the following sequencing and voltage relationship must be adhered to during power up :

Voltage description	Sequencing	Voltage relationship to avoid latch-up
VDDQ	After or with VDD	< VDD + 0.3V
VTT	After or with VDDQ	< VDDQ + 0.3V
VREF	After or with VDDQ	< VDDQ + 0.3V

2. Start clock and maintain stable clock for a minimum of 200usec.

3. After stable power and clock, apply NOP condition and take CKE high.

4. Issue Extended Mode Register Set (EMRS) to enable DLL.

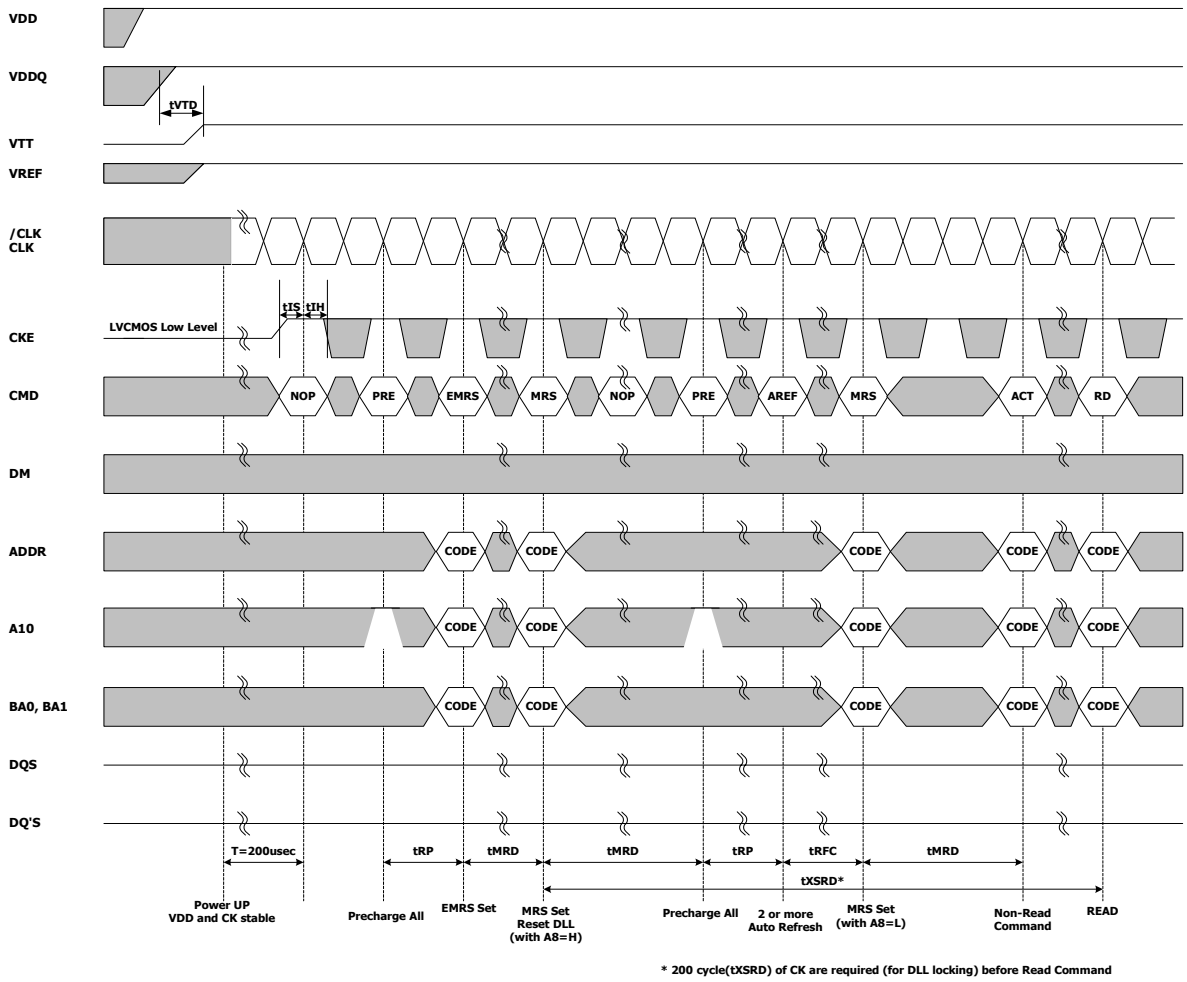
5. Issue Mode Register Set (MRS) to reset DLL and set device to idle state with bit A8=high. (An additional 200 cycles(tXSRD) of clock are required for locking DLL)

6. Issue Precharge commands for all banks of the device.

7. Issue 2 or more Auto Refresh commands.

8. Issue a Mode Register Set command to initialize the mode register with bit A8 = Low.

Power-Up Sequence



MODE REGISTER SET (MRS)

The mode register is used to store the various operating modes such as /CAS latency, addressing mode, burst length, burst type, test mode, DLL reset. The mode register is program via MRS command. This command is issued by the low signals of /RAS, /CAS, /CS0 ,/CS1, /WE and BA0. This command can be issued only when all banks are in idle state and CKE must be high at least one cycle before the Mode Register Set Command can be issued. Two cycles are required to write the data in mode register. During the the MRS cycle, any command cannot be issued. Once mode register field is determined, the information will be held until resetted by another MRS command.

BA1	BA0	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	RFU			DR	TM	CAS Latency			BT	Burst Length		

BA0	MRS Type
0	MRS
1	EMRS

A7	Test Mode
0	Normal
1	Vendor test mode

A8	DLL Reset
0	No
1	Yes

A6	A5	A4	CAS Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	Reserved
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	Reserved
1	1	1	Reserved

A2	A1	A0	Burst Length	
			Sequential	Interleave
0	0	0	Reserved	Reserved
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserved	Reserved
1	0	1	Reserved	Reserved
1	1	0	Reserved	Reserved
1	1	1	Reserved	Reserved

A3	Burst Type
0	Sequential
1	Interleave

BURST DEFINITION

Burst Length	Starting Address (A2,A1,A0)	Sequential	Interleave
2	XX0	0, 1	0, 1
	XX1	1, 0	1, 0
4	X00	0, 1, 2, 3	0, 1, 2, 3
	X01	1, 2, 3, 0	1, 0, 3, 2
	X10	2, 3, 0, 1	2, 3, 0, 1
	X11	3, 0, 1, 2	3, 2, 1, 0
8	000	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
	001	1, 2, 3, 4, 5, 6, 7, 0	1, 0, 3, 2, 5, 4, 7, 6
	010	2, 3, 4, 5, 6, 7, 0, 1	2, 3, 0, 1, 6, 7, 4, 5
	011	3, 4, 5, 6, 7, 0, 1, 2	3, 2, 1, 0, 7, 6, 5, 4
	100	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
	101	5, 6, 7, 0, 1, 2, 3, 4	5, 4, 7, 6, 1, 0, 3, 2
	110	6, 7, 0, 1, 2, 3, 4, 5	6, 7, 4, 5, 2, 3, 0, 1
	111	0, 1, 2, 3, 4, 5, 6, 7	7, 6, 5, 4, 3, 2, 1, 0

BURST LENGTH & TYPE

Read and write accesses to the DDR SDRAM are burst oriented, with the burst length being programmable. The burst length determines the maximum number of column locations that can be accessed for a given Read or Write command. Burst lengths of 2, 4 or 8 locations are available for both the sequential and the interleaved burst types. Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

When a Read or Write command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst wraps within the block if a boundary is reached. The block is uniquely selected by A1-Ai when the burst length is set to two, by A2-Ai when the burst length is set to four and by A3-Ai when the burst length is set to eight (where Ai is the most significant column address bit for a given configuration). The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. The programmed burst length applies to both Read and Write bursts.

Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit A3. The ordering of accesses within a burst is determined by the burst length, the burst type and the starting column address, as shown in Burst Definitionon Table

CAS LATENCY

The Read latency or CAS latency is the delay in clock cycles between the registration of a Read command and the availability of the first burst of output data. The latency can be programmed 3, 4 or 5 clocks.

If a Read command is registered at clock edge n, and the latency is m clocks, the data is available nominally coincident with clock edge n + m.

Reserved states should not be used as unknown operation or incompatibility with future versions may result.

DLL RESET

The DLL must be enabled for normal operation. DLL enable is required during power up initialization, and upon returning to normal operation after having disabled the DLL for the purpose of debug or evaluation. The DLL is automatically disabled when entering self refresh operation and is automatically re-enabled upon exit of self refresh operation. Any time the DLL is enabled, 200 clock cycles must occur to allow time for the internal clock to lock to the externally applied clock before an any command can be issued.

OUTPUT DRIVER IMPEDANCE CONTROL

This device supports both Half strength driver and Matched impedance driver, intended for lighter load and/or point-to-point environments. Half strength driver is to define about 50% of Full drive strength which is specified to be SSTL_2, Class II, and Matched impedance driver, about 30% of Full drive strength.

EXTENDED MODE REGISTER SET (EMRS)

The Extended Mode Register controls functions beyond those controlled by the Mode Register; these additional functions include DLL enable/disable, output driver strength selection(optional). These functions are controlled via the bits shown below. The Extended Mode Register is programmed via the Mode Register Set command (BA0=1 and BA1=0) and will retain the stored information until it is programmed again or the device loses power.

The Extended Mode Register must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time before initiating any subsequent operation. Violating either of these requirements will result in unspecified operation.

BA1	BA0	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	1	RFU*					DS	RFU*			DS	DS	DLL

BA0	MRS Type
0	MRS
1	EMRS

A0	DLL enable
0	Enable
1	Diable

A2	A6	A1	Output Driver Impedance Control
0	0	0	RFU*
0	0	1	Half (60%)
0	1	0	RFU*
0	1	1	Weak (40%)
1	0	0	RFU*
1	0	1	Semi Half (50%)
1	1	0	RFU*
1	1	1	Semi Weak (30%)

* All bits in RFU address fields must be programmed to Zero, all other states are reserved for future usage.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Ambient Temperature	TA	0 ~ 70	°C
Storage Temperature	TSTG	-55 ~ 125	°C
Voltage on Any Pin relative to VSS	VIN, VOUT	-0.5 ~ 3.6	V
Voltage on VDD relative to VSS	VDD	-0.5 ~ 3.6	V
Voltage on VDDQ relative to VSS	VDDQ	-0.5 ~ 3.6	V
Output Short Circuit Current	IOS	50	mA
Power Dissipation	PD	2	W
Soldering Temperature · Time	TSOLDER	260 · 10	°C · sec

Note : Operation at above absolute maximum rating can adversely affect device reliability

DC OPERATING CONDITIONS (TA=0 to 70°C, Voltage referenced to VSS = 0V)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Power Supply Voltage	VDD	2.2	2.5	2.625	V	1, 4
		2.375	2.5	2.625	V	1, 5
		2.55	2.8	2.95	V	1, 6
Power Supply Voltage	VDDQ	2.2	2.5	2.625	V	1, 4
		2.375	2.5	2.625	V	1, 5
		2.55	2.8	2.95	V	1, 6
Input High Voltage	VIH	VREF + 0.15	-	VDDQ + 0.3	V	
Input Low Voltage	VIL	-0.3	-	VREF - 0.15	V	2
Termination Voltage	VTT	VREF - 0.04	VREF	VREF + 0.04	V	
Reference Voltage	VREF	0.49*VDDQ	0.5*VDDQ	0.51*VDDQ	V	3

Note : 1. VDDQ must not exceed the level of VDD.
2. VIL (min) is acceptable -1.5V AC pulse width with ≤ 5ns of duration.
3. VREF is expected to be equal to 0.5*VDDQ of the transmitting device, and to track variations in the DC level of the same. Peak to peak noise on VREF may not exceed ± 2% of the DC value.
4. Supports 300MHz
5. Supports 275/250MHz
6. Supports 400/350MHz

DC CHARACTERISTICS I (TA=0 to 70°C, Voltage referenced to VSS = 0V)

Parameter	Symbol	Min	Max	Unit	Note
Input Leakage Current	ILI	-2	2	uA	1
Output Leakage Current	ILO	-5	5	uA	2
Output High Voltage	VOH	VTT + 0.76	-	V	IOH = -15.2mA
Output Low Voltage	VOL	-	VTT - 0.76	V	IOL = +15.2mA

Note : 1. VIN = 0 to 3.6V, All other pins are not tested under VIN =0V. 2. DOUT is disabled, VOUT=0 to 2.7V

DC CHARACTERISTICS II (TA=0 to 70°C, Voltage referenced to VSS = 0V)

Parameter	Symbol	Test Condition	Speed					Unit	Note
			25	28	33	36	4		
Operating Current	IDD0	One bank; Active - Precharge; tRC=tRC(min); tCK=tCK(min); DQ,DM and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle one chip active, the other chip precarge standby	260	240	220	210	200	mA	1
Operating Current	IDD1	Burst length=4, One bank active tRC ≥ tRC(min), IOL=0mA one chip active, the other chip precarge standby	280	260	240	230	220	mA	1
Precharge Standby Current in Power Down Mode	IDD2P	CKE ≤ VIL(max), tCK=min both chips precharge standby	70	60	50	50	50	mA	
Precharge Standby Current in Non Power Down Mode	IDD2N	CKE ≥ VIH(min), /CS ≥ VIH(min), tCK = min, Input signals are changed one time during 2clks both chips precharge standby	170	150	120	120	120	mA	
Active Standby Current in Power Down Mode	IDD3P	CKE ≤ VIL(max), tCK=min one chip active standby, the other chip precharge standby	100	90	70	70	70	mA	
Active Standby Current in Non Power Down Mode	IDD3N	CKE ≥ VIH(min), /CS ≥ VIH(min), tCK=min, Input signals are changed one time during 2clks one chip active standby, the other chip precharge standby	270	250	200	200	200	mA	
Burst Mode Operating Current	IDD4	tCK ≥ tCK(min), IOL=0mA All banks both chips active	820	740	620	570	570	mA	1
Auto Refresh Current	IDD5	tRC ≥ tRFC(min), All banks active both chips refresh	700	700	600	600	600	mA	1,2
Self Refresh Current	IDD6	CKE ≤ 0.2V both chips refresh	6	6	6	6	6	mA	
Operating Current - Four Bank Operation	IDD7	Four bank interleaving with BL=4, both chips and 4 bank interleaving	1100	950	820	720	720	mA	

Note :

1. IDD1, IDD4 and IDD5 depend on output loading and cycle rates. Specified values are measured with the output open.
2. Min. of tRFC (Auto Refresh Row Cycle Time) is shown at AC CHARACTERISTICS.

AC OPERATING CONDITIONS (TA=0 to 70°C, Voltage referenced to VSS = 0V)

Parameter	Symbol	Min	Max	Unit	Note
Input High (Logic 1) Voltage, DQ, DQS and DM signals	VIH(AC)	VREF + 0.35		V	
Input Low (Logic 0) Voltage, DQ, DQS and DM signals	VIL(AC)		VREF - 0.35	V	
Input Differential Voltage, CK and /CK inputs	VID(AC)	0.7	VDDQ + 0.6	V	1
Input Crossing Point Voltage, CK and /CK inputs	VIX(AC)	0.5*VDDQ-0.2	0.5*VDDQ+0.2	V	2

Note :
1. VID is the magnitude of the difference between the input level on CK and the input on /CK.
2. The value of VIX is expected to equal 0.5*VDDQ of the transmitting device and must track variations in the DC level of the same.

AC OPERATING TEST CONDITIONS (TA=0 to 70°C, Voltage referenced to VSS = 0V)

Parameter	Value	Unit
Reference Voltage	VDDQ x 0.5	V
Termination Voltage	VDDQ x 0.5	V
AC Input High Level Voltage (VIH, min)	VREF + 0.35	V
AC Input Low Level Voltage (VIL, max)	VREF - 0.35	V
Input Timing Measurement Reference Level Voltage	VREF	V
Output Timing Measurement Reference Level Voltage	VTT	V
Input Signal maximum peak swing	1.5	V
Input minimum Signal Slew Rate	1	V/ns
Termination Resistor (RT)	50	Ω
Series Resistor (RS)	25	Ω
Output Load Capacitance for Access Time Measurement (CL)	30	pF

AC CHARACTERISTICS - I (AC operating conditions unless otherwise noted)

Parameter		Symbol	25		28		Unit	Note
			Min	Max	Min	Max		
Row Cycle Time		tRC	18	-	16	-	CK	
Auto Refresh Row Cycle Time		tRFC	21	-	17	-	CK	
Row Active Time		tRAS	12	100K	10	100K	CK	
Row Address to Column Address Delay for Read		tRCDRD	6	-	5	-	CK	
Row Address to Column Address Delay for Write		tRCDWR	3	-	2	-	CK	
Row Active to Row Active Delay		tRRD	4	-	4	-	CK	
Column Address to Column Address Delay		tCCD	1	-	1	-	CK	
Row Precharge Time		tRP	6	-	5	-	CK	
Write Recovery Time		tWR	3	-	3	-	CK	
Last Data-In to Read Command		tDRL	2	-	2	-	CK	
Auto Precharge Write Recovery + Precharge Time		tDAL	9	-	8	-	CK	
System Clock Cycle Time	CL=5	tCK	2.5	6	-	-	ns	
	CL=4		-	-	2.8	6	ns	
Clock High Level Width		tCH	0.45	0.55	0.45	0.55	CK	
Clock Low Level Width		tCL	0.45	0.55	0.45	0.55	CK	
Data-Out edge to Clock edge Skew		tAC	-0.6	0.6	-0.6	0.6	ns	
DQS-Out edge to Clock edge Skew		tDQSCK	-0.6	0.6	-0.6	0.6	ns	
DQS-Out edge to Data-Out edge Skew		tDQSQ	-	0.35	-	0.35	ns	
Data-Out hold time from DQS		tQH	tHPmin -tQHS	-	tHPmin -tQHS	-	ns	1,6
Clock Half Period		tHP	tCH/L min	-	tCH/L min	-	ns	1,5
Data Hold Skew Factor		tQHS	-	0.35	-	0.35	ns	6
Input Setup Time		tIS	0.75	-	0.75	-	ns	2
Input Hold Time		tIH	0.75	-	0.75	-	ns	2
Write DQS High Level Width		tDQSH	0.4	0.6	0.4	0.6	CK	
Write DQS Low Level Width		tDQSL	0.4	0.6	0.4	0.6	CK	
Clock to First Rising edge of DQS-In		tDQSS	0.85	1.15	0.85	1.15	CK	
Data-In Setup Time to DQS-In (DQ & DM)		tDS	0.35	-	0.35	-	ns	3
Data-In Hold Time to DQS-In (DQ & DM)		tDH	0.35	-	0.35	-	ns	3

Parameter	Symbol	25		28		Unit	Note
		Min	Max	Min	Max		
Read DQS Preamble Time	tRPRE	0.9	1.1	0.9	1.1	CK	
Read DQS Postamble Time	tRPST	0.4	0.6	0.4	0.6	CK	
Write DQS Preamble Setup Time	tWPRES	0	-	0	-	ns	
Write DQS Preamble Hold Time	tWPREH	0.35	-	0.35	-	CK	
Write DQS Postamble Time	tWPST	0.4	0.6	0.4	0.6	CK	
Mode Register Set Delay	tMRD	2	-	2	-	CK	
Exit Self Refresh to Any Execute Command	tXSC	200	-	200	-	CK	4
Power Down Exit Time	tPDEX	2tCK + tIS	-	2tCK + tIS	-	CK	
Average Periodic Refresh Interval	tREFI	-	7.8	-	7.8	us	

Note :

1. This calculation accounts for tDQSQ(max), the pulse width distortion of on-chip circuit and jitter.
2. Data sampled at the rising edges of the clock : A0~A11, BA0~BA1, CKE, /CS0, /CS1, /RAS, /CAS, /WE.
3. Data latched at both rising and falling edges of Data Strobes(DQS0~DQS3) : DQ, DM(0~3).
4. Minimum of 200 cycles of stable input clocks after Self Refresh Exit command, where CKE is held high, is required to complete Self Refresh Exit and lock the internal DLL circuit of DDR SDRAM.
5. Min (tCL, tCH) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device (i.e. this value can be greater than the minimum specification limits for tCL and tCH).
6. tHP = minimum half clock period for any given cycle and is defined by clock high or clock low (tCH, tCL). tQHS consists of tDQSQmax, the pulse width distortion of on-chip clock circuits, data pin to pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers.
7. DQS, DM and DQ input slew rate is specified to prevent double clocking of data and preserve setup and hold times. Signal transitions through the DC region must be monotonic.

AC CHARACTERISTICS - I (continue)

Parameter		Symbol	33		36		4		Unit	Note
			Min	Max	Min	Max	Min	Max		
Row Cycle Time		tRC	14	-	14	-	13	-	CK	
Auto Refresh Row Cycle Time		tRFC	17	-	16	-	15	-	CK	
Row Active Time		tRAS	9	100K	9	100K	8	100K	CK	
Row Address to Column Address Delay for Read		tRCDRD	5	-	5	-	5	-	CK	
Row Address to Column Address Delay for Write		tRCDWR	2	-	2	-	2	-	CK	
Row Active to Row Active Delay		tRRD	3	-	3	-	3	-	CK	
Column Address to Column Address Delay		tCCD	1	-	1	-	1	-	CK	
Row Precharge Time		tRP	5	-	5	-	5	-	CK	
Write Recovery Time		tWR	3	-	3	-	3	-	CK	
Last Data-In to Read Command		tDRL	2	-	2	-	2	-	CK	
Auto Precharge Write Recovery + Precharge Time		tDAL	8	-	8	-	8	-	CK	
System Clock Cycle Time	CL=4	tCK	3.3	10	3.6	10	4	10	ns	
	CL=3		4.5	10	4.5	10	4.5	10	ns	
Clock High Level Width		tCH	0.45	0.55	0.45	0.55	0.45	0.55	CK	
Clock Low Level Width		tCL	0.45	0.55	0.45	0.55	0.45	0.55	CK	
Data-Out edge to Clock edge Skew		tAC	-0.6	0.6	-0.6	0.6	-0.6	0.6	ns	
DQS-Out edge to Clock edge Skew		tDQSCK	-0.6	0.6	-0.6	0.6	-0.6	0.6	ns	
DQS-Out edge to Data-Out edge Skew		tDQSQ	-	0.35	-	0.4	-	0.4	ns	
Data-Out hold time from DQS		tQH	tHPmin -tQHS	-	tHPmin -tQHS	-	tHPmin -tQHS	-	ns	1,6
Clock Half Period		tHP	tCH/L min	-	tCH/L min	-	tCH/L min	-	ns	1,5
Data Hold Skew Factor		tQHS	-	0.35	-	0.4	-	0.4	ns	6
Input Setup Time		tIS	0.75	-	0.75	-	0.75	-	ns	2
Input Hold Time		tIH	0.75	-	0.75	-	0.75	-	ns	2
Write DQS High Level Width		tDQSH	0.4	0.6	0.4	0.6	0.4	0.6	CK	
Write DQS Low Level Width		tDQSL	0.4	0.6	0.4	0.6	0.4	0.6	CK	
Clock to First Rising edge of DQS-In		tDQSS	0.85	1.15	0.85	1.15	0.85	1.15	CK	
Data-In Setup Time to DQS-In (DQ & DM)		tDS	0.35	-	0.4	-	0.4	-	ns	3
Data-In Hold Time to DQS-In (DQ & DM)		tDH	0.35	-	0.4	-	0.4	-	ns	3

Parameter	Symbol	33		36		4		Unit	Note
		Min	Max	Min	Max	Min	Max		
Read DQS Preamble Time	tRPRE	0.9	1.1	0.9	1.1	0.9	1.1	CK	
Read DQS Postamble Time	tRPST	0.4	0.6	0.4	0.6	0.4	0.6	CK	
Write DQS Preamble Setup Time	tWPRES	0	-	0	-	0	-	ns	
Write DQS Preamble Hold Time	tWPREH	0.35	-	0.35	-	0.35	-	CK	
Write DQS Postamble Time	tWPST	0.4	0.6	0.4	0.6	0.4	0.6	CK	
Mode Register Set Delay	tMRD	2	-	2	-	2	-	CK	
Exit Self Refresh to Any Execute Command	tXSC	200	-	200	-	200	-	CK	4
Power Down Exit Time	tPDEX	2tCK + tIS	-	1tCK + tIS	-	1tCK + tIS	-	CK	
Average Periodic Refresh Interval	tREFI	-	7.8	-	7.8	-	7.8	us	

Note :

1. This calculation accounts for tDQSQ(max), the pulse width distortion of on-chip circuit and jitter.
2. Data sampled at the rising edges of the clock : A0~A11, BA0~BA1, CKE, /CS0, /CS1, /RAS, /CAS, /WE.
3. Data latched at both rising and falling edges of Data Strobes(DQS0~DQS3) : DQ, DM(0~3).
4. Minimum of 200 cycles of stable input clocks after Self Refresh Exit command, where CKE is held high, is required to complete Self Refresh Exit and lock the internal DLL circuit of DDR SDRAM.
5. Min (tCL, tCH) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device (i.e. this value can be greater than the minimum specification limits for tCL and tCH).
6. tHP = minimum half clock period for any given cycle and is defined by clock high or clock low (tCH, tCL). tQHS consists of tDQSQmax, the pulse width distortion of on-chip clock circuits, data pin to pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers.
7. DQS, DM and DQ input slew rate is specified to prevent double clocking of data and preserve setup and hold times. Signal transitions through the DC region must be monotonic.

AC CHARACTERISTICS - II

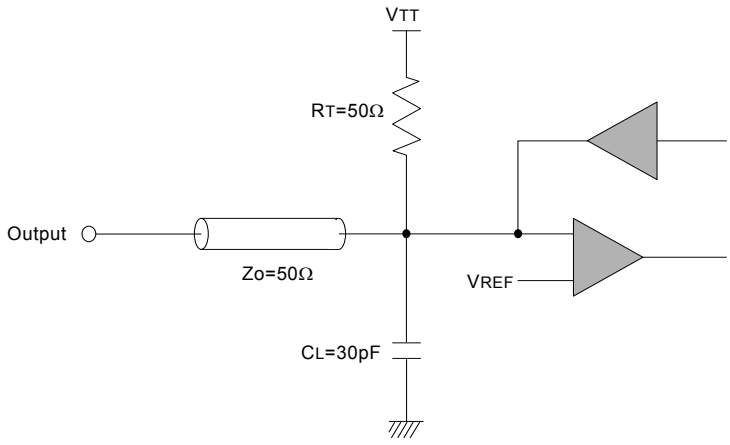
Frequency	CL	tRC	tRFC	tRAS	tRCDRD	tRCDWR	tRP	tDAL	Unit
400MHz (2.5ns)	5	18	21	12	6	3	6	9	tCK
350MHz (2.8ns)	4	16	17	10	5	2	5	8	tCK
300MHz (3.3ns)	4	14	17	9	5	2	5	8	tCK
275MHz (3.6ns)	4	14	16	9	5	2	5	8	tCK
250MHz (4.0ns)	4	13	15	8	5	2	5	8	tCK

CAPACITANCE (T_A=25°C, f=1MHz)

Parameter	Pin	Symbol	Min	Max	Unit
Input Clock Capacitance	CK, /CK	C_{CK}	1.5	5.5	pF
Input Capacitance	All other input-only pins	C_{IN}	1.5	5.5	pF
Input / Output Capacitance	DQ, DQS, DM	C_{IO}	5.5	9.5	pF

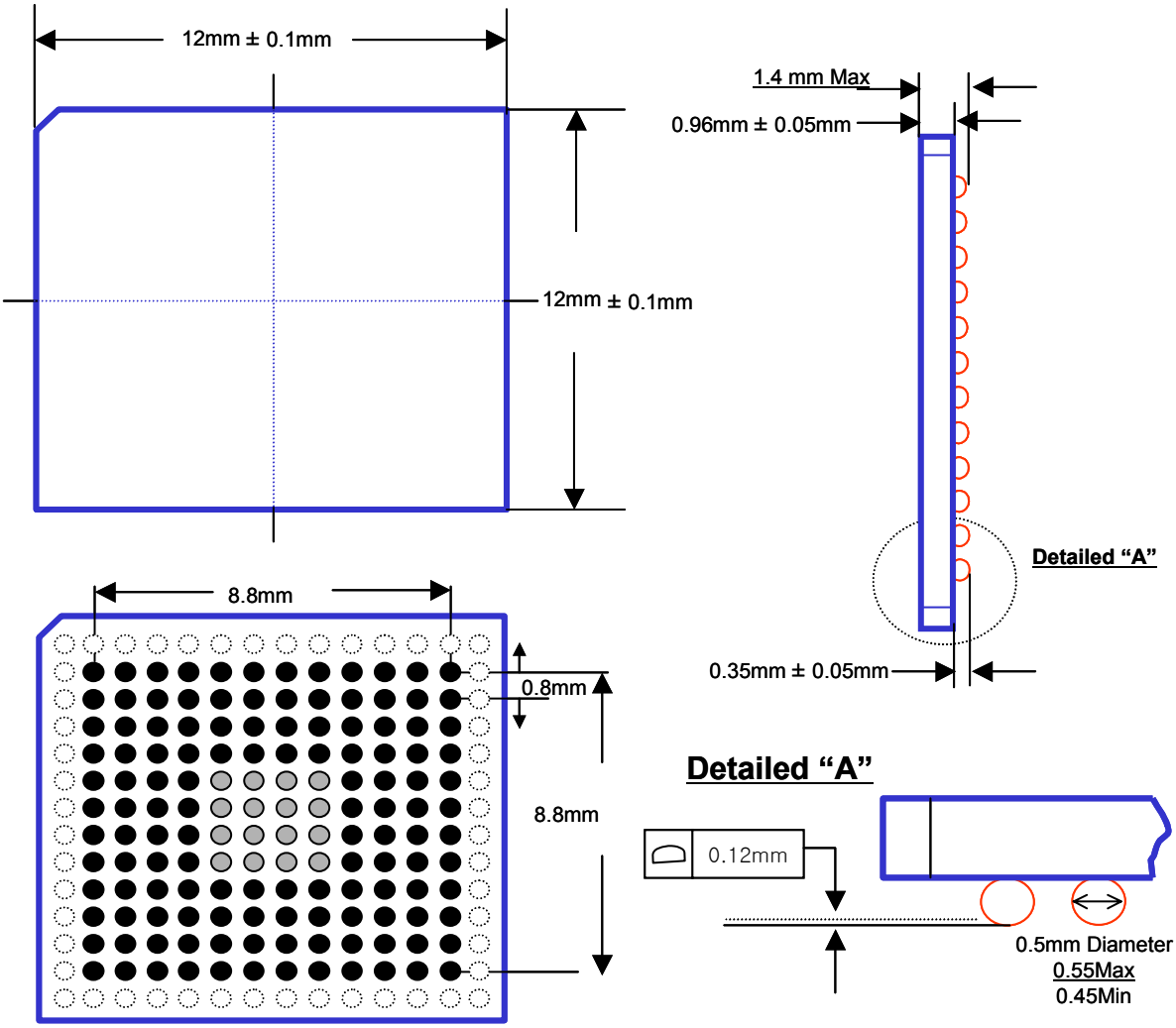
Note :
1. V_{DD} = min. to max., V_{DDQ} = 2.3V to 2.7V, V_{ODC} = V_{DDQ}/2, V_{O}peak-to-peak = 0.2V
2. Pins not under test are tied to GND.
3. These values are guaranteed by design and are tested on a sample basis only.

OUTPUT LOAD CIRCUIT



PACKAGE INFORMATION

12mm x 12mm, 144ball Fine-pitch Ball Grid Array



[Ball Location]

- **Ball existing**
- **Optional (Thermal ball, NC, No ball)**
- **Depopulated ball**

(MO 205-D, AE in JEDEC)

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