Integrated Circuit Systems, Inc.

ICS9147-06

Frequency Generator & Integrated Buffers for PENTIUM™

General Description

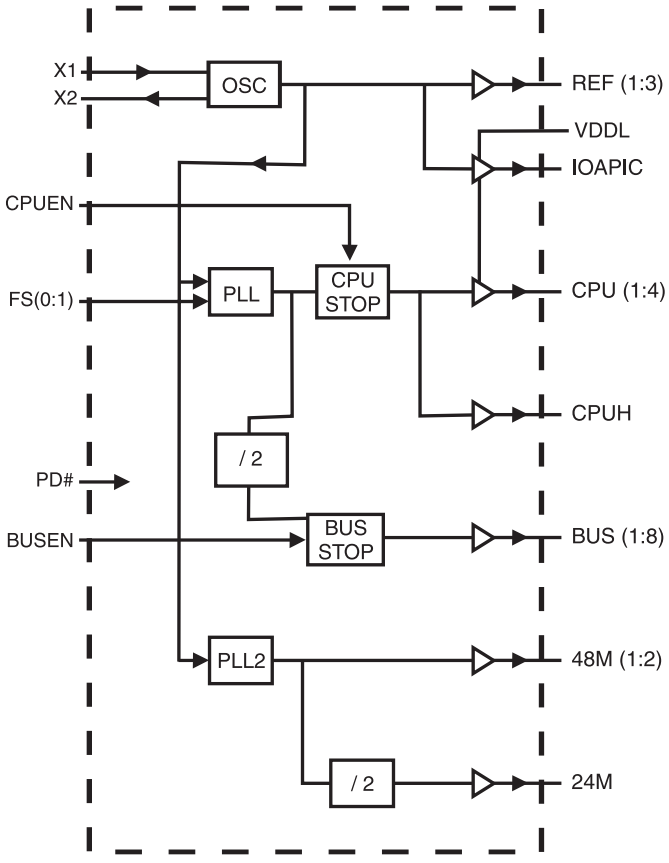
The **ICS9147-06** generates all clocks required for high speed RISC or CISC microprocessor systems such as Intel PentiumPro. Two different reference frequency multiplying factors are externally selectable with smooth frequency transitions. Glitch-free Stop clock control is provided for CPU and BUS clocks. Complete chip low current mode is achieved with the Power Down# pin.

High drive BUS outputs typically provide greater than 1V/ns slew rate into 30 pF loads. CPU outputs typically provide better than 1V/ns slew rate into 20 pF loads while maintaining 50± 5% duty cycle. The REF and IOAPIC clock outputs typically provide better than 0.5V/ns slew rates. Separate buffer supply pins VDDL allow for nominal 3.3V voltage or reduced voltage swing (from 2.9 to 2.5V) for CPU (1:4) and IOAPIC outputs.

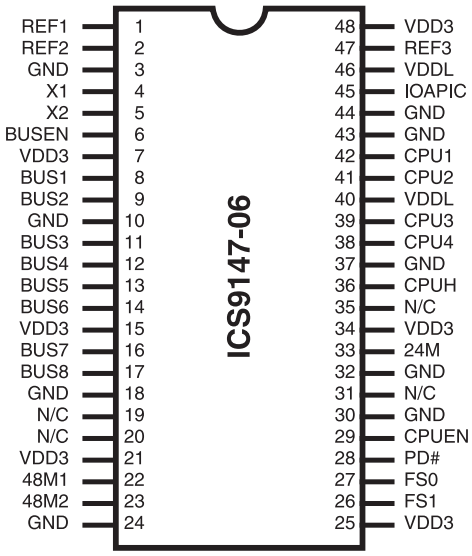
Features

- Generates five processor, eight bus, four 14.31818 MHz, two 48 MHz clocks for USB support and one 24 MHz clock.
- CPU to BUS clock skew 1 to 4ns (CPU early)
- Synchronous clocks skew matched to 250ps window on CPU and 500ps window on BUS.
- Selectable multiplying ratios
- Glitch free stop clock controls CPUEN and BUSEN
- 3.0V – 3.7V supply range, 2.5V to VDD supply range for CPU (1:4) clocks and IOAPIC clock.
- 48-pin SSOP package

Block Diagram



Pin Configuration



48-Pin SSOP

Pentium is a trademark of Intel Corporation

Functionality

PD#	BUSEN	CPUEN	FS1	FS0	CPU (1:4) CPUH	BUS	REF IOAPIC	24 (MHz)	48 (MHz)
1	1	1	0	0	Tristate	Tristate	Tristate	Tristate	Tristate
1	1	1	0	1	60	30	14.31818	24	48
1	1	1	1	0	66.6	33.3	14.31818	24	48
1	1	1	1	1	REF/2	REF/4	REF	REF/4	REF/2
1	1	0	X	X	LOW	Running	14.31818	24	48
1	0	1	X	X	Running	LOW	14.31818	24	48
0	X	X	X	X	LOW	LOW	LOW	LOW	LOW

Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1, 2, 47	REF1, REF2, REF3	OUT	14.318 MHz reference clock outputs.
3, 10, 18, 24, 30, 32, 37, 43, 44	GND	PWR	Ground.
4	X1	IN	Crystal input, has internal crystal load capacitor, and feedback resistor from X2. Nominally 14.31818MHz.
5	X2	OUT	Crystal output, has internal crystal load capacitor
8, 9, 11, 12, 13, 14, 16, 17	BUS (1:8)	OUT	BUS clock outputs, operates synchronously at CPU/2.
26, 27	FS (0:1)	IN	Select pin for enabling CPU and BUS clock frequencies.*
7, 15, 21, 25, 34, 48	VDD3	PWR	Core and Buffer output clock power supply.
22, 23	48M (1:2)	OUT	48 MHz clock output
28	PD#	IN	Device power down input, stops outputs low and shuts off crystal oscillator and PLLs when low.*
29	CPUEN	IN	Output enable for all CPU clocks, a logic low will Stop low all CPU clocks.*
36	CPUH	OUT	3.3 (VDD3 dependent) CPU clock output
38, 39, 41, 42	CPU (1:4)	OUT	CPU clock output clocks, operates at VDDL supply voltage (with IOAPIC), either nominal 3.3V VDD or reduced voltage 2.9 to 2.5V.
6	BUSEN	IN	Output enable for all BUS clock, a logic low will stop Low all Bus clocks.*
45	IOAPIC	OUT	IOAPIC clock output. (14.318 MHz), operates at VDDL supply voltage with CPU (1:4), either nominal 3.3V VDD or reduced voltage 2.9 to 2.5V.
40, 46	VDDL	PWR	Power supply for CPU and IOAPIC block buffers, operates at nominal 3.3V VDD or reduced voltage 2.9 to 2.5V.
33	24M	OUT	24 MHz clock output

* Has internal pull-up to V_{DD3}.

Absolute Maximum Ratings

Supply Voltage ..... 7.0 V

Logic Inputs ..... GND –0.5 V to V_{DD} +0.5 V

Ambient Operating Temperature ..... 0°C to +70°C

Storage Temperature ..... –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics at 3.3V

V_{DDL}=V_{DD3}=3.0 – 3.7 V, T_A = 0 – 70° C unless otherwise stated

DC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}		-	-	0.2VDD	V
Input High Voltage	V_{IH}		0.7V_{DD}	-	-	V
Input Low Current	I_{IL}	VIN=0V	-28.0	-10.5	-	µA
Input High Current	I_{IH}	VIN=VDD	-5.0	-	5.0	µA
Output Low Current	I_{OL1}	VOL=0.8V; for CPUH, BUS & REF1 (and CPU & IOAPIC at VDDL= 3.0 to 3.7V)	-	33.0	-	mA
Output High Current	I_{OH1}	VOH=2.0V; for CPUH, BUS & REF1 (and CPU & IOAPIC at VDDL = 3.0 to 3.7V)	-	-28.0	-	mA
Output Low Current	I_{OL2}	VOL=0.8V; REF (2:3), 24, 48 CLKs	-	26.0	-	mA
Output High Current	I_{OH2}	VOH=2.0V; REF (2:3), 24, 48 CLKs	-	-21.0	-	mA
Output Low Current	I_{OL3}	VOL=0.8V; for CPUL at VDDL = 2.5V	-	26	-	mA
Output High Current	I_{OH3}	VOH = 1.7V; for CPUL at VDDL = 2.5V	-	24	-	mA
Output Low Voltage	V_{OL1}	IOL = 10mA; for CPUH, BUS & REF1 (and CPUL at VDDL = 3.0 to 3.7V)	-	0.22	0.4	V
Output High Voltage	V_{OH1}	IOH = -10mA; for CPUH, BUS & REF (and CPUL at VDDL = 3.0 to 3.7V)	2.4	2.8	-	V
Output Low Voltage	V_{OL2}	IOL = 8mA	-	0.25	0.4	V
Output High Voltage	V_{OH2}	IOH = -8mA	2.4	2.6	-	V
Output Low Voltage	V_{OL3}	IOL = 8 mA; for CPUL at VDDL = 2.5V	-	0.25	0.4	V
Output High Voltage	V_{OH3}	IOH = -8mA; for CPUL at VDDL = 2.5V	2.1	2.25	-	V
Supply Current	I_{DD}	@66.6 MHz; all outputs unloaded	-	70	140	mA
Supply Current	I_{DD}	PD#		230	500	µA

Note 1: Parameter is guaranteed by design and characterization. Not 100% tested in production.

Electrical Characteristics at 3.3V

V_{DDL}=V_{DD3}=3.0 – 3.7 V, T_A = 0 – 70° C unless otherwise stated

AC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Rise Time[1]	T_{r1}	20pF load, 0.8 to 2.0V CPU, BUS & REF1	-	0.9	1.5	ns
Fall Time[1]	T_{f1}	20pF load, 2.0 to 0.8V CPU, BUS & REF1	-	0.8	1.4	ns
Rise Time[1]	T_{r2}	20pF load, 20% to 80% CPU, BUS & REF1	-	1.5	2.5	ns
Fall Time[1]	T_{f2}	20pF load, 80% to 20% CPU, BUS & REF1	-	1.4	2.4	ns
Rise Time[1]	T_{r1}	30pF load, 0.8 to 2.0V CPU, BUS & REF1	-	0.9	1.5	ns
Fall Time[1]	T_{f1}	30pF load, 2.0 to 0.8V CPU, BUS & REF1	-	0.8	1.4	ns
Rise Time[1]	T_{r2}	30pF load, 20% to 80% CPU, BUS & REF1	-	1.5	2.5	ns
Fall Time[1]	T_{f2}	30pF load, 80% to 20% CPU, BUS & REF1	-	1.4	2.4	ns
Rise Time[1]	T_{r3}	20pF load, 0.8 to 2.0V 24 & 48 clocks & REF (2:3)	-	-	-	ns
Fall Time[1]	T_{f3}	20pF load, 2.0 to 0.8V 24 & 48 clocks & REF (2:3)	-	-		ns
Rise Time[1]	T_{r4}	20pF load, 0.4 to 2.0V , CPU with VDDL = 2.5V and IOAPIC	-	-	1.6	ns
Fall Time[1]	T_{f4}	20pF load, 2.0 to 0.4V, CPU with VDDL = 2.5V and IOAPIC	-	-	1.6	ns
Duty Cycle[1]	D_{t1}	20pF load @ VOUT=1.4V	45	50	55	%
Duty Cycle	D_{t2}	REF (1:3)	40	45	50	%
Jitter, One Sigma[1]	T_{jis1}	CPU & Fixed BUS Load=20pF, BUS; Load = 30pF	-	50	150	ps
Jitter, Absolute[1]	T_{jab1}	CPU & Fixed BUS Load=20pF, BUS; Load = 30pF	-250	-	250	ps
Jitter, One Sigma[1]	T_{jis2}	REF1; Load = 47pF	-	55	250	ps
Jitter, Absolute[1]	T_{jab2}	REF1; Load = 47pF	-500	200	500	ps
Input Frequency[1]	F_i		12.0	14.318	16.0	MHz
Logic Input Capacitance[1]	C_{IN}	Logic input pins	-	5	-	pF
Oscillator Input Capacitance[1]	C_{INX}	X1, X2 pins	-	18	-	pF
Power-on Time[1]	ton	From VDD=3.0V to 1st crossing of 66.6 MHz VDD supply ramp < 1 ms	-	1.5	3.0	ms
Clock Skew[1]	T_{sk1}	CPU to CPU; Load=20pF; @1.4V (Same VDD)	-	150	250	ps
Clock Skew[1]	T_{sk2}	BUS to BUS; Load=20pF; @1.4V	-	300	500	ps
Clock Skew[1]	T_{sk3}	CPU to BUS; Load=20pF; @1.4V (CPU is early) (All at 3.3V)	1	3.3	4	ns
Clock Skew[1]	T_{sk4}	CPU @ 2.5 to CPUH @ 3.3V				
	T_{sk5}	CPU @ 2.5V to BUS @ 3.3V				
	T_{sk6}	REF @ 3.3V to IOAPIC @ 2.5V				

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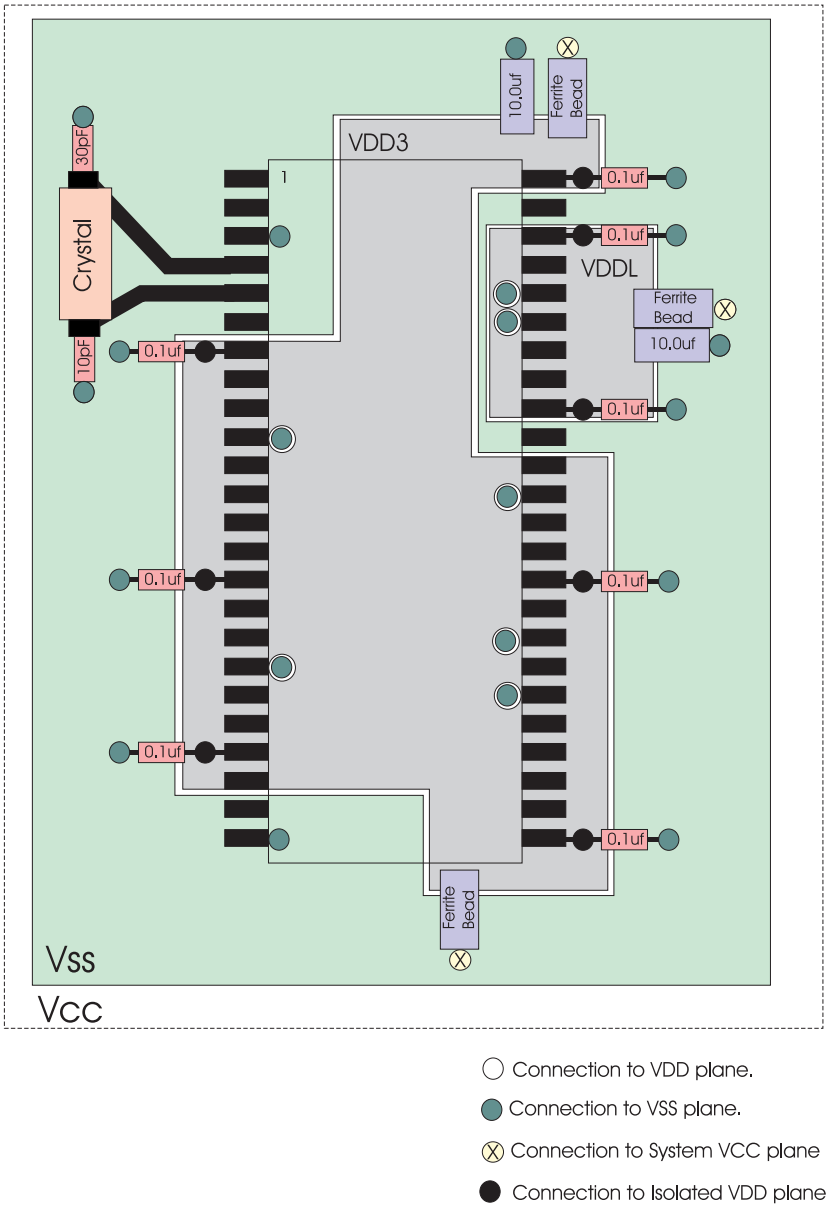
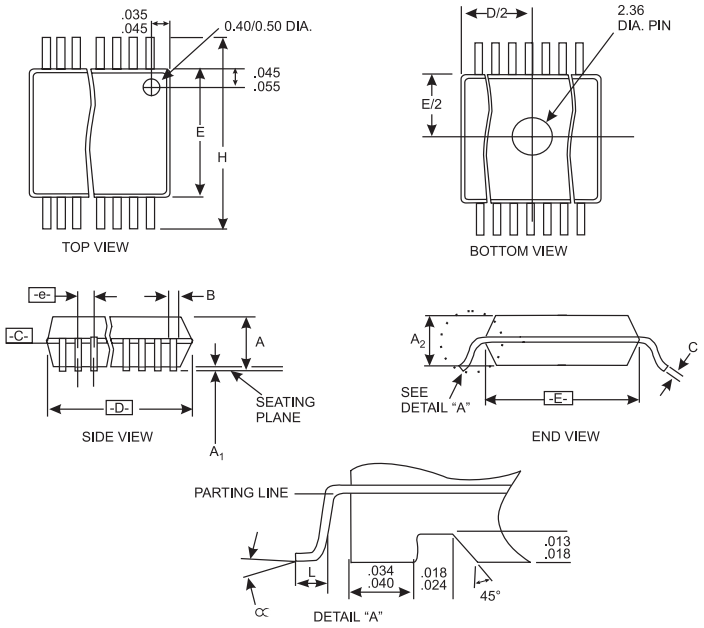
Recommended PCB Layout for ICS9147-06



NOTE:
This PCB Layout is based on a 4 layer board with an internal Ground (common) and Vcc plane. Placement of components will depend on routing of signal trace. The 0.1uf Capacitors should be placed as close as possible to the Power pins. Placement on the backside of the board is also possible. The Ferrite Beads can be replaced with 10-15ohm Resistors. For best results, use a Fixed Voltage Regulator between the main (board) Vcc and the different Vdd planes.



SSOP Package

SYMBOL	COMMON DIMENSIONS			VARIATIONS	D			N
	MIN.	NOM.	MAX.		MIN.	NOM.	MAX.	
A	.095	.101	.110	AC	.620	.625	.630	48
A1	.008	.012	.016					
A2	.088	.090	.092					
B	.008	.010	.0135					
C	.005	-	.010					
D	See Variations							
E	.292	.296	.299					
e	0.025 BSC							
H	.400	.406	.410					
h	.010	.013	.016					
L	.024	.032	.040					
N	See Variations							
∝	0°	5°	8°					
X	.085	.093	.100					

Ordering Information

ICS9147F-06

Example:

ICS XXXX F - PPP

- **Pattern Number (2 or 3 digit number for parts with ROM code patterns)**
- **Package Type**
  F=SSOP
- **Device Type (consists of 3 or 4 digit numbers)**
- **Prefix**
  ICS = Standard Device

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