



Frequency Generator and Buffers for Mobile Pentium™ Systems

General Description

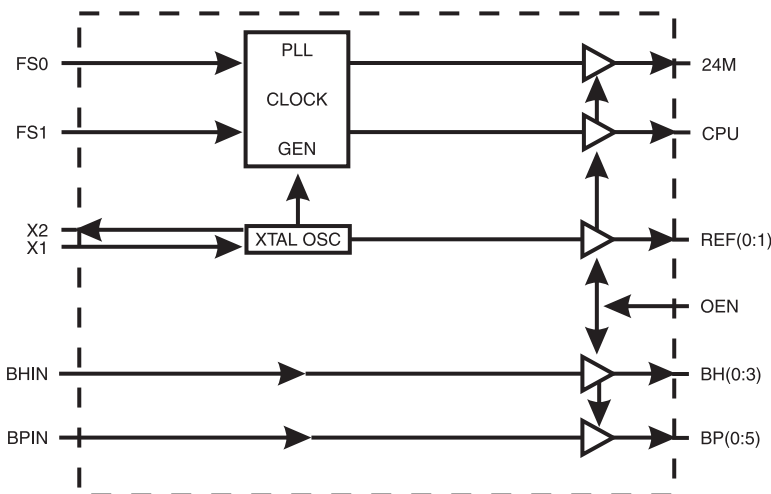
The ICS9159-12 generates all clocks required for mobile microprocessor systems based on Pentium/Mobile Triton chip sets. Three different reference frequency multiplying factors are externally selectable with smooth frequency transitions. These multiplying factors can be customized for specific applications. A test mode is provided to drive all clocks directly.

High drive BCLK outputs provide greater than 1V/ns slew rate into 30pF loads. PCLK outputs provide better than 1V/ns slew rate into 20pF loads while maintaining ±5% duty cycle.

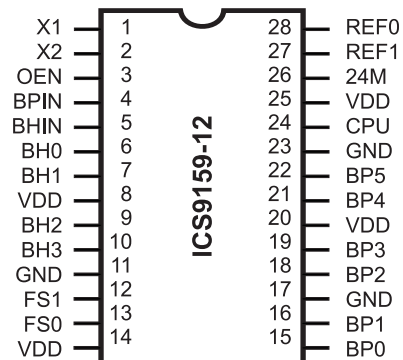
Features

- Generates 14 clocks including processor, disk and reference
- Meets all Pentium/Mobile Triton 82430MX requirements
- Independent buffers provide 4 and 6 clock copies
- Buffered clocks skew matched to ±250ps
- Buffer inputs are 5V tolerant
- Test clock mode eases system design
- Selectable multiplying and processor/bus ratios
- Custom configurations available
- 3.0V- 5.5V supply range
- 28pin, .209" SSOP package

Block Diagram



Pin Configuration



28-Pin SSOP

Functionality

FS1	FS0	*VCO	X1, REF (MHz)	CPU (MHz)
0	0	118/17*X1	14.318	50 (49.69)
0	1	65/7*X1	14.318	66.6 (66.47)
1	0	92/11*X1	14.318	60 (59.87)
1	1	Test mode	TCLK	TCLK/2

*VCO range is limited form 60 - 200 MHz.

CPU	24M
VCO/2	24 MHz
TCLK/2	TCLK/4

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Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
8, 25	VDD	PWR	Power for logic, CPU and fixed frequency output buffers.
1	X1	IN	XTAL or external reference frequency input. This input includes XTAL load capacitance and feedback bias for a 10 - 30 MHz XTAL.
2	X2	OUT	XTAL output which includes XTAL load capacitance.
3	OEN	IN	OEN tristates all outputs when low. This input has an internal pull-up device.
4	BPIN	IN	Input to BPIN(0:5) buffers.
5	BHIN	IN	Input to BHIN(0:3) buffers.
11, 23	GND	PWR	Ground for logic, CPU and fixed frequency output buffers.
6, 7, 9, 10	BH(0:3)	OUT	Buffered copies of the BHIN input, typically used to drive the PCI device clock inputs at one half the CPU frequency.
13, 12	FS(0:1)	IN	Frequency multiplier select pins. See table below. These inputs have internal pull-up devices.
14, 20	VDD	PWR	Power for BCLK output buffers.
15, 16, 18 19, 21, 22	BP(0:5)	OUT	Buffered copies of the BPIN input, typically used to drive the host device clock inputs at the CPU frequency. 17 VSS PWR Ground for BCLK output buffers.
24	CPU	OUT	The CPU output, which is a multiple of the input reference frequency as shown in the table above. Duty cycle is 50/50±5% with a maximum frequency of 100 MHz.
26	24M	OUT	The 24M clock is fixed at 24 MHz.
28, 27	REF(0:1)	OUT	REF is a buffered copy of the crystal oscillator or reference input clock, nominally 14.31818 MHz.

Note: BCLK buffers cannot be supplied with 5 volts (Pins 14 and 20) if CPU and fixed frequencies (Pins 1, 8 and 26) are being supplied with 3 volts.



Absolute Maximum Ratings

Supply Voltage 7.0 V
 Logic Inputs GND -0.5 V to $V_{DD} + 0.5$ V
 Ambient Operating Temperature 0°C to +70°C
 Storage Temperature -65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics at 3.3V

$V_{DD} = 3.0 - 3.7$ V

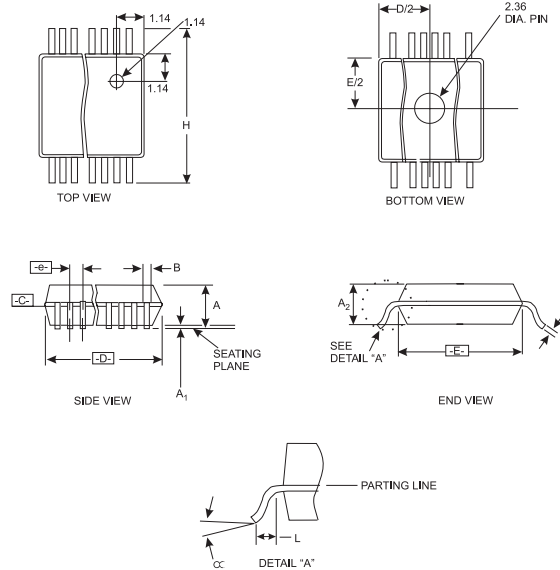
DC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}		-	-	$0.2V_{DD}$	V
Input High Voltage	V_{IH}		$0.7V_{DD}$	-	-	V
Input Low Current	I_{IL}	$V_{IN}=0V$	-	10.5	28.0	μA
Input High Current	I_{IH}	$V_{IN}=V_{DD}$	-5.0	-	5.0	μA
Output Low Current	I_{OL}	$V_{OL}=0.8V$; for PCLKS & BCLKS	30.0	47.0	-	mA
Output High Current	I_{OH}	$V_{OL}=2.0V$; for PCLKS & BCLKS	-	-66.0	-42.0	mA
Output Low Current	I_{OL}	$V_{OL}=0.8V$; for fixed CLKs	25.0	38.0	-	mA
Output High Current	I_{OH}	$V_{OL}=2.0V$; for fixed CLKs	-	-47.0	-30.0	mA
Output Low Voltage	V_{OL}	$I_{OL}=15mA$; for PCLKS & BCLKS	-	0.3	0.4	V
Output High Voltage	V_{OH}	$I_{OH}=-30mA$; for PCLKS & BCLKS	2.4	2.8	-	V
Output Low Voltage	V_{OL}	$I_{OL}=12.5mA$; for fixed CLKs	-	0.3	0.4	V
Output High Voltage	V_{OH}	$I_{OH}=-20mA$; for fixed CLKs	2.4	2.8	-	V
Supply Current	I_{CC}	@66.66 MHz; all outputs unloaded	-	55	110	mA



Electrical Characteristics at 3.3V

$V_{DD} = 3.0 - 3.7 V$

AC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Rise Time 0.8 to 2.0V	T_r	20pF load	-	1.5	3	ns
Fall Time 2.0 to 0.8V	T_f	20pF load	-	0.9	2	ns
Rise Time 20% to 80%	T_r	20pF load	-	2	4.5	ns
Fall Time 80% to 20%	T_f	20pF load	-	1.8	4.25	ns
Duty Cycle [CPU]	D_t	20pF load	45	50	55	%
Duty Cycle, [REF(0:1)]	D_t	20pF load	40	-	60	%
Jitter, One Sigma	T_{j1s}	CPU Clock; Load=20pF, FOUT>25 MHz	-	50	150	ps
Jitter, Absolute	T_{jab}	CPU Clock; Load=20pF, FOUT>25 MHz	-250	-	250	ps
Jitter, One Sigma	T_{j1s}	Fixed CLK; Load=20pF; Comp. to the period	-	1	3	%
Jitter, Absolute	T_{jab}	Fixed CLK; Load=20pF; Comp. to the period	-	2	5	%
Input Frequency	F_i		-	14.318	-	MHz
Clock Skew Window	T_{sk}	BH to BH; Load=20pF; @1.4V	-	50	250	ps
Clock Skew Window	T_{sk}	BP to BP; Load=20pF; @1.4V	-	50	250	ps
Clock Skew Window	T_{sk}	BH to BP; Load=20pF; @1.4V	-	100	500	ps



SYMBOL	COMMON DIMENSIONS			VARIATIONS	D		
	MIN.	NOM.	MAX.		MIN.	NOM.	MAX.
A	0.068	0.073	0.078	14	0.239	0.244	0.249
A1	0.002	0.005	0.008	16	0.239	0.244	0.249
A2	0.066	0.068	0.070	20	0.278	0.284	0.289
B	0.010	0.012	0.015	24	0.318	0.323	0.328
C	0.005	0.006	0.008	28	0.397	0.402	0.407
D	See Variations			30	0.397	0.402	0.407
E	0.205	0.209	0.212	34	0.701	0.706	0.711
e	0.0256 BSC			36	0.602	0.607	0.612
H	0.301	0.307	0.311	44	0.701	0.706	0.711
L	0.022	0.030	0.037	48	0.620	0.625	0.630
N	See Variations			56	0.720	0.725	0.730
∞	0°	4°	8°				

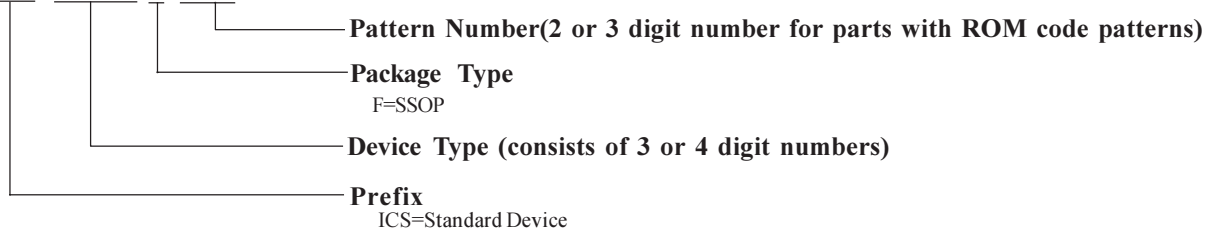
SSOP Package

Ordering Information

ICS9159F-12

Example:

ICS XXXX F-PPP





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