

### 50A, 50V, 0.022 Ohm, N-Channel Power MOSFETs

These are N-Channel power MOSFET'S manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits, gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers and emitter switches for bipolar transistors.

Formerly developmental type TA09772.

### Ordering Information

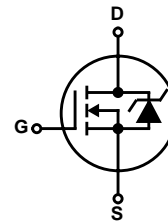
PART NUMBER	PACKAGE	BRAND
RFG50N05	TO-247	RFG50N05
RFP50N05	TO-220AB	RFP50N05

NOTE: When ordering, include the entire part number.

### Features

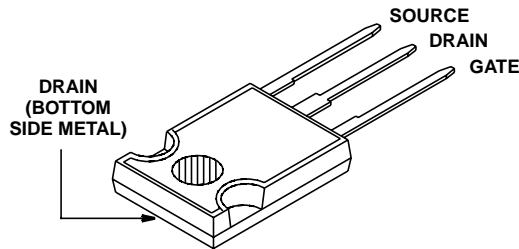
- 50A, 50V
- $r_{DS(ON)} = 0.022\Omega$
- UIS Rating Curve (Single Pulse)
- 175°C Operating Temperature

### Symbol

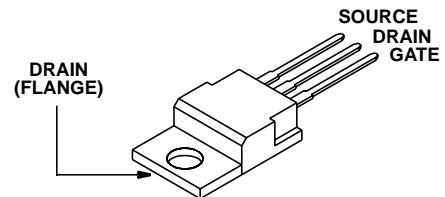


### Packaging

JEDEC STYLE TO-247



JEDEC TO-220AB



## RFG50N05, RFP50N05

### Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ , Unless Otherwise Specified

	RFG50N05, RFP50N05	UNITS
Drain to Source Voltage (Note 1) . . . . .	$V_{DSS}$	50 V
Drain to Gate Voltage ( $R_{GS} = 20k\Omega$ ) (Note 1) . . . . .	$V_{DGR}$	50 V
Continuous Drain Current . . . . .	$I_D$	50 A
Pulsed Drain Current (Note 3) . . . . .	$I_{DM}$	120 A
Gate to Source Voltage . . . . .	$V_{GS}$	$\pm 20$ V
Maximum Power Dissipation . . . . .	$P_D$	132 W
Linear Derating Factor . . . . .		0.88 W/ $^\circ\text{C}$
Single Pulse Avalanche Energy Rating . . . . .	$E_{as}$	Refer to UIS SOA Curve
Operating and Storage Junction Temperature Range . . . . .	$T_J, T_{STG}$	$-55$ to $175$ $^\circ\text{C}$
Maximum Temperature for Soldering		
Leads at 0.063in (1.6mm) from Case for 10s. . . . .	$T_L$	300 $^\circ\text{C}$
Package Body for 10s, See Techbrief 334 . . . . .	$T_{pkg}$	260 $^\circ\text{C}$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

- $T_J = 25^\circ\text{C}$  to  $150^\circ\text{C}$ .

### Electrical Specifications $T_C = 25^\circ\text{C}$ , Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	$BV_{DSS}$	$I_D = 0.250\mu\text{A}, V_{GS} = 0\text{V}$ (Figure 9)	50	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS} = V_{GS}, I_D = 0.250\mu\text{A}$ (Figure 8)	2.0	-	4.0	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = \text{Rated } BV_{DSS}, V_{GS} = 0\text{V}$	-	-	1	A
Zero Gate Voltage Drain Current,		$V_{DS} = 0.8 \times \text{Rated } BV_{DSS}, V_{GS} = 0\text{V}, T_J = 150^\circ\text{C}$	-	-	25	$\mu\text{A}$
Gate to Source Leakage Current	$I_{GSS}$	$V_{GS} = \pm 20\text{V}$	-	-	$\pm 100$	nA
Drain to Source On Resistance (Note 2)	$r_{DS(ON)}$	$I_D = 50\text{A}, V_{GS} = 10\text{V}$ (Figure 7)	-	-	0.022	$\Omega$
Turn-On Time	$t_{(ON)}$	$V_{DD} = 25\text{V}, I_D \approx 25\text{A}, R_L = 1.0\Omega,$ $R_{GS} = 6.67\Omega, V_{GS} = 10\text{V}$ (Figure 11)	-	-	100	ns
Turn-On Delay Time	$t_{d(ON)}$		-	15	-	ns
Rise Time	$t_r$		-	55	-	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	60	-	ns
Fall Time	$t_f$		-	15	-	ns
Turn-Off Time	$t_{(OFF)}$		-	-	100	ns
Total Gate Charge	$Q_{g(tot)}$	$V_{GS} = 0-20\text{V}$	-	-	160	nC
Gate Charge at 10V	$Q_{g(10)}$	$V_{GS} = 0-10\text{V}$				
Threshold Gate Charge	$Q_{g(th)}$	$V_{GS} = 0-2\text{V}$				
Thermal Resistance Junction to Case	$R_{\theta JC}$		-	-	1.14	$^\circ\text{C}/\text{W}$
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	TO-220	-	-	62	$^\circ\text{C}/\text{W}$
		TO-247			30	$^\circ\text{C}/\text{W}$

### Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage (Note 2)	$V_{SD}$	$I_{SD} = 50\text{A}$	-		1.5	V
Diode Reverse Recovery Time	$t_{rr}$	$I_{SD} = 50\text{A}, dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-		125	ns

NOTES:

- Pulsed test: pulse width  $\leq 300\mu\text{s}$  duty cycle  $\leq 2\%$ .
- Repetitive rating: pulse width is limited by maximum junction temperature.

Typical Performance Curves Unless Otherwise Specified

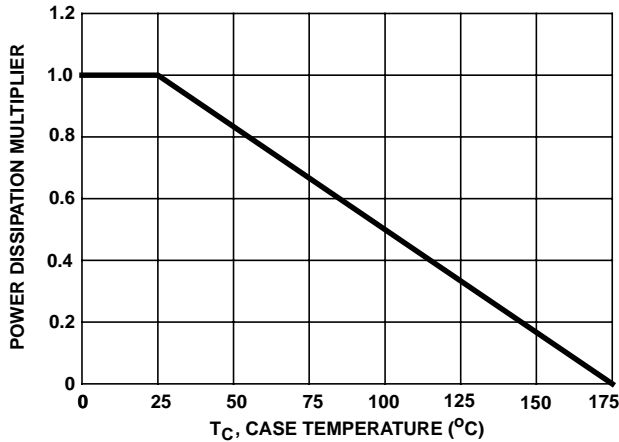


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

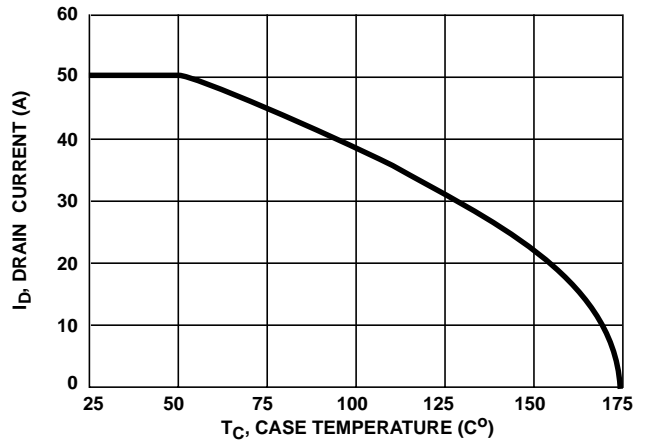


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

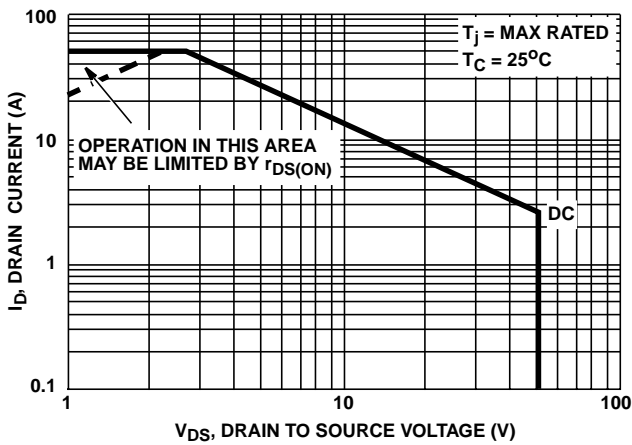


FIGURE 3. FORWARD BIAS SAFE OPERATING AREA

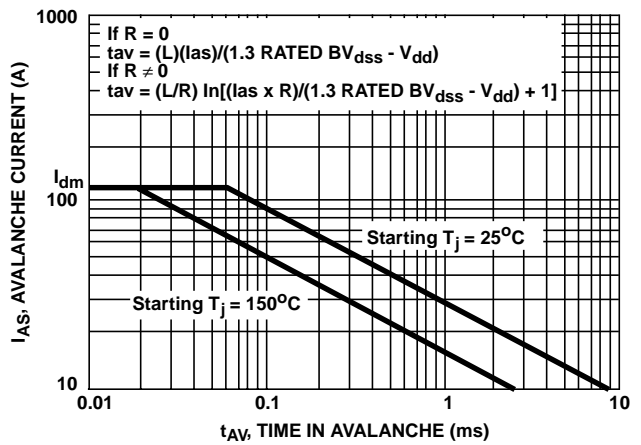


FIGURE 4. UNCLAMPED INDUCTIVE SWITCHING

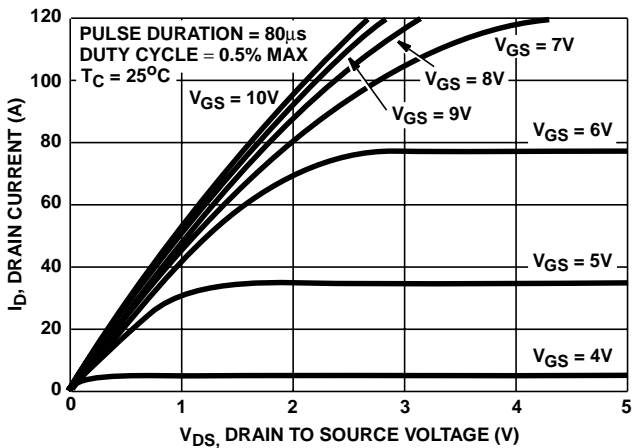


FIGURE 5. SATURATION CHARACTERISTICS

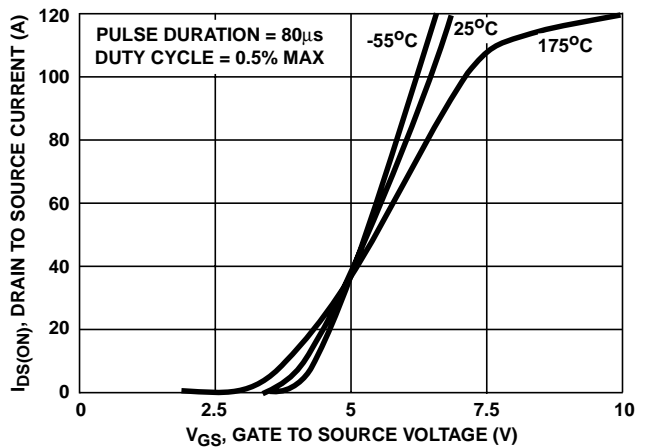


FIGURE 6. TRANSFER CHARACTERISTICS

Typical Performance Curves Unless Otherwise Specified (Continued)

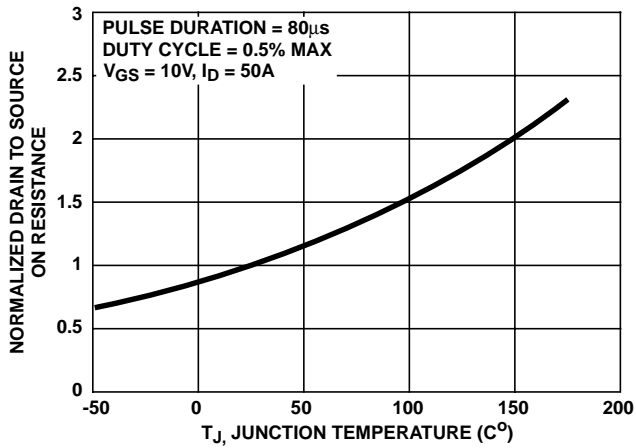


FIGURE 7. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

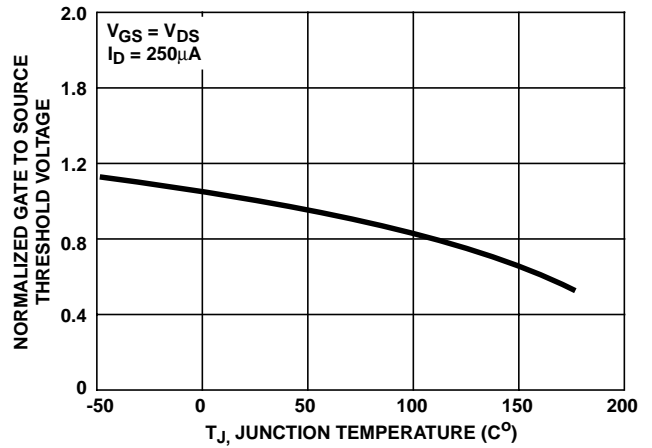


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

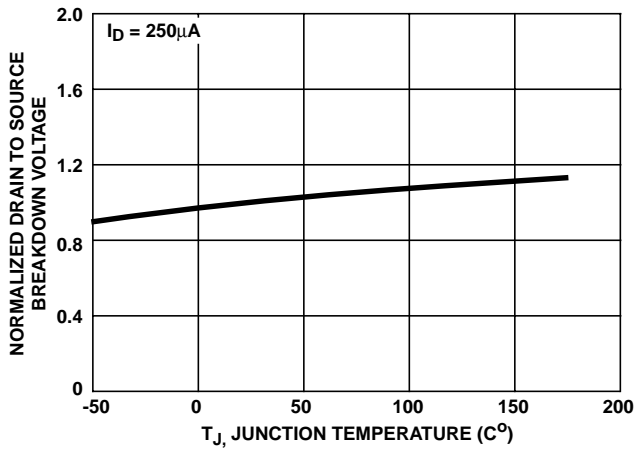


FIGURE 9. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs. JUNCTION TEMPERATURE

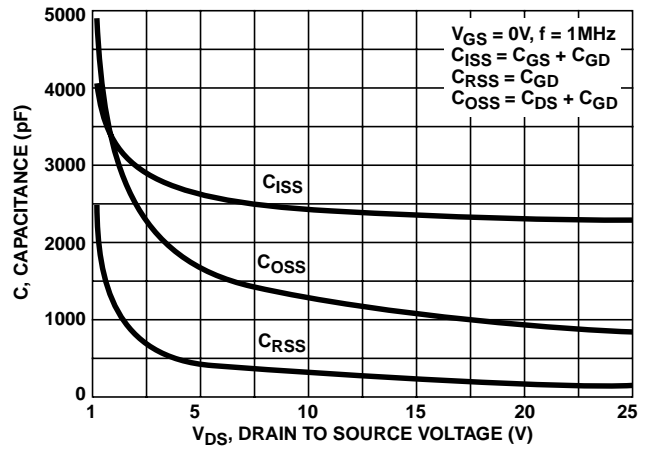
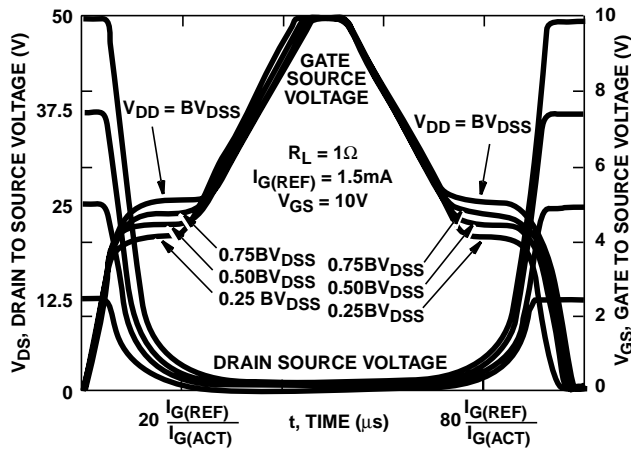


FIGURE 10. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Intersil Application Notes AN7254 and AN7260

FIGURE 11. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

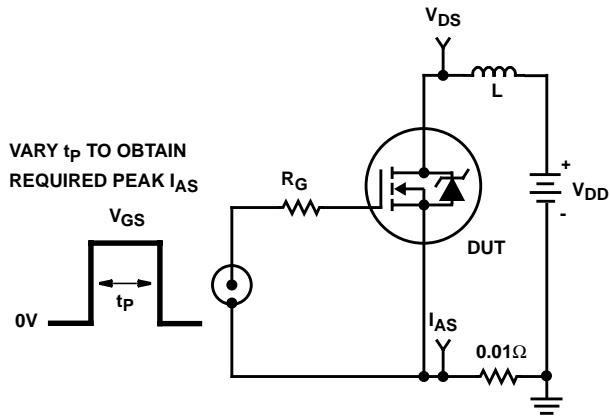


FIGURE 12. UNCLAMPED ENERGY TEST CIRCUIT

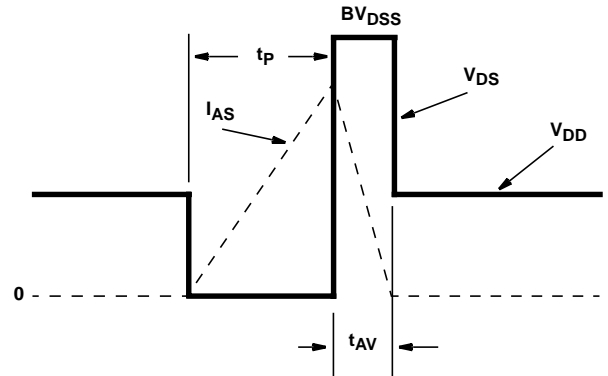


FIGURE 13. UNCLAMPED ENERGY WAVEFORMS

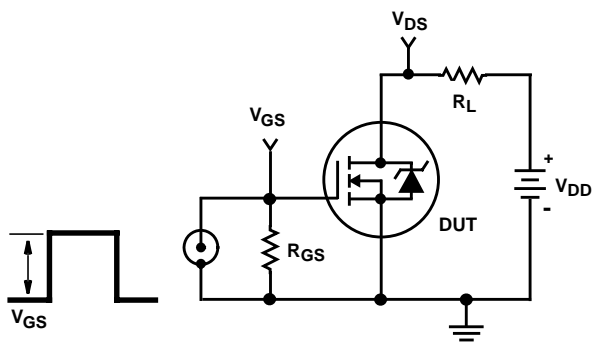


FIGURE 14. SWITCHING TIME TEST CIRCUIT

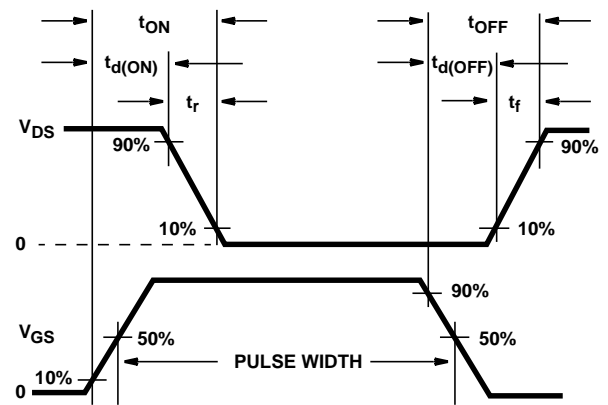


FIGURE 15. RESISTIVE SWITCHING WAVEFORMS

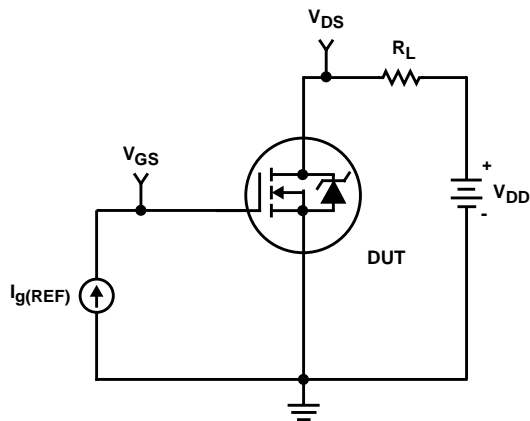


FIGURE 16. GATE CHARGE TEST CIRCUIT

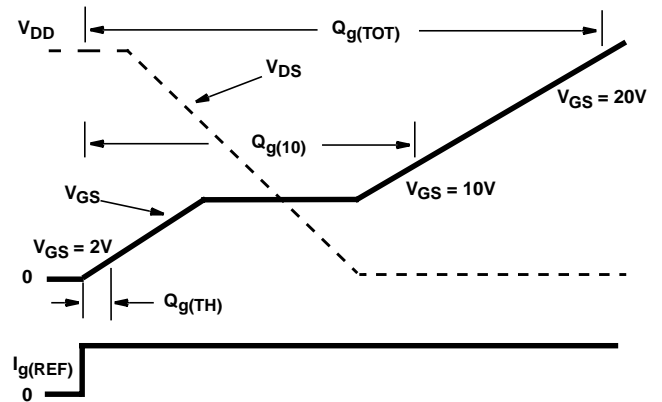


FIGURE 17. GATE CHARGE WAVEFORMS

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