

Description

The IDT70914 is a high-speed 4K x 9 bit synchronous Dual-Port RAM. The memory array is based on Dual-Port memory cells to allow simultaneous access from both ports. Registers on control, data, and address inputs provide low set-up and hold times. The timing latitude provided by this approach allow systems to be designed with very short cycle times. With an input data register, this device has been optimized for applications having unidirectional data flow or bi-directional data flow in bursts.

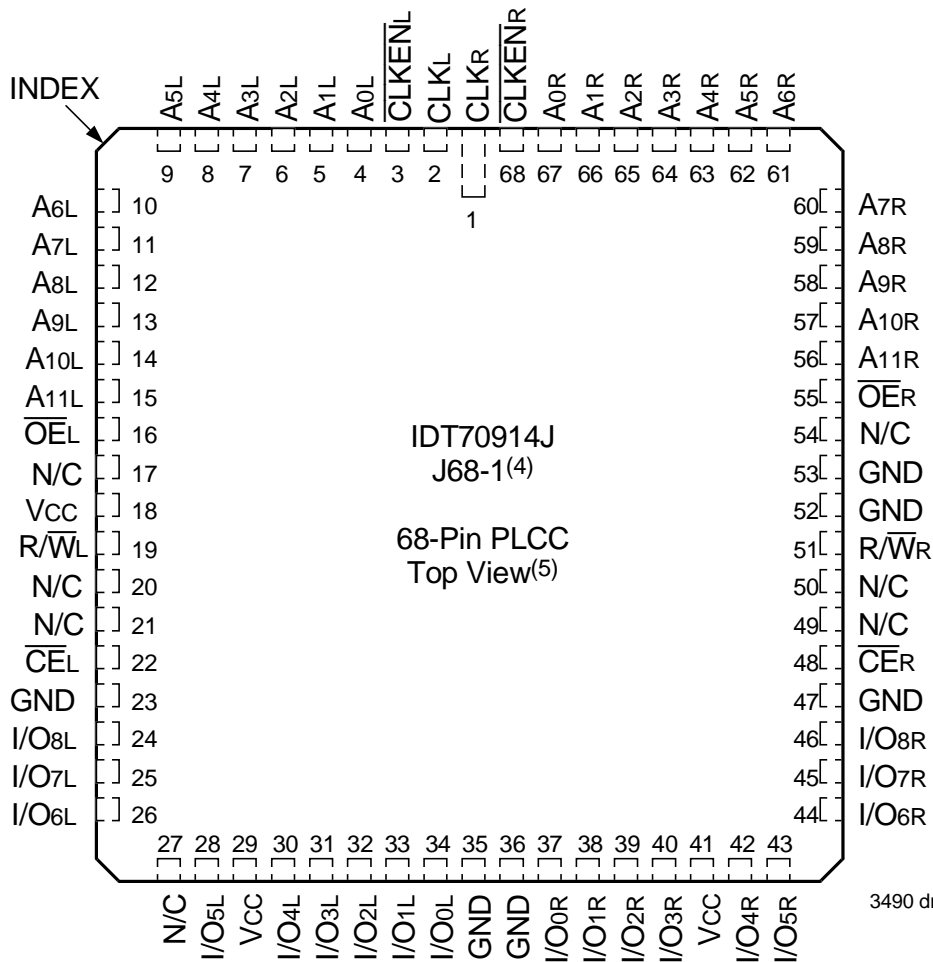
The IDT70914 utilizes a 9-bit wide data path to allow for parity at the user's option. This feature is especially useful in data communication applications where it is necessary to use a parity bit for transmission/

reception error checking.

Fabricated using IDT's CMOS high-performance technology, these Dual-Ports typically operate on only 850mW of power at maximum high-speed clock-to-data output times as fast as 12ns. An automatic power down feature, controlled by \overline{CE} , permits the on-chip circuitry of each port to enter a very low standby power mode.

The IDT70914 is packaged in a 68-pin PLCC, and an 80-pin TQFP. Military grade product is manufactured in compliance with the latest revision of MIL-PRF-38535 QML, making it ideally suited for military temperature applications demanding the highest level of performance and reliability.

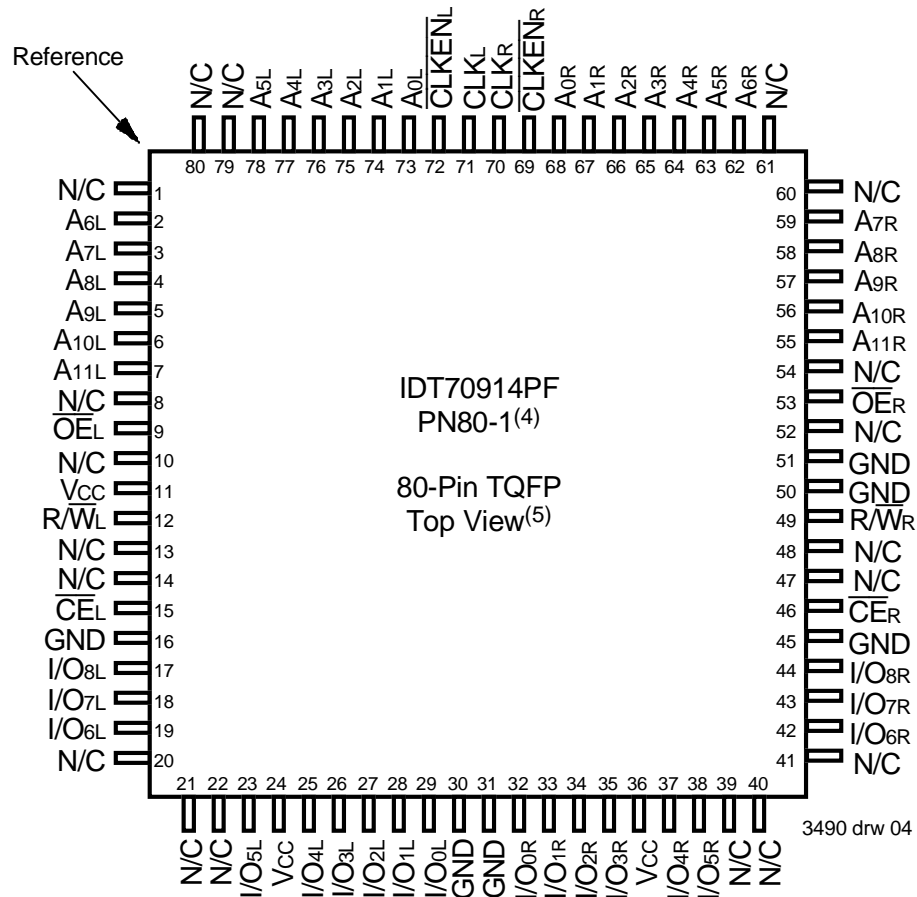
Pin Configurations^(1,2,3)



NOTES:

1. All Vcc pins must be connected to power supply.
2. All ground pins must be connected to ground supply.
3. J68-1 package body is approximately .95 in x .95 in x .17 in.
4. This package code is used to reference the package diagram.
5. This text does not indicate orientation of the actual part-marking.

Pin Configuration^(1,2,3) (con't.)



NOTES:

1. All V_{CC} pins must be connected to power supply.
2. All ground pins must be connected to ground supply.
3. PN80-1 package body is approximately 14mm x 14mm x 1.4mm.
4. This package code is used to reference the package diagram.
5. This text does not indicate orientation of the actual part-marking.

Absolute Maximum Ratings⁽¹⁾

Symbol	Rating	Commercial & Industrial	Military	Unit
$V_{TERM}^{(2)}$	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
$V_{TERM}^{(2)}$	Terminal Voltage	-0.5 to V_{CC}	-0.5 to V_{CC}	V
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-65 to +150	-65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

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NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{TERM} must not exceed $V_{CC} + 10\%$ for more than 25% of the cycle time or 10ns maximum, and is limited to $\leq 20mA$ for the period of $V_{TERM} \geq V_{CC} + 10\%$.

Capacitance**($T_A = +25^\circ C$, $f = 1.0MHz$) TQFP Only**

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	$V_{IN} = 3dV$	8	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 3dV$	9	pF

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NOTES:

- These parameters are determined by device characterization, but are not production tested.
- 3dV references the interpolated capacitance when the input and output switch from 0V to 3V or from 3V to 0V.

Maximum Operating Temperature and Supply Voltage^(1,2)

Grade	Ambient Temperature	GND	V_{CC}
Military	-55°C to +125°C	0V	$5.0V \pm 10\%$
Commercial	0°C to +70°C	0V	$5.0V \pm 10\%$
Industrial	-40°C to +85°C	0V	$5.0V \pm 10\%$

3490 tbl 02

NOTES:

- This is the parameter T_A . This is the "instant on" case temperature.
- Industrial temperature: for specific speeds, packages and powers contact your

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	$6.0^{(2)}$	V
V_{IL}	Input Low Voltage	$-0.5^{(1)}$	—	0.8	V

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NOTES:

- $V_{IL} \geq -1.5V$ for pulse width less than 10ns.
- V_{TERM} must not exceed $V_{CC} + 10\%$.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range ($V_{CC} = 5.0V \pm 10\%$)

Symbol	Parameter	Test Conditions	70914S		Unit
			Min.	Max.	
$ I_{LI} $	Input Leakage Current ⁽¹⁾	$V_{CC} = 5.5V, V_{IN} = 0V \text{ to } V_{CC}$	—	10	μA
$ I_{LO} $	Output Leakage Current	$\overline{CE} = V_{IH}, V_{OUT} = 0V \text{ to } V_{CC}$	—	10	μA
V_{OL}	Output Low Voltage	$I_{OL} = +4mA$	—	0.4	V
V_{OH}	Output High Voltage	$I_{OH} = -4mA$	2.4	—	V

3490 tbl 05

NOTE:

- At $V_{CC} \leq 2.0V$, input leakages are undefined

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range^(4,5) ($V_{CC} = 5V \pm 10\%$)

Symbol	Parameter	Test Condition	Version	70914S12 Com'l Only		70914S15 Com'l Only		Unit
				Typ. ⁽²⁾	Max.	Typ. ⁽²⁾	Max.	
I _{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE_L}$ and $\overline{CE_R} = V_{IL}$, Outputs Disabled $f = f_{MAX}^{(1)}$	COM'L	190	310	180	300	mA
			MIL & IND	---	---	---	---	
I _{SB1}	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE_L}$ and $\overline{CE_R} = V_{IH}$ $f = f_{MAX}^{(1)}$	COM'L	95	150	90	140	mA
			MIL & IND	---	---	---	---	
I _{SB2}	Standby Current (One Port - TTL Level Inputs)	$\overline{CE_{A^*}} = V_{IL}$ and $\overline{CE_{B^*}} = V_{IH}^{(3)}$ Active Port Outputs Disabled, $f = f_{MAX}^{(1)}$	COM'L	170	220	160	210	mA
			MIL & IND	---	---	---	---	
I _{SB3}	Full Standby Current (Both Ports - All CMOS Level Inputs)	Both Ports $\overline{CE_R}$ and $\overline{CE_L} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$, $f = 0^{(2)}$	COM'L	10	15	10	15	mA
			MIL & IND	---	---	---	---	
I _{SB4}	Full Standby Current (One Port - All CMOS Level Inputs)	$\overline{CE_{A^*}} \leq 0.2V$ and $\overline{CE_{B^*}} \geq V_{CC} - 0.2V^{(3)}$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$, Active Port Outputs Disabled $f = f_{MAX}^{(1)}$	COM'L	165	210	155	200	mA
			MIL & IND	---	---	---	---	

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Symbol	Parameter	Test Condition	Version	70914S20 Com'l & Military		70914S25 Military Only		Unit
				Typ. ⁽²⁾	Max.	Typ. ⁽²⁾	Max.	
I _{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE_L}$ and $\overline{CE_R} = V_{IL}$, Outputs Disabled $f = f_{MAX}^{(1)}$	COM'L	170	290	---	---	mA
			MIL & IND	170	310	160	290	
I _{SB1}	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE_L}$ and $\overline{CE_R} = V_{IH}$ $f = f_{MAX}^{(1)}$	COM'L	85	130	---	---	mA
			MIL & IND	85	140	80	130	
I _{SB2}	Standby Current (One Port - TTL Level Inputs)	$\overline{CE_{A^*}} = V_{IL}$ and $\overline{CE_{B^*}} = V_{IH}^{(3)}$ Active Port Outputs Disabled, $f = f_{MAX}^{(1)}$	COM'L	150	200	---	---	mA
			MIL & IND	150	210	140	200	
I _{SB3}	Full Standby Current (Both Ports - All CMOS Level Inputs)	Both Ports $\overline{CE_R}$ and $\overline{CE_L} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$, $f = 0^{(2)}$	COM'L	10	15	---	---	mA
			MIL & IND	10	20	10	20	
I _{SB4}	Full Standby Current (One Port - All CMOS Level Inputs)	$\overline{CE_{A^*}} \leq 0.2V$ and $\overline{CE_{B^*}} \geq V_{CC} - 0.2V^{(3)}$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$, Active Port Outputs Disabled $f = f_{MAX}^{(1)}$	COM'L	145	190	---	---	mA
			MIL & IND	145	200	135	190	

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NOTES:

- At f_{MAX} , address and control lines (except Output Enable) are cycling at the maximum frequency clock cycle of $1/t_{cvc}$, using "AC TEST CONDITIONS" at input levels of GND to 3V.
- $f = 0$ means no address, clock, or control lines change. Applies only to input at CMOS level standby.
- Port "A" may be either left or right port. Port "B" is the opposite from port "A".
- $V_{CC} = 5V$, $T_A = 25^\circ C$ for Typ, and are not production tested. $I_{CC DC} = 150mA$ (Typ).
- Industrial temperature: for specific speeds, packages and powers contact your sales office.

AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns Max.
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	Figures 1,2 and 3

3490 tbl 07

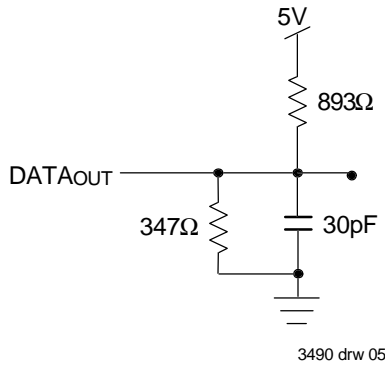


Figure 1. AC Output Test load.

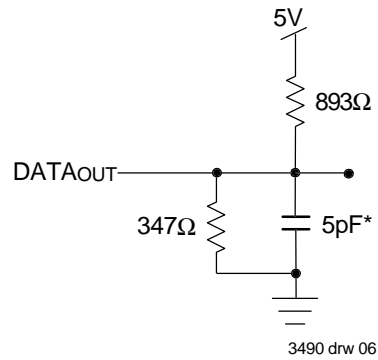


Figure 2. Output Test Load
(For tCKLZ, tCKHZ, tOLZ, and tOHZ).
*Including scope and jig.

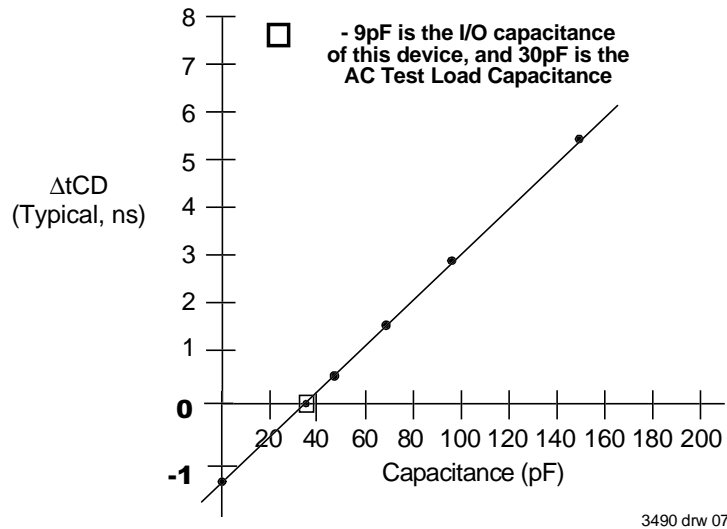


Figure 3. Typical Output Derating (Lumped Capacitive Load).

AC Electrical Characteristics Over the Operating Temperature Range (Read and Write Cycle Timing)⁽³⁾

(Commercial: $V_{CC} = 5V \pm 10\%$, $T_A = 0^\circ C$ to $+70^\circ C$; Military: $V_{CC} = 5V \pm 10\%$, $T_A = -55^\circ C$ to $+125^\circ C$)

Symbol	Parameter	70914S12 Com'l Only		70914S15 Com'l Only		Unit
		Min.	Max.	Min.	Max.	
t _{CYC}	Clock Cycle Time	16	—	20	—	ns
t _{CH}	Clock High Time	6	—	6	—	ns
t _{CL}	Clock Low Time	6	—	6	—	ns
t _{CD}	Clock High to Output Valid	—	12	—	15	ns
t _S	Registered Signal Set-up Time	4	—	4	—	ns
t _H	Registered Signal Hold Time	1	—	1	—	ns
t _{DC}	Data Output Hold After Clock High	3	—	3	—	ns
t _{CKLZ}	Clock High to Output Low-Z ^(1,2)	2	—	2	—	ns
t _{CKHZ}	Clock High to Output High-Z ^(1,2)	—	7	—	7	ns
t _{OE}	Output Enable to Output Valid	—	7	—	8	ns
t _{OLZ}	Output Enable to Output Low-Z ^(1,2)	0	—	0	—	ns
t _{OHZ}	Output Disable to Output High-Z ^(1,2)	—	7	—	7	ns
t _{SCK}	Clock Enable, Disable Set-up Time	4	—	4	—	ns
t _{HCK}	Clock Enable, Disable Hold Time	2	—	2	—	ns
Port-to-Port Delay						
t _{OWDD}	Write Port Clock High to Read Data Delay	—	25	—	30	ns
t _{CSS}	Clock-to-Clock Setup Time	—	13	—	15	ns

3490 tbl 08a

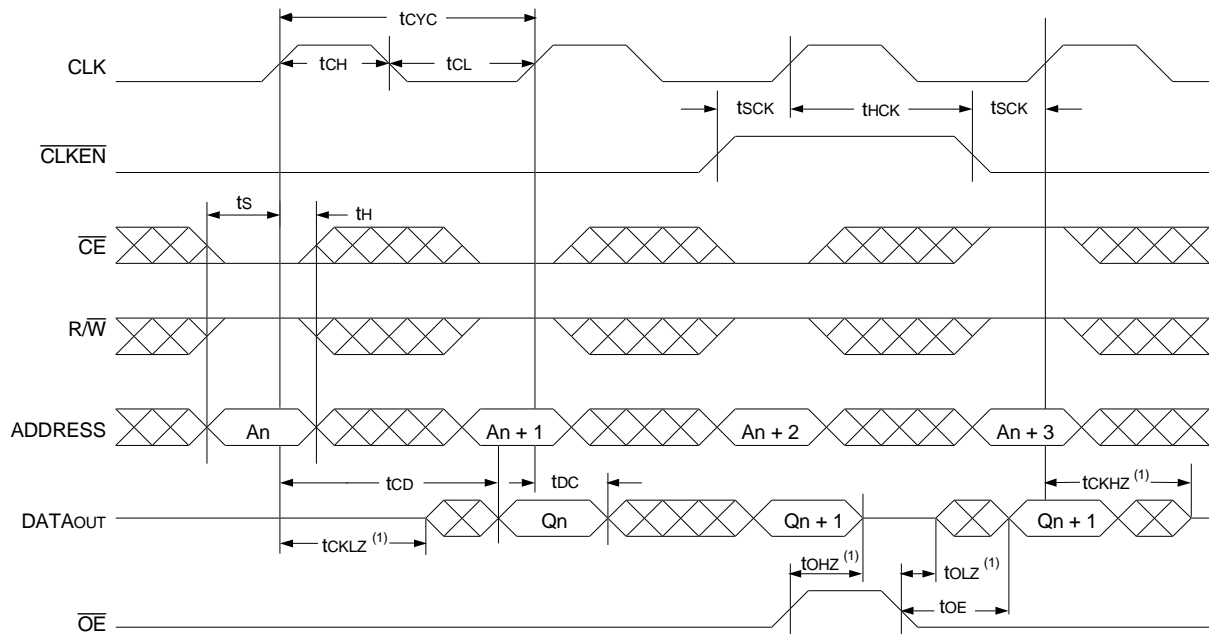
Symbol	Parameter	70914S20 Com'l & Military		70914S25 Military Only		Unit
		Min.	Max.	Min.	Max.	
t _{CYC}	Clock Cycle Time	20	—	25	—	ns
t _{CH}	Clock High Time	8	—	10	—	ns
t _{CL}	Clock Low Time	8	—	10	—	ns
t _{CD}	Clock High to Output Valid	—	20	—	25	ns
t _S	Registered Signal Set-up Time	5	—	6	—	ns
t _H	Registered Signal Hold Time	1	—	1	—	ns
t _{DC}	Data Output Hold After Clock High	3	—	3	—	ns
t _{CKLZ}	Clock High to Output Low-Z ^(1,2)	2	—	2	—	ns
t _{CKHZ}	Clock High to Output High-Z ^(1,2)	—	9	—	12	ns
t _{OE}	Output Enable to Output Valid	—	10	—	12	ns
t _{OLZ}	Output Enable to Output Low-Z ^(1,2)	0	—	0	—	ns
t _{OHZ}	Output Disable to Output High-Z ^(1,2)	—	9	—	11	ns
t _{SCK}	Clock Enable, Disable Set-up Time	5	—	6	—	ns
t _{HCK}	Clock Enable, Disable Hold Time	2	—	2	—	ns
Port-to-Port Delay						
t _{OWDD}	Write Port Clock High to Read Data Delay	—	35	—	45	ns
t _{CSS}	Clock-to-Clock Setup Time	—	15	—	20	ns

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NOTES:

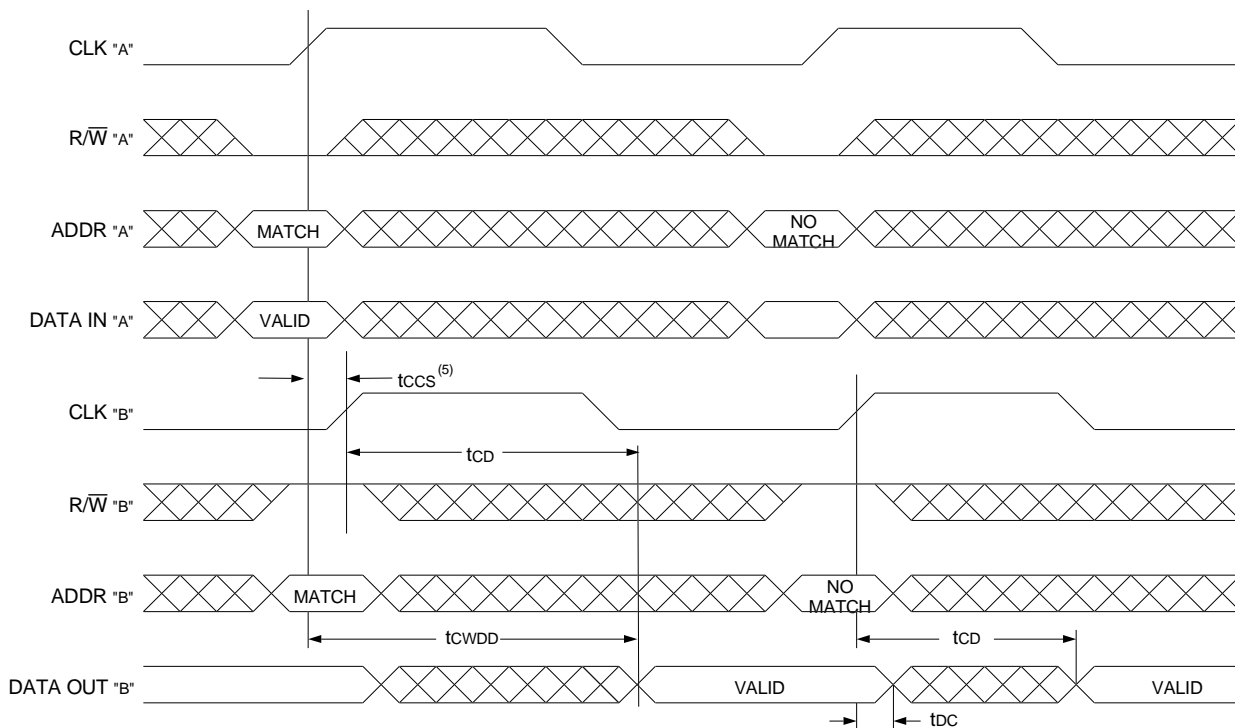
1. Transition is measured 0mV from Low or High impedance voltage with the Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterization, but is not production tested.
3. Industrial temperature: for specific speeds, packages and powers contact your sales office.

Timing Waveform of Read Cycle, Either Side



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Timing Waveform of Write with Port-to-Port Read^(2,3,4)

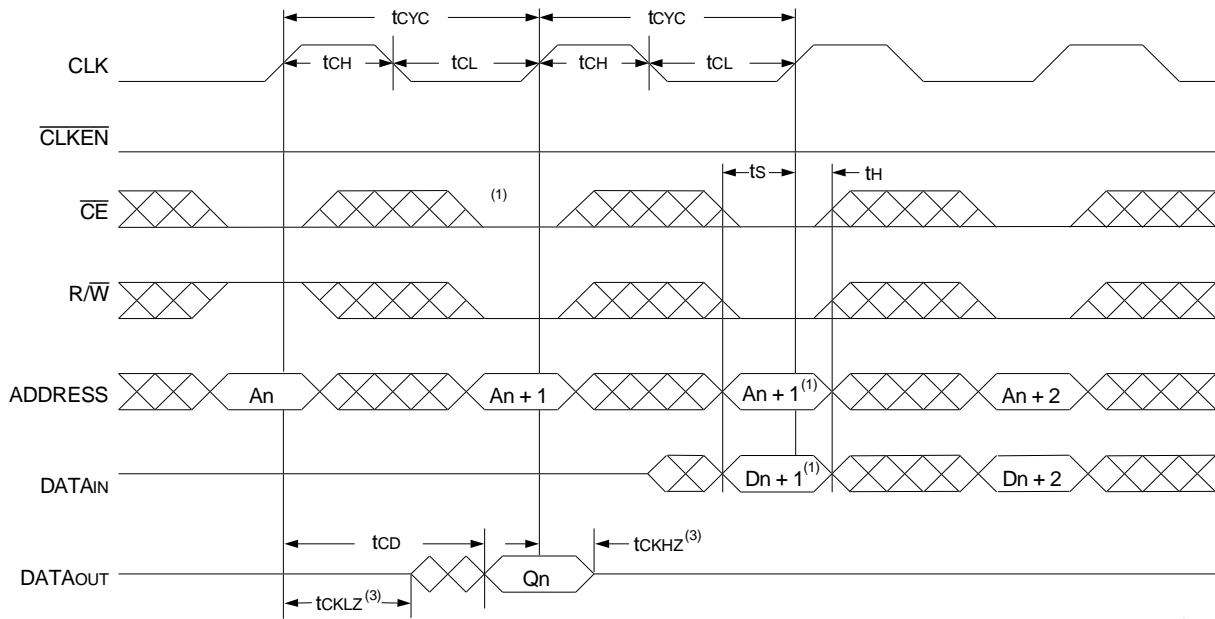


3490 drw 09

NOTES:

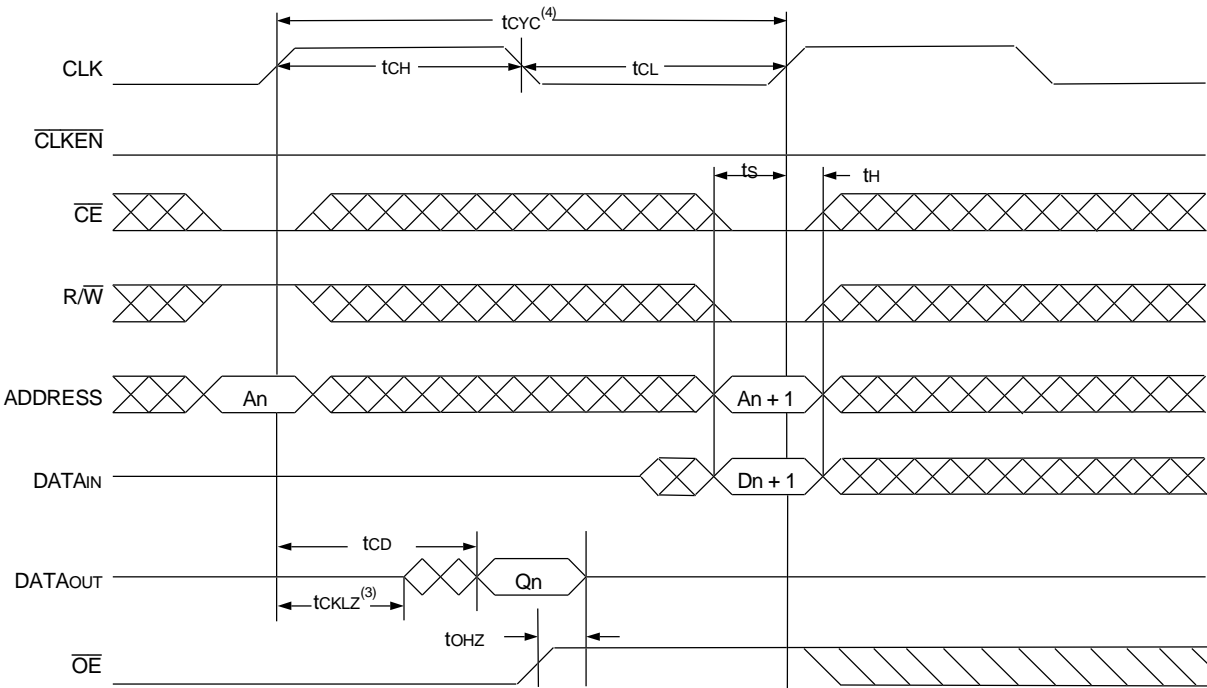
1. Transition is measured $\pm 200\text{mV}$ from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. $\overline{CE}_L = \overline{CE}_R = V_{IL}$, $\overline{CLKEN}_L = \overline{CLKEN}_R = V_{IL}$.
3. $\overline{OE} = V_{IL}$ for the reading port, port 'B'.
4. All timing is the same for left and right ports. Ports 'A' may be either the left or right port. Port 'B' is opposite from port 'A'.
5. If $t_{CCS} \leq$ maximum specified, then data from right port READ is not valid until the maximum specified for t_{CWDD} .
If $t_{CCS} >$ maximum specified, then data from right port READ is not valid until $t_{CCS} + t_{CD}$. t_{CWDD} does not apply in this case.

Timing Waveform of Read-to-Write Cycle No. 1^(1,2) (tcyc = min.)



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Timing Waveform of Read-to-Write Cycle No. 2⁽⁴⁾ (tcyc > min.)



3490 drw 11

NOTES:

1. For tcyc = min.; data out coincident with the rising edge of the subsequent write clock can occur. To ensure writing to the correct address location, the write must be repeated on the second write clock rising edge. If CE = VIL, invalid data will be written into array. The An+1 must be rewritten on the following cycle.
2. OE LOW throughout.
3. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
4. For tcyc > min.; OE may be used to avoid data out coincident with the rising edge of the subsequent write clock. Use of OE will eliminate the need for the write to be repeated.

Functional Description

The IDT70914 provides a true synchronous Dual-Port Static RAM interface. Registered inputs provide very short set-up and hold times on address, data, and all critical control inputs. All internal registers are clocked on the rising edge of the clock signal. An asynchronous output enable is provided to ease asynchronous bus interfacing.

The internal write pulse width is dependent on the LOW to HIGH

transitions of the clock signal allowing the shortest possible realized cycle times. Clock enable inputs are provided to stall the operation of the address and data input registers without introducing clock skew for very fast interleaved memory applications.

A HIGH on the \overline{CE} input for one clock cycle will power down the internal circuitry to reduce static power consumption.

Truth Table I: Read/Write Control⁽¹⁾

Inputs				Outputs	Mode
Synchronous ⁽³⁾		Asynchronous			
CLK	\overline{CE}	R/ \overline{W}	\overline{OE}	I/O ₀₋₈	
↑	H	X	X	High-Z	Deselected, Power-Down
↑	L	L	X	DATA _{IN}	Selected and Write Enabled
↑	L	H	L	DATA _{OUT}	Read Selected and Data Output Enable Read
↑	X	X	H	High-Z	Outputs Disabled

3490 tbl 09

Truth Table II: Clock Enable Function Table⁽¹⁾

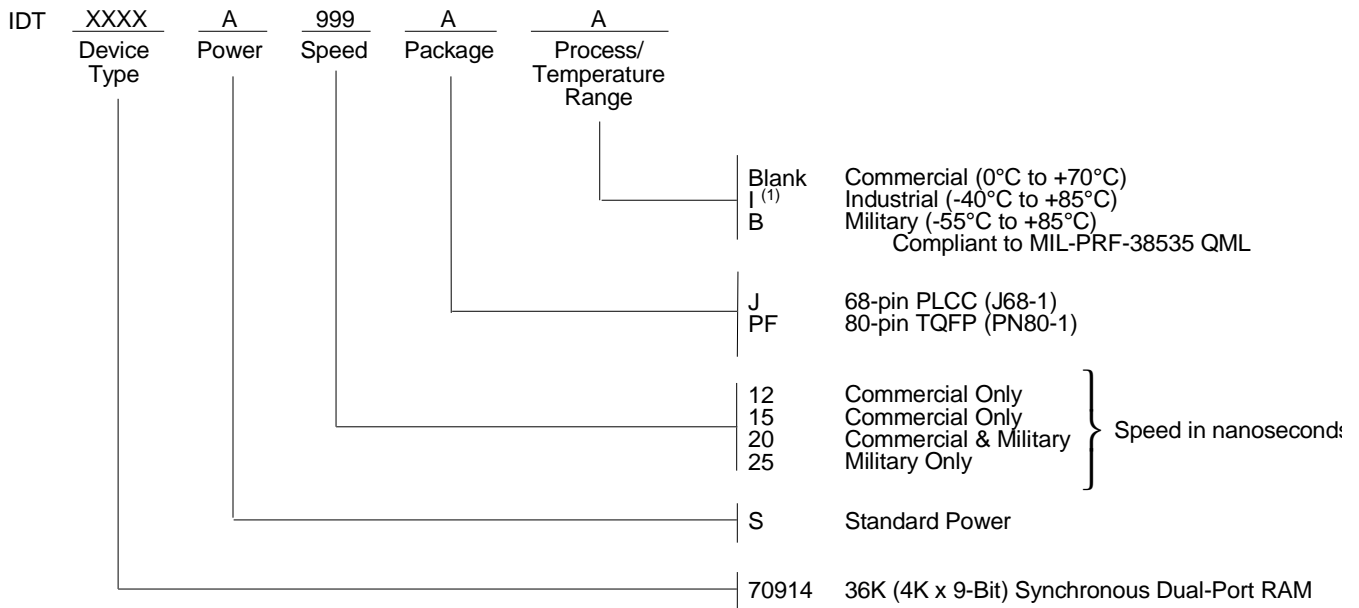
Mode	Inputs		Register Inputs		Register Outputs ⁽⁴⁾	
	CLK ⁽³⁾	\overline{CLKEN} ⁽²⁾	ADDR	DATA _{IN}	ADDR	DATA _{OUT}
Load "1"	↑	L	H	H	H	H
Load "0"	↑	L	L	L	L	L
Hold (do nothing)	↑	H	X	X	NC	NC
	X	H	X	X	NC	NC

3490 tbl 10

NOTES:

- 'H' = HIGH voltage level steady state, 'h' = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition, 'L' = LOW voltage level steady state 'l' = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition, 'X' = Don't care, 'NC' = No change
- \overline{CLKEN} = V_{IL} must be clocked in during Power-Up.
- Control signals are initiated and terminated on the rising edge of the CLK, depending on their input level. When $\overline{R/W}$ and \overline{CE} are LOW, a write cycle is initiated on the LOW-to-HIGH transition of the CLK. Termination of a write cycle is done on the next LOW-to-HIGH transition of the CLK.
- The register outputs are internal signals from the register inputs being clocked in or disabled by \overline{CLKEN} .

Ordering Information



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NOTE:

- Industrial temperature range is available on selected TQFP packages in standard power.
 For specific speeds, packages and powers contact your sales office.

Datasheet Document History

- 3/10/99: Initiated datasheet document history
 Converted to new format
 Cosmetic and typographical corrections
 Page 2 and 3 Added additional notes to pin configurations
- 6/7/99: Changed drawing format
- 11/10/99: Replaced IDT logo
- 5/24/00: Page 4 Increased storage temperature parameter
 Clarified TA parameter
 Page 5 DC Electrical parameters—changed wording from "open" to "disabled"
 Changed ±200mV to 0mV in notes
- 1/12/01: Removed PGA pinout (obsolete package)
 Changed cycle time of 12ns part from 17ns (58MHz) to 16ns (60MHz)



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