



HIGH-SPEED 3.3V 256/128K x 18 SYNCHRONOUS DUAL-PORT STATIC RAM WITH 3.3V OR 2.5V INTERFACE

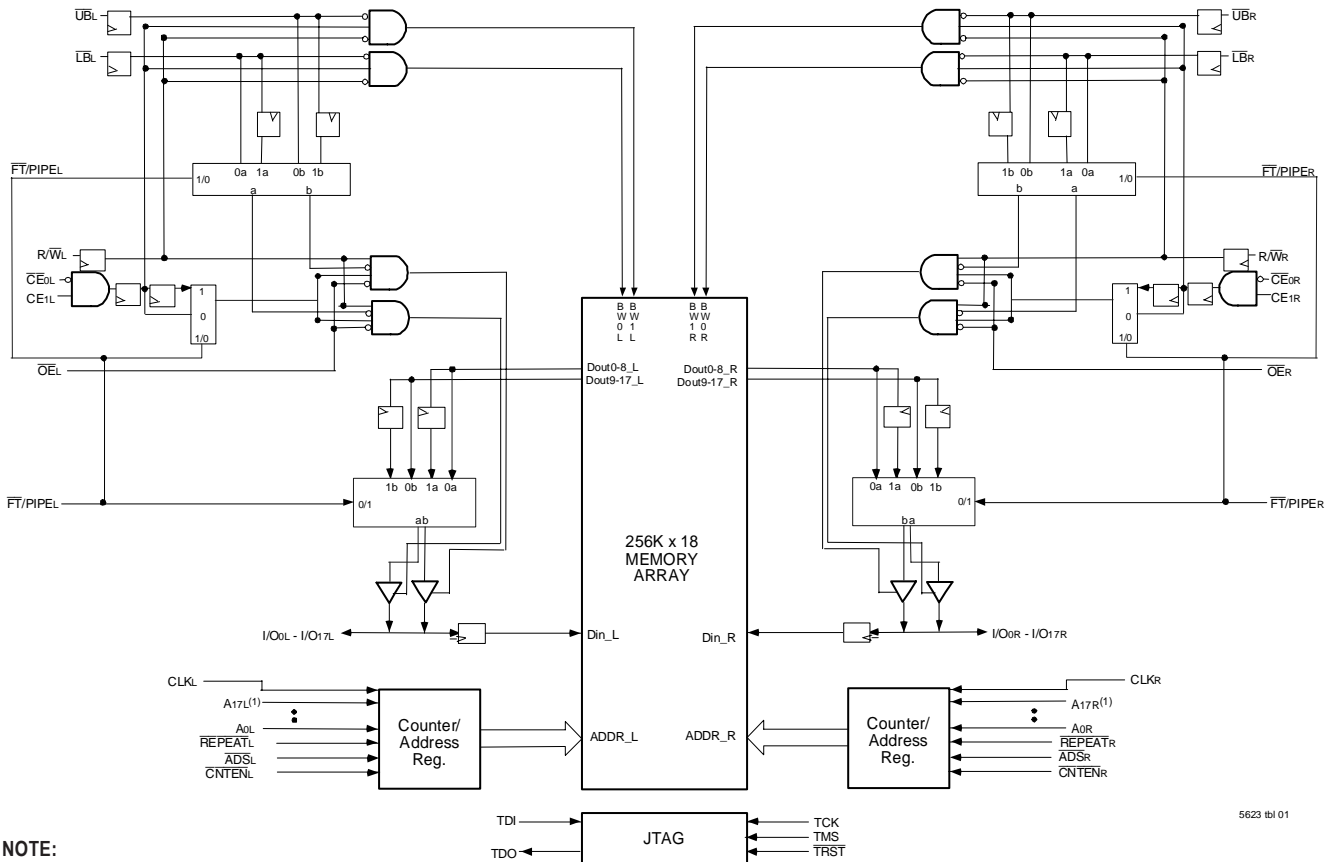
IDT70V3319/99S

Features:

- ◆ True Dual-Port memory cells which allow simultaneous access of the same memory location
- ◆ High-speed data access
 - Commercial: 3.6ns (166MHz)/4.2ns (133MHz) (max.)
 - Industrial: 4.2ns (133MHz) (max.)
- ◆ Selectable Pipelined or Flow-Through output mode
 - Due to limited pin count PL/ \overline{FT} option is not supported on the 128-pin TQFP package. Device is pipelined outputs only on each port.
- ◆ Counter enable and repeat features
- ◆ Dual chip enables allow for depth expansion without additional logic
- ◆ Full synchronous operation on both ports
 - 6ns cycle time, 166MHz operation (6Gbps bandwidth)
 - Fast 3.6ns clock to data out
 - 1.7ns setup to clock and 0.5ns hold on all control, data, and address inputs @ 166MHz

- Data input, address, byte enable and control registers
- Self-timed write allows fast cycle time
- ◆ Separate byte controls for multiplexed bus and bus matching compatibility
- ◆ Dual Cycle Deselect (DCD) for Pipelined Output mode
- ◆ LVTTTL-compatible, single 3.3V ($\pm 150\text{mV}$) power supply for core
- ◆ LVTTTL compatible, selectable 3.3V ($\pm 150\text{mV}$) or 2.5V ($\pm 100\text{mV}$) power supply for I/Os and control signals on each port
- ◆ Industrial temperature range (-40°C to +85°C) is available at 133MHz.
- ◆ Available in a 128-pin Thin Quad Flatpack, 208-pin fine pitch Ball Grid Array, and 256-pin Ball Grid Array
- ◆ Supports JTAG features compliant to IEEE 1149.1
 - Due to limited pin count, JTAG is not supported on the 128-pin TQFP package.

Functional Block Diagram



NOTE:

1. A17 is a NC for IDT70V3399.

5623 tbl 01

MAY 2003

Description:

The IDT70V3319/99 is a high-speed 256/128K x 18 bit synchronous Dual-Port RAM. The memory array utilizes Dual-Port memory cells to allow simultaneous access of any address from both ports. Registers on control, data, and address inputs provide minimal setup and hold times. The timing latitude provided by this approach allows systems to be designed with very short cycle times. With an input data register, the IDT70V3319/99 has been optimized for applications having unidirectional

or bidirectional data flow in bursts. An automatic power down feature, controlled by $\overline{CE0}$ and $CE1$, permits the on-chip circuitry of each port to enter a very low standby power mode.

The 70V3319/99 can support an operating voltage of either 3.3V or 2.5V on one or both ports, controllable by the OPT pins. The power supply for the core of the device (V_{DD}) remains at 3.3V.

Pin Configuration (1,2,3,4,5)

08/01/02	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	
	I/O _{9L}	NC	V _{SS}	TDO	NC	A _{16L}	A _{12L}	A _{8L}	NC	V _{DD}	CLK _L	\overline{CNTENL}	A _{4L}	A _{0L}	OPT _L	NC	V _{SS}	A
	NC	V _{SS}	NC	TDI	A _{17L} ⁽¹⁾	A _{13L}	A _{9L}	NC	$\overline{CE0L}$	V _{SS}	\overline{ADSL}	A _{5L}	A _{1L}	V _{SS}	V _{DDQR}	I/O _{8L}	NC	B
	V _{DDQL}	I/O _{9R}	V _{DDQR}	$\overline{PIPE/FTL}$	NC	A _{14L}	A _{10L}	\overline{UBL}	CE _{1L}	V _{SS}	\overline{RWL}	A _{6L}	A _{2L}	V _{DD}	I/O _{8R}	NC	V _{SS}	C
	NC	V _{SS}	I/O _{10L}	NC	A _{15L}	A _{11L}	A _{7L}	\overline{LBL}	V _{DD}	\overline{OEL}	$\overline{REPEATL}$	A _{3L}	V _{DD}	NC	V _{DDQL}	I/O _{7L}	I/O _{7R}	D
	I/O _{11L}	NC	V _{DDQR}	I/O _{10R}	70V3319/99BF BF-208 ⁽⁶⁾ 208-Pin fpBGA Top View ⁽⁷⁾								I/O _{6L}	NC	V _{SS}	NC	E	
	V _{DDQL}	I/O _{11R}	NC	V _{SS}									V _{SS}	I/O _{6R}	NC	V _{DDQR}	F	
	NC	V _{SS}	I/O _{12L}	NC									NC	V _{DDQL}	I/O _{5L}	NC	G	
	V _{DD}	NC	V _{DDQR}	I/O _{12R}									V _{DD}	NC	V _{SS}	I/O _{5R}	H	
	V _{DDQL}	V _{DD}	V _{SS}	V _{SS}									V _{SS}	V _{DD}	V _{SS}	V _{DDQR}	J	
	I/O _{14R}	V _{SS}	I/O _{13R}	V _{SS}									I/O _{3R}	V _{DDQL}	I/O _{4R}	V _{SS}	K	
	NC	I/O _{14L}	V _{DDQR}	I/O _{13L}									NC	I/O _{3L}	V _{SS}	I/O _{4L}	L	
	V _{DDQL}	NC	I/O _{15R}	V _{SS}									V _{SS}	NC	I/O _{2R}	V _{DDQR}	M	
	NC	V _{SS}	NC	I/O _{15L}									I/O _{1R}	V _{DDQL}	NC	I/O _{2L}	N	
	I/O _{16R}	I/O _{16L}	V _{DDQR}	NC									\overline{TRST}	A _{16R}	A _{12R}	A _{8R}	NC	V _{DD}
	V _{SS}	NC	I/O _{17R}	TCK	A _{17R} ⁽¹⁾	A _{13R}	A _{9R}	NC	$\overline{CE0R}$	V _{SS}	\overline{ADSR}	A _{5R}	A _{1R}	V _{SS}	V _{DDQL}	I/O _{0R}	V _{DDQR}	R
	NC	I/O _{17L}	V _{DDQL}	TMS	NC	A _{14R}	A _{10R}	\overline{UBR}	CE _{1R}	V _{SS}	\overline{RWR}	A _{6R}	A _{2R}	V _{SS}	NC	V _{SS}	NC	T
	V _{SS}	NC	$\overline{PIPE/FTR}$	NC	A _{15R}	A _{11R}	A _{7R}	\overline{LBR}	V _{DD}	\overline{OER}	$\overline{REPEATR}$	A _{3R}	A _{0R}	V _{DD}	OPT _R	NC	I/O _{0L}	U

5623 drw 02c

NOTES:

1. A₁₇ is a NC for IDT70V3399.
2. All V_{DD} pins must be connected to 3.3V power supply.
3. All V_{DDQ} pins must be connected to appropriate power supply: 3.3V if OPT pin for that port is set to V_{IH} (3.3V), and 2.5V if OPT pin for that port is set to V_{IL} (0V).
4. All V_{SS} pins must be connected to ground supply.
5. Package body is approximately 15mm x 15mm x 1.4mm with 0.8mm ball pitch.
6. This package code is used to reference the package diagram.
7. This text does not indicate orientation of the actual part-marking.

Pin Configuration^(1,2,3,4,5) (con't.)

70V3319/99BC

BC-256⁽⁶⁾

256-Pin BGA

Top View⁽⁷⁾

08/01/02

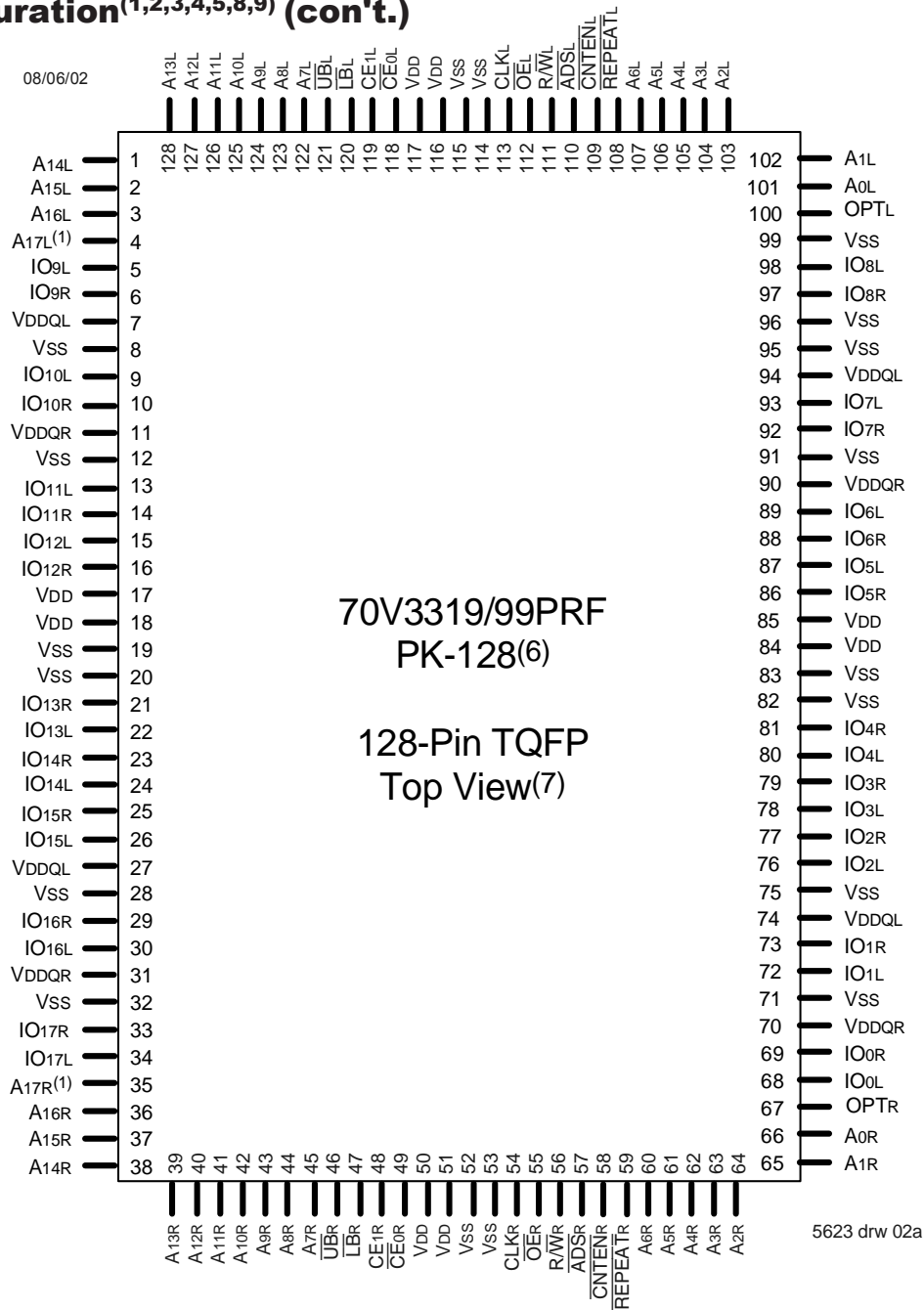
A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13	A14	A15	A16
NC	TDI	NC	A17L ⁽¹⁾	A14L	A11L	A8L	NC	CE1L	OE _L	CNTEN _L	A5L	A2L	A0L	NC	NC
B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12	B13	B14	B15	B16
NC	NC	TDO	NC	A15L	A12L	A9L	UB _L	CE0L	R/W _L	REPEAT _L	A4L	A1L	VDD	NC	NC
C1	C2	C3	C4	C5	C6	C7	C8	C9	C10	C11	C12	C13	C14	C15	C16
NC	I/O9L	VSS	A16L	A13L	A10L	A7L	NC	LB _L	CLK _L	ADSL	A6L	A3L	OPT _L	NC	I/O8L
D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	D16
NC	I/O9R	NC	PIPE/FT _L	VDDQL	VDDQL	VDDQR	VDDQR	VDDQL	VDDQL	VDDQR	VDDQR	VDD	NC	NC	I/O8R
E1	E2	E3	E4	E5	E6	E7	E8	E9	E10	E11	E12	E13	E14	E15	E16
I/O10R	I/O10L	NC	VDDQL	VDD	VDD	VSS	VSS	VSS	VSS	VDD	VDD	VDDQR	NC	I/O7L	I/O7R
F1	F2	F3	F4	F5	F6	F7	F8	F9	F10	F11	F12	F13	F14	F15	F16
I/O11L	NC	I/O11R	VDDQL	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VDD	VDDQR	I/O6R	NC	I/O6L
G1	G2	G3	G4	G5	G6	G7	G8	G9	G10	G11	G12	G13	G14	G15	G16
NC	NC	I/O12L	VDDQR	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDDQL	I/O5L	NC	NC
H1	H2	H3	H4	H5	H6	H7	H8	H9	H10	H11	H12	H13	H14	H15	H16
NC	I/O12R	NC	VDDQR	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDDQL	NC	NC	I/O5R
J1	J2	J3	J4	J5	J6	J7	J8	J9	J10	J11	J12	J13	J14	J15	J16
I/O13L	I/O14R	I/O13R	VDDQL	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDDQR	I/O4R	I/O3R	I/O4L
K1	K2	K3	K4	K5	K6	K7	K8	K9	K10	K11	K12	K13	K14	K15	K16
NC	NC	I/O14L	VDDQL	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDDQR	NC	NC	I/O3L
L1	L2	L3	L4	L5	L6	L7	L8	L9	L10	L11	L12	L13	L14	L15	L16
I/O15L	NC	I/O15R	VDDQR	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VDD	VDDQL	I/O2L	NC	I/O2R
M1	M2	M3	M4	M5	M6	M7	M8	M9	M10	M11	M12	M13	M14	M15	M16
I/O16R	I/O16L	NC	VDDQR	VDD	VDD	VSS	VSS	VSS	VSS	VDD	VDD	VDDQL	I/O1R	I/O1L	NC
N1	N2	N3	N4	N5	N6	N7	N8	N9	N10	N11	N12	N13	N14	N15	N16
NC	I/O17R	NC	PIPE/FT _R	VDDQR	VDDQR	VDDQL	VDDQL	VDDQR	VDDQR	VDDQL	VDDQL	VDD	NC	I/O0R	NC
P1	P2	P3	P4	P5	P6	P7	P8	P9	P10	P11	P12	P13	P14	P15	P16
NC	I/O17L	TMS	A16R	A13R	A10R	A7R	NC	LB _R	CLK _R	ADSR	A6R	A3R	NC	NC	I/O0L
R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	R11	R12	R13	R14	R15	R16
NC	NC	TRST	NC	A15R	A12R	A9R	UB _R	CE0R	R/W _R	REPEAT _R	A4R	A1R	OPT _R	NC	NC
T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13	T14	T15	T16
NC	TCK	NC	A17R ⁽¹⁾	A14R	A11R	A8R	NC	CE1R	OE _R	CNTEN _R	A5R	A2R	A0R	NC	NC

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NOTES:

1. A17 is a NC for IDT70V3399.
2. All VDD pins must be connected to 3.3V power supply.
3. All VDDQ pins must be connected to appropriate power supply: 3.3V if OPT pin for that port is set to VIH (3.3V), and 2.5V if OPT pin for that port is set to VIL (0V).
4. All VSS pins must be connected to ground supply.
5. Package body is approximately 17mm x 17mm x 1.4mm, with 1.0mm ball-pitch.
6. This package code is used to reference the package diagram.
7. This text does not indicate orientation of the actual part-marking.

Pin Configuration(1,2,3,4,5,8,9) (con't.)



NOTES:

1. A17 is a NC for IDT70V3399.
2. All VDD pins must be connected to 3.3V power supply.
3. All VDDQ pins must be connected to appropriate power supply: 3.3V if OPT pin for that port is set to V_{IH} (3.3V), and 2.5V if OPT pin for that port is set to V_{IL} (0V).
4. All VSS pins must be connected to ground supply.
5. Package body is approximately 14mm x 20mm x 1.4mm.
6. This package code is used to reference the package diagram.
7. This text does not indicate orientation of the actual part-marking.
8. PIPE/FT option in PK-128 is not supported due to limitation in pin count. Device is pipelined outputs only on each port.
9. Due to the limited pin count, JTAG is not supported in the PK-128 package.

Pin Names

Left Port	Right Port	Names
\overline{CE}_{0L} , CE_{1L}	\overline{CE}_{0R} , CE_{1R}	Chip Enables ⁽⁶⁾
R/\overline{WL}	R/\overline{WR}	Read/Write Enable
\overline{OE}_L	\overline{OE}_R	Output Enable
A_{0L} - A_{17L} ⁽¹⁾	A_{0R} - A_{17R} ⁽¹⁾	Address
I/O_{0L} - I/O_{17L}	I/O_{0R} - I/O_{17R}	Data Input/Output
CLK_L	CLK_R	Clock
$PIPE/\overline{FT}_L$ ⁽⁶⁾	$PIPE/\overline{FT}_R$ ⁽⁶⁾	Pipeline/Flow-Through
\overline{ADS}_L	\overline{ADS}_R	Address Strobe Enable
\overline{CNTEN}_L	\overline{CNTEN}_R	Counter Enable
\overline{REPEAT}_L	\overline{REPEAT}_R	Counter Repeat ⁽⁴⁾
\overline{UB}_L	\overline{UB}_R	Upper Byte Enable (I/O_9 - I/O_{17}) ⁽⁶⁾
\overline{LB}_L	\overline{LB}_R	Lower Byte Enable (I/O_0 - I/O_8) ⁽⁶⁾
V_{DDQL}	V_{DDQR}	Power (I/O Bus) (3.3V or 2.5V) ⁽²⁾
OPT_L	OPT_R	Option for selecting V_{DDQX} ^(2,3)
V_{DD}		Power (3.3V) ⁽²⁾
V_{SS}		Ground (0V)
TDI		Test Data Input
TDO		Test Data Output
TCK		Test Logic Clock (10MHz)
TMS		Test Mode Select
\overline{TRST}		Reset (Initialize TAP Controller)

5623 tbl 01

NOTES:

1. A_{17} is a NC for IDT70V3399.
2. V_{DD} , OPT_x , and V_{DDQX} must be set to appropriate operating levels prior to applying inputs on the I/Os and controls for that port.
3. OPT_x selects the operating voltage levels for the I/Os and controls on that port. If OPT_x is set to VIH (3.3V), then that port's I/Os and controls will operate at 3.3V levels and V_{DDQX} must be supplied at 3.3V. If OPT_x is set to VIL (0V), then that port's I/Os and address controls will operate at 2.5V levels and V_{DDQX} must be supplied at 2.5V. The OPT pins are independent of one another—both ports can operate at 3.3V levels, both can operate at 2.5V levels, or either can operate at 3.3V with the other at 2.5V.
4. When \overline{REPEAT}_x is asserted, the counter will reset to the last valid address loaded via \overline{ADS}_x .
5. PIPE/ \overline{FT} option in PK-128 package is not supported due to limitation in pin count. Device is pipelined output mode only on each port.
6. Chip Enables and Byte Enables are double buffered when $PL/\overline{FT} = V_{IH}$, i.e., the signals take two cycles to deselect.

Truth Table I—Read/Write and Enable Control^(1,2,3)

\overline{OE}	CLK	$\overline{CE_0}$	CE ₁	\overline{UB}	\overline{LB}	R/ \overline{W}	Upper Byte I/O ₉₋₁₇	Lower Byte I/O ₀₋₈	MODE
X	↑	H	X	X	X	X	High-Z	High-Z	Deselected—Power Down
X	↑	X	L	X	X	X	High-Z	High-Z	Deselected—Power Down
X	↑	L	H	H	H	X	High-Z	High-Z	Both Bytes Deselected
X	↑	L	H	H	L	L	High-Z	D _{IN}	Write to Lower Byte Only
X	↑	L	H	L	H	L	D _{IN}	High-Z	Write to Upper Byte Only
X	↑	L	H	L	L	L	D _{IN}	D _{IN}	Write to Both Bytes
L	↑	L	H	H	L	H	High-Z	D _{OUT}	Read Lower Byte Only
L	↑	L	H	L	H	H	D _{OUT}	High-Z	Read Upper Byte Only
L	↑	L	H	L	L	H	D _{OUT}	D _{OUT}	Read Both Bytes
H	↑	L	H	L	L	X	High-Z	High-Z	Outputs Disabled

5623 tbl 02

NOTES:

- "H" = V_{IH}, "L" = V_{IL}, "X" = Don't Care.
- \overline{ADS} , CNTEN, REPEAT = V_{IH}.
- \overline{OE} is an asynchronous input signal.

Truth Table II—Address Counter Control^(1,2)

External Address	Previous Internal Address	Internal Address Used	CLK	\overline{ADS}	\overline{CNTEN}	REPEAT ⁽⁶⁾	I/O ⁽⁹⁾	MODE
X	X	A _n	↑	X	X	L ⁽⁴⁾	D _{I/O} (0)	Counter Reset to last valid \overline{ADS} load
A _n	X	A _n	↑	L ⁽⁴⁾	X	H	D _{I/O} (n)	External Address Used
A _n	A _p	A _p	↑	H	H	H	D _{I/O} (p)	External Address Blocked—Counter disabled (A _p reused)
X	A _p	A _p + 1	↑	H	L ⁽⁵⁾	H	D _{I/O} (p+1)	Counter Enabled—Internal Address generation

5623 tbl 03

NOTES:

- "H" = V_{IH}, "L" = V_{IL}, "X" = Don't Care.
- Read and write operations are controlled by the appropriate setting of R/ \overline{W} , $\overline{CE_0}$, CE₁, \overline{UB} , \overline{LB} and \overline{OE} .
- Outputs configured in flow-through output mode: if outputs are in pipelined mode the data out will be delayed by one cycle.
- \overline{ADS} and REPEAT are independent of all other memory control signals including $\overline{CE_0}$, CE₁ and \overline{UB} , \overline{LB} .
- The address counter advances if CNTEN = V_{IL} on the rising edge of CLK, regardless of all other memory control signals including $\overline{CE_0}$, CE₁, \overline{UB} , \overline{LB} .
- When REPEAT is asserted, the counter will reset to the last valid address loaded via \overline{ADS} . This value is not set at power-up: a known location should be loaded via \overline{ADS} during initialization if desired. Any subsequent \overline{ADS} access during operations will update the REPEAT address location.

Recommended Operating Temperature and Supply Voltage⁽¹⁾

Grade	Ambient Temperature	GND	VDD
Commercial	0°C to +70°C	0V	3.3V \pm 150mV
Industrial	-40°C to +85°C	0V	3.3V \pm 150mV

5623 tbl 04

NOTES:

1. This is the parameter TA. This is the "instant on" case temperature.

Absolute Maximum Ratings⁽¹⁾

Symbol	Rating	Commercial & Industrial	Unit
V _{TERM} ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
T _{BIAS} ⁽³⁾	Temperature Under Bias	-55 to +125	°C
T _{STG}	Storage Temperature	-65 to +150	°C
T _{JN}	Junction Temperature	+150	°C
I _{OUT}	DC Output Current	50	mA

5623 tbl 06

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed V_{DD} + 150mV for more than 25% of the cycle time or 4ns maximum, and is limited to \leq 20mA for the period of V_{TERM} \geq V_{DD} + 150mV.
3. Ambient Temperature Under Bias. No AC Conditions. Chip Deselected.

Recommended DC Operating Conditions with VDDQ at 2.5V

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{DD}	Core Supply Voltage	3.15	3.3	3.45	V
V _{DDQ}	I/O Supply Voltage ⁽²⁾	2.4	2.5	2.6	V
V _{SS}	Ground	0	0	0	V
V _{IH}	Input High Voltage (Address & Control Inputs)	1.7	—	V _{DDQ} + 100mV ⁽²⁾	V
V _{IH}	Input High Voltage - I/O ⁽³⁾	1.7	—	V _{DDQ} + 100mV ⁽²⁾	V
V _{IL}	Input Low Voltage	-0.3 ⁽¹⁾	—	0.7	V

5623 tbl 05a

NOTES:

1. Undershoot of V_{IL} \geq -1.5V for pulse width less than 10ns is allowed.
2. V_{TERM} must not exceed V_{DDQ} + 100mV.
3. To select operation at 2.5V levels on the I/Os and controls of a given port, the OPT pin for that port must be set to V_{IL} (0V), and V_{DDQX} for that port must be supplied as indicated above.

Recommended DC Operating Conditions with VDDQ at 3.3V

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{DD}	Core Supply Voltage	3.15	3.3	3.45	V
V _{DDQ}	I/O Supply Voltage ⁽²⁾	3.15	3.3	3.45	V
V _{SS}	Ground	0	0	0	V
V _{IH}	Input High Voltage (Address & Control Inputs) ⁽³⁾	2.0	—	V _{DDQ} + 150mV ⁽²⁾	V
V _{IH}	Input High Voltage - I/O ⁽³⁾	2.0	—	V _{DDQ} + 150mV ⁽²⁾	V
V _{IL}	Input Low Voltage	-0.3 ⁽¹⁾	—	0.8	V

5623 tbl 05b

NOTES:

1. Undershoot of V_{IL} \geq -1.5V for pulse width less than 10ns is allowed.
2. V_{TERM} must not exceed V_{DDQ} + 150mV.
3. To select operation at 3.3V levels on the I/Os and controls of a given port, the OPT pin for that port must be set to V_{IH} (3.3V), and V_{DDQX} for that port must be supplied as indicated above.

Capacitance⁽¹⁾ ($T_A = +25^\circ\text{C}$, $F = 1.0\text{MHz}$)

Symbol	Parameter	Conditions ⁽²⁾	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 3dV	8	pF
C _{OUT} ⁽³⁾	Output Capacitance	V _{OUT} = 3dV	10.5	pF

5623 tbl 07

NOTES:

1. These parameters are determined by device characterization, but are not production tested.
2. 3dV references the interpolated capacitance when the input and output switch from 0V to 3V or from 3V to 0V.
3. C_{OUT} also references C_{IO}.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range ($V_{DD} = 3.3\text{V} \pm 150\text{mV}$)

Symbol	Parameter	Test Conditions	70V3319/99S		Unit
			Min.	Max.	
I _L	Input Leakage Current ⁽¹⁾	V _{DDQ} = Max., V _{IN} = 0V to V _{DDQ}	—	10	μA
I _{LO}	Output Leakage Current ⁽¹⁾	$\overline{CE}_0 = V_H$ or $CE_1 = V_L$, V _{OUT} = 0V to V _{DDQ}	—	10	μA
V _{OL} (3.3V)	Output Low Voltage ⁽²⁾	I _{OL} = +4mA, V _{DDQ} = Min.	—	0.4	V
V _{OH} (3.3V)	Output High Voltage ⁽²⁾	I _{OH} = -4mA, V _{DDQ} = Min.	2.4	—	V
V _{OL} (2.5V)	Output Low Voltage ⁽²⁾	I _{OL} = +2mA, V _{DDQ} = Min.	—	0.4	V
V _{OH} (2.5V)	Output High Voltage ⁽²⁾	I _{OH} = -2mA, V _{DDQ} = Min.	2.0	—	V

5623 tbl 08

NOTE:

1. At V_{DD} ≤ 2.0V leakages are undefined.
2. V_{DDQ} is selectable (3.3V/2.5V) via OPT pins. Refer to p.5 for details.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range⁽³⁾ ($V_{DD} = 3.3V \pm 150mV$)

Symbol	Parameter	Test Condition	Version	70V3319/99S166 Com'l Only		70V3319/99S133 Com'l & Ind		Unit	
				Typ. ⁽⁴⁾	Max.	Typ. ⁽⁴⁾	Max.		
IDD	Dynamic Operating Current (Both Ports Active)	\overline{CE}_L and $\overline{CE}_R = V_{IL}$, Outputs Disabled, $f = f_{MAX}^{(1)}$	COM'L	S	370	500	320	400	mA
			IND	S	—	—	320	480	
ISB1	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_L = \overline{CE}_R = V_{IH}$, Outputs Disabled, $f = f_{MAX}^{(1)}$	COM'L	S	125	200	115	160	mA
			IND	S	—	—	115	195	
ISB2	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}^*A = V_{IL}$ and $\overline{CE}^*B = V_{IH}^{(5)}$ Active Port Outputs Disabled, $f = f_{MAX}^{(1)}$	COM'L	S	250	350	220	290	mA
			IND	S	—	—	220	350	
ISB3	Full Standby Current (Both Ports - CMOS Level Inputs)	Both Ports Outputs Disabled \overline{CE}_L and $\overline{CE}_R \geq V_{DD} - 0.2V$, $V_{IN} \geq V_{DD} - 0.2V$ or $V_{IN} \leq 0.2V$, $f = 0^{(2)}$	COM'L	S	15	30	15	30	mA
			IND	S	—	—	15	40	
ISB4	Full Standby Current (One Port - CMOS Level Inputs)	$\overline{CE}^*A \leq 0.2V$ and $\overline{CE}^*B \geq V_{DD} - 0.2V^{(5)}$ $V_{IN} \geq V_{DD} - 0.2V$ or $V_{IN} \leq 0.2V$ Active Port, Outputs Disabled, $f = f_{MAX}^{(1)}$	COM'L	S	250	350	220	290	mA
			IND	S	—	—	220	350	

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NOTES:

- At $f = f_{MAX}$, address and control lines (except Output Enable) are cycling at the maximum frequency clock cycle of $1/t_{cyc}$, using "AC TEST CONDITIONS" at input levels of GND to 3V.
- $f = 0$ means no address, clock, or control lines change. Applies only to input at CMOS level standby.
- Port "A" may be either left or right port. Port "B" is the opposite from port "A".
- $V_{DD} = 3.3V$, $T_A = 25^\circ C$ for Typ, and are not production tested. $I_{DD} DC(f=0) = 120mA$ (Typ).
- $\overline{CE}_X = V_{IL}$ means $\overline{CE}_{0X} = V_{IL}$ and $CE_{1X} = V_{IH}$
 $\overline{CE}_X = V_{IH}$ means $\overline{CE}_{0X} = V_{IH}$ or $CE_{1X} = V_{IL}$
 $\overline{CE}_X \leq 0.2V$ means $\overline{CE}_{0X} \leq 0.2V$ and $CE_{1X} \geq V_{CC} - 0.2V$
 $\overline{CE}_X \geq V_{CC} - 0.2V$ means $\overline{CE}_{0X} \geq V_{CC} - 0.2V$ or $CE_{1X} = 0.2V$
 "X" represents "L" for left port or "R" for right port.

AC Test Conditions (V_{DDQ} - 3.3V/2.5V)

Input Pulse Levels (Address & Controls)	GND to 3.0V/GND to 2.4V
Input Pulse Levels (I/Os)	GND to 3.0V/GND to 2.4V
Input Rise/Fall Times	2ns
Input Timing Reference Levels	1.5V/1.25V
Output Reference Levels	1.5V/1.25V
Output Load	Figures 1 and 2

5623 tbl 10

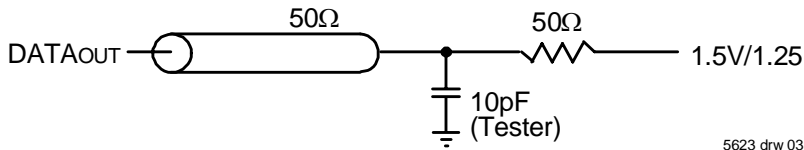


Figure 1. AC Output Test load.

5623 drw 03

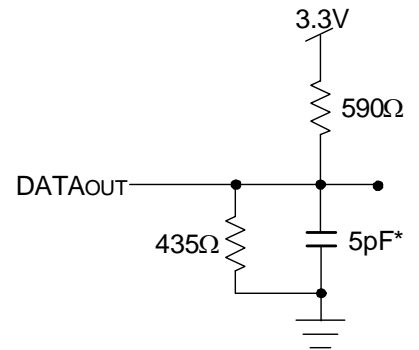
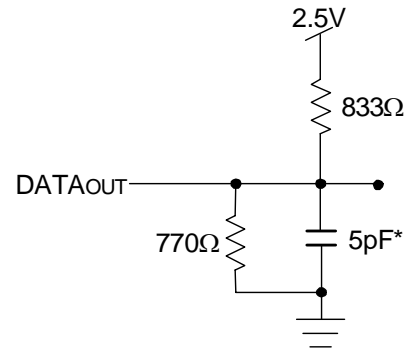
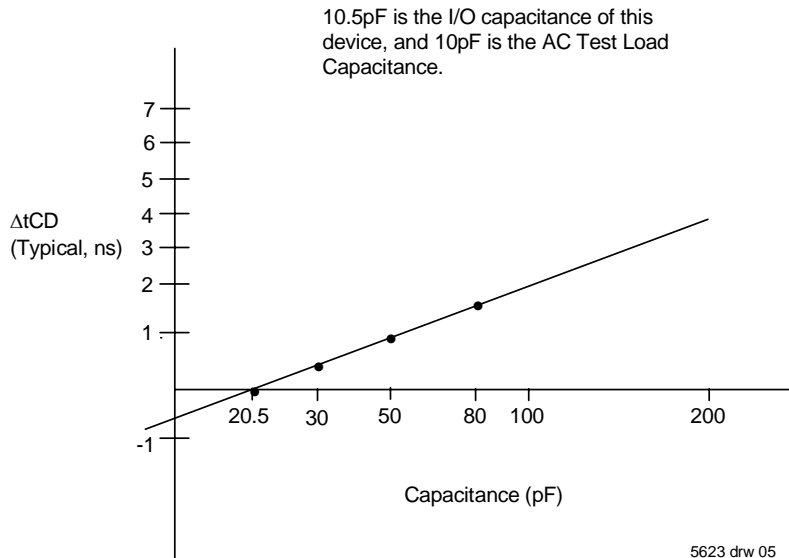


Figure 2. Output Test Load
(For t_{CKLZ}, t_{CKHZ}, t_{OLZ}, and t_{OHZ}).
*Including scope and jig.

5623 drw 04



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Figure 3. Typical Output Derating (Lumped Capacitive Load).

AC Electrical Characteristics Over the Operating Temperature Range (Read and Write Cycle Timing)^(2,3) ($V_{DD} = 3.3V \pm 150mV$, $T_A = 0^\circ C$ to $+70^\circ C$)

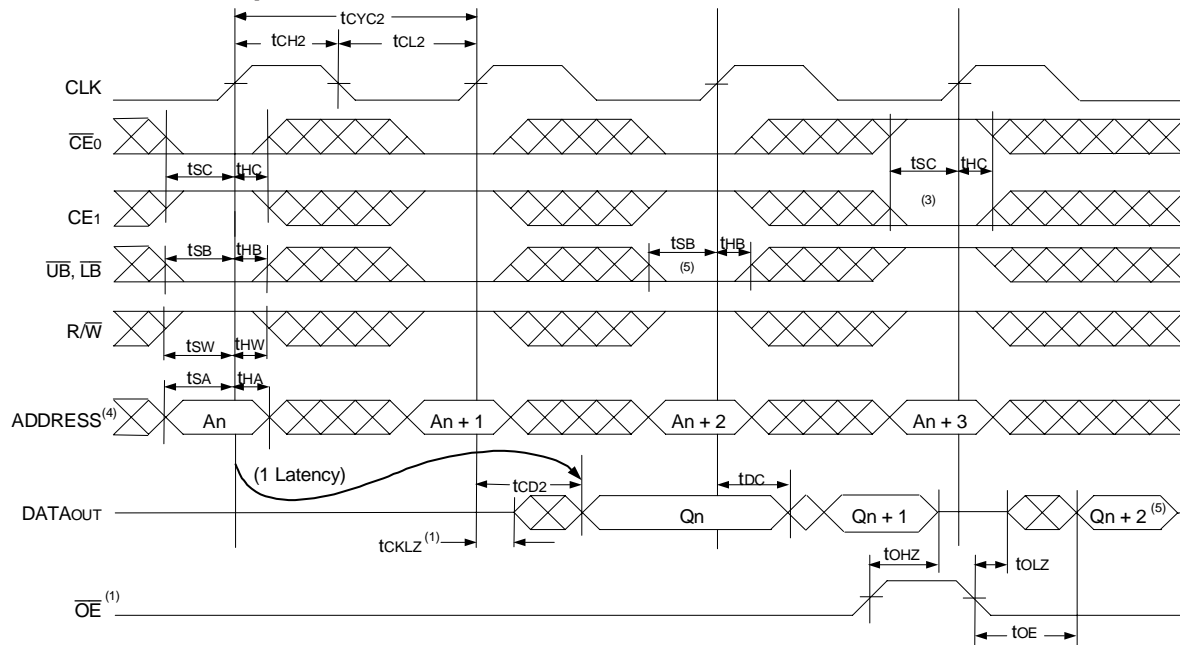
Symbol	Parameter	70V3319/99S166 Com'l Only		70V3319/99S133 Com'l & Ind		Unit
		Min.	Max.	Min.	Max.	
t _{CYC1}	Clock Cycle Time (Flow-Through) ⁽¹⁾	20	—	25	—	ns
t _{CYC2}	Clock Cycle Time (Pipelined) ⁽¹⁾	6	—	7.5	—	ns
t _{CH1}	Clock High Time (Flow-Through) ⁽¹⁾	6	—	7	—	ns
t _{CL1}	Clock Low Time (Flow-Through) ⁽¹⁾	6	—	7	—	ns
t _{CH2}	Clock High Time (Pipelined) ⁽²⁾	2.1	—	2.6	—	ns
t _{CL2}	Clock Low Time (Pipelined) ⁽¹⁾	2.1	—	2.6	—	ns
t _{SA}	Address Setup Time	1.7	—	1.8	—	ns
t _{HA}	Address Hold Time	0.5	—	0.5	—	ns
t _{SC}	Chip Enable Setup Time	1.7	—	1.8	—	ns
t _{HC}	Chip Enable Hold Time	0.5	—	0.5	—	ns
t _{SB}	Byte Enable Setup Time	1.7	—	1.8	—	ns
t _{HB}	Byte Enable Hold Time	0.5	—	0.5	—	ns
t _{SW}	R/W Setup Time	1.7	—	1.8	—	ns
t _{HW}	R/W Hold Time	0.5	—	0.5	—	ns
t _{SD}	Input Data Setup Time	1.7	—	1.8	—	ns
t _{HD}	Input Data Hold Time	0.5	—	0.5	—	ns
t _{SAD}	\overline{ADS} Setup Time	1.7	—	1.8	—	ns
t _{HAD}	\overline{ADS} Hold Time	0.5	—	0.5	—	ns
t _{SCN}	\overline{CNTEN} Setup Time	1.7	—	1.8	—	ns
t _{HCN}	\overline{CNTEN} Hold Time	0.5	—	0.5	—	ns
t _{SRPT}	\overline{REPEAT} Setup Time	1.7	—	1.8	—	ns
t _{HRPT}	\overline{REPEAT} Hold Time	0.5	—	0.5	—	ns
t _{OE}	Output Enable to Data Valid	—	4.0	—	4.2	ns
t _{OLZ}	Output Enable to Output Low-Z	1	—	1	—	ns
t _{OHZ}	Output Enable to Output High-Z	1	3.6	1	4.2	ns
t _{CD1}	Clock to Data Valid (Flow-Through) ⁽¹⁾	—	12	—	15	ns
t _{CD2}	Clock to Data Valid (Pipelined) ⁽¹⁾	—	3.6	—	4.2	ns
t _{DC}	Data Output Hold After Clock High	1	—	1	—	ns
t _{CKHZ}	Clock High to Output High-Z	1	3	1	3	ns
t _{CKLZ}	Clock High to Output Low-Z	1	—	1	—	ns
Port-to-Port Delay						
t _{CO}	Clock-to-Clock Offset	5	—	6	—	ns

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NOTES:

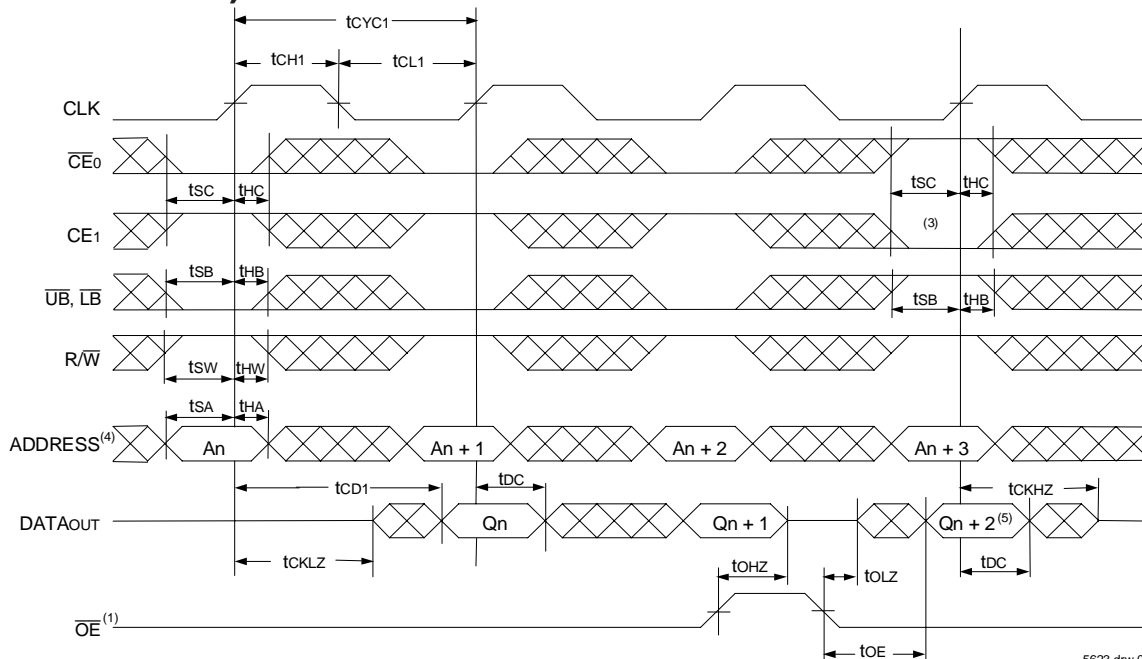
- The Pipelined output parameters (t_{CYC2}, t_{CD2}) apply to either or both left and right ports when $\overline{FT}/PIPE_x = V_{IH}$. Flow-through parameters (t_{CYC1}, t_{CD1}) apply when $\overline{FT}/PIPE = V_{IL}$ for that port.
- All input signals are synchronous with respect to the clock except for the asynchronous Output Enable (\overline{OE}) and $\overline{FT}/PIPE$. $\overline{FT}/PIPE$ should be treated as a DC signal, i.e. steady state during operation.
- These values are valid for either level of V_{DDQ} (3.3V/2.5V). See page 5 for details on selecting the desired operating voltage levels for each port.

Timing Waveform of Read Cycle for Pipelined Operation ($\overline{FT}/\text{PIPE}^* = V_{IH}$)⁽²⁾



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Timing Waveform of Read Cycle for Flow-through Output ($\overline{FT}/\text{PIPE}^* = V_{IL}$)^(2,6)

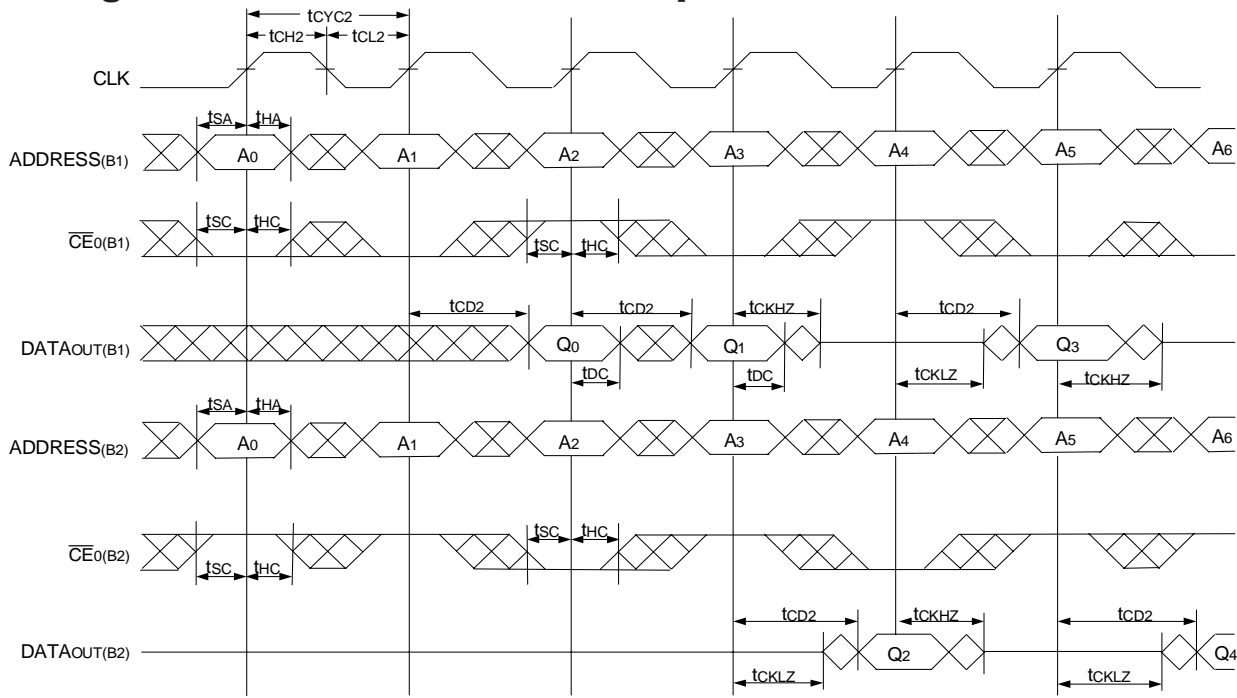


5623 drw 07

NOTES:

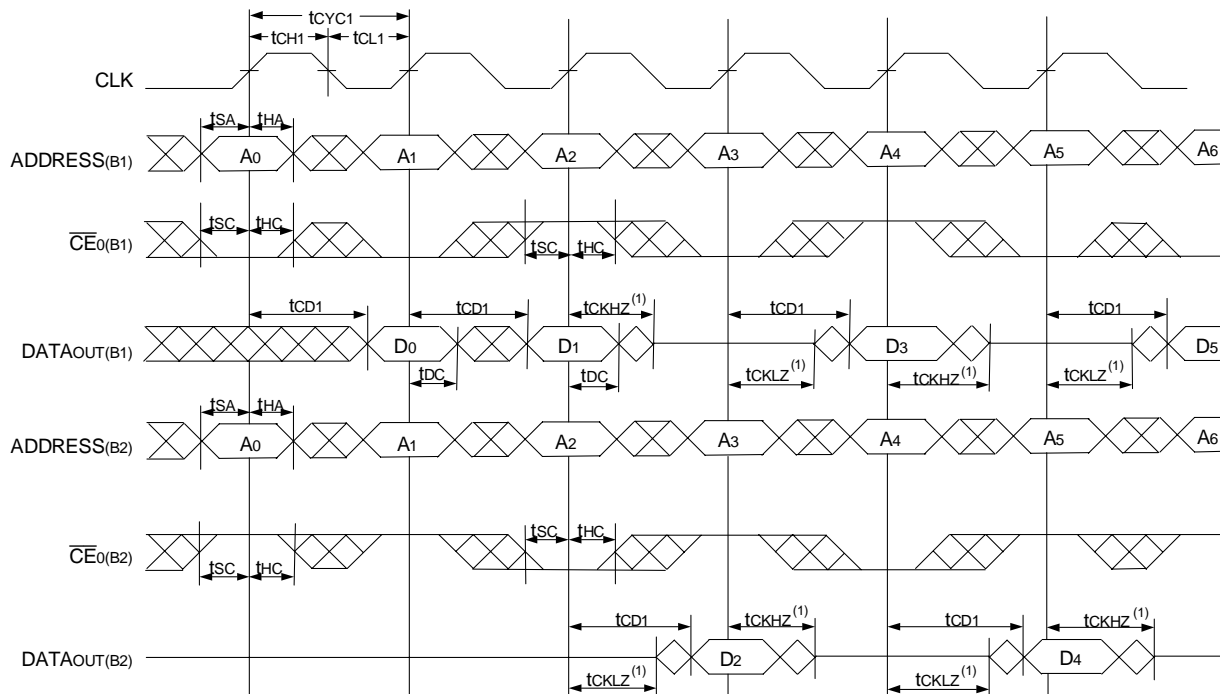
1. \overline{OE} is asynchronously controlled; all other inputs are synchronous to the rising clock edge.
2. $\overline{ADS} = V_{IL}$, \overline{CNTEN} and $\overline{REPEAT} = V_{IH}$.
3. The output is disabled (High-Impedance state) by $\overline{CE}0 = V_{IH}$, $\overline{CE}1 = V_{IL}$, \overline{UB} , $\overline{LB} = V_{IH}$ following the next rising edge of the clock. Refer to Truth Table 1.
4. Addresses do not have to be accessed sequentially since $\overline{ADS} = V_{IL}$ constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. If \overline{UB} , \overline{LB} was HIGH, then the appropriate Byte of DATAout for $Q_n + 2$ would be disabled (High-Impedance state).
6. "x" denotes Left or Right port. The diagram is with respect to that port.

Timing Waveform of a Multi-Device Pipelined Read^(1,2)



5623 drw 08

Timing Waveform of a Multi-Device Flow-Through Read^(1,2)

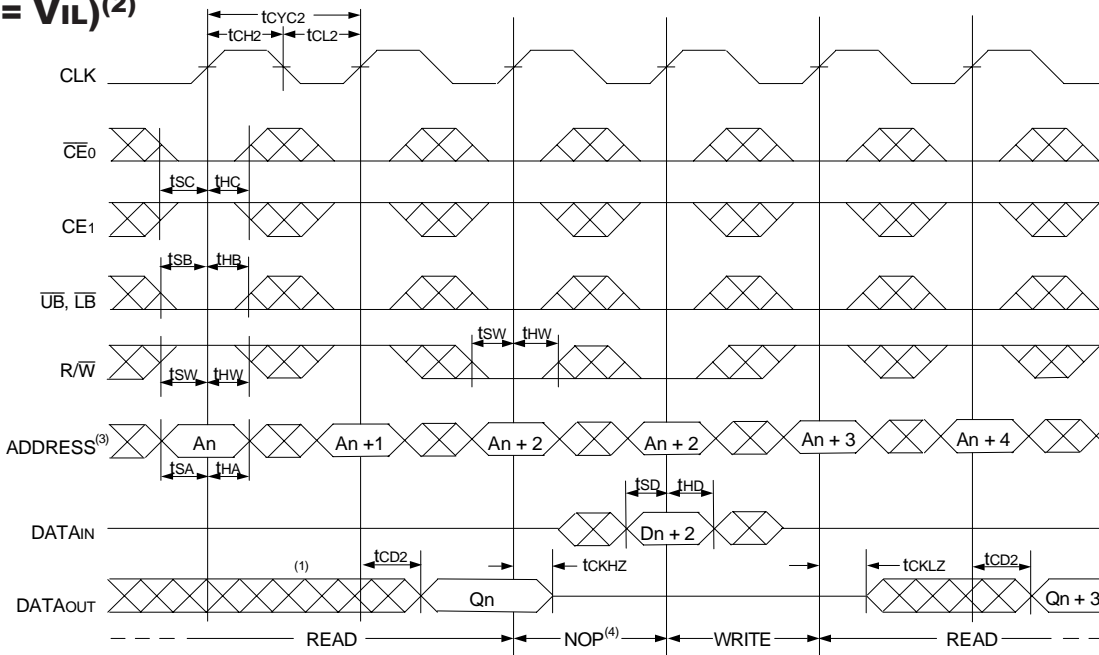


5623 drw 09

NOTES:

1. B1 Represents Device #1; B2 Represents Device #2. Each Device consists of one IDT70V3319/99 for this waveform, and are setup for depth expansion in this example. ADDRESS(B1) = ADDRESS(B2) in this situation.
2. UB, LB, OE, and ADS = VIL; CE1(B1), CE1(B2), R/W, CNTEN, and REPEAT = VIH.

Timing Waveform of Pipelined Read-to-Write-to-Read ($\overline{OE} = V_{IL}$)⁽²⁾

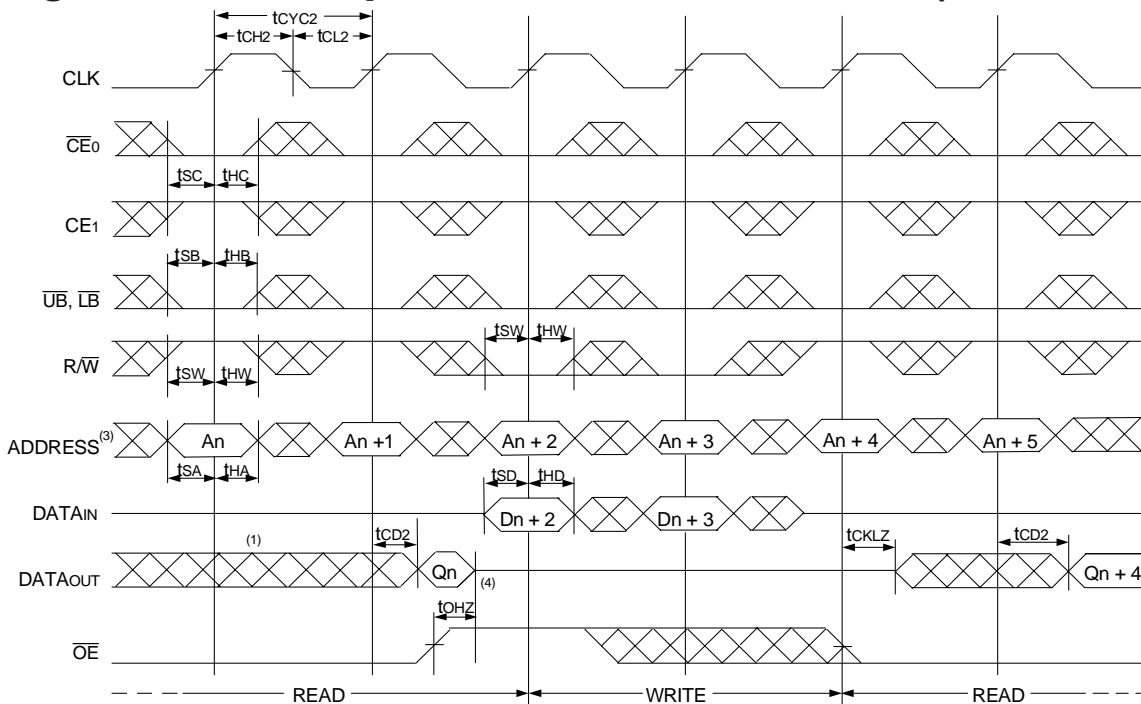


NOTES:

1. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
2. \overline{CE}_0 , \overline{UB} , \overline{LB} , and $\overline{ADS} = V_{IL}$; CE_1 , \overline{CNTEN} , and $\overline{REPEAT} = V_{IH}$. "NOP" is "No Operation".
3. Addresses do not have to be accessed sequentially since $\overline{ADS} = V_{IL}$ constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
4. "NOP" is "No Operation." Data in memory at the selected address may be corrupted and should be re-written to guarantee data integrity.

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Timing Waveform of Pipelined Read-to-Write-to-Read (\overline{OE} Controlled)⁽²⁾

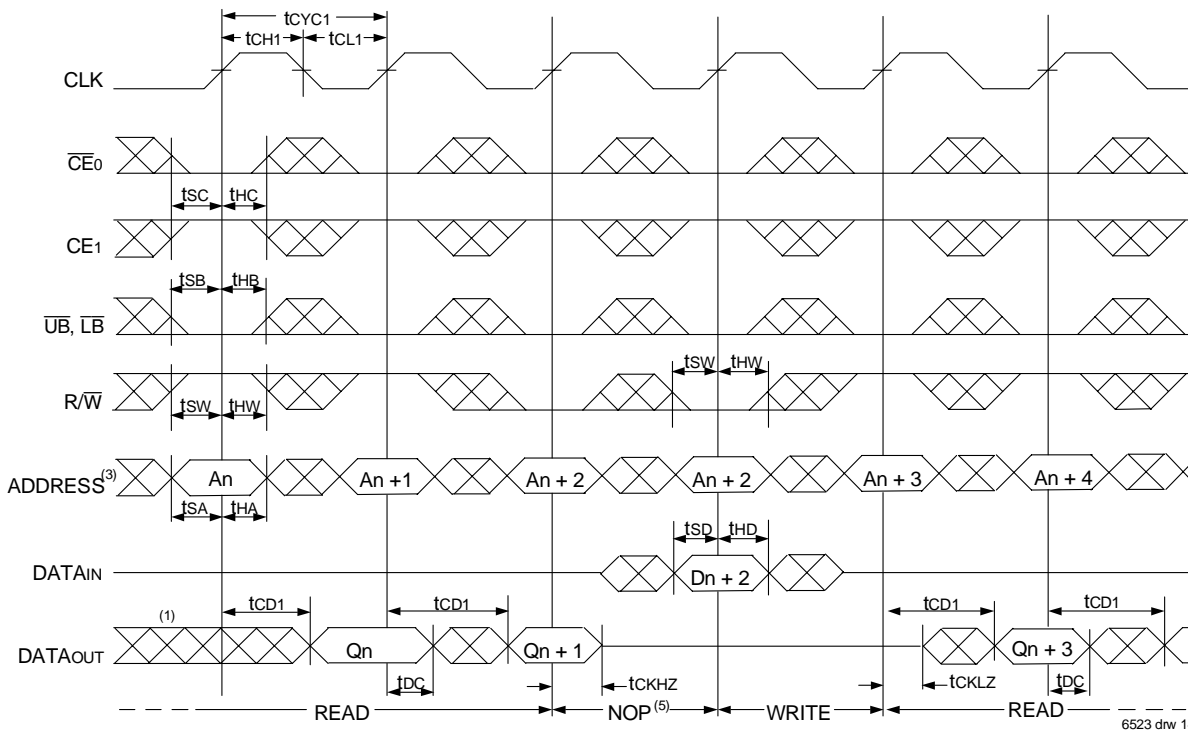


NOTES:

1. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
2. \overline{CE}_0 , \overline{UB} , \overline{LB} , and $\overline{ADS} = V_{IL}$; CE_1 , \overline{CNTEN} , and $\overline{REPEAT} = V_{IH}$.
3. Addresses do not have to be accessed sequentially since $\overline{ADS} = V_{IL}$ constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
4. This timing does not meet requirements for fastest speed grade. This waveform indicates how logically it could be done if timing so allows.

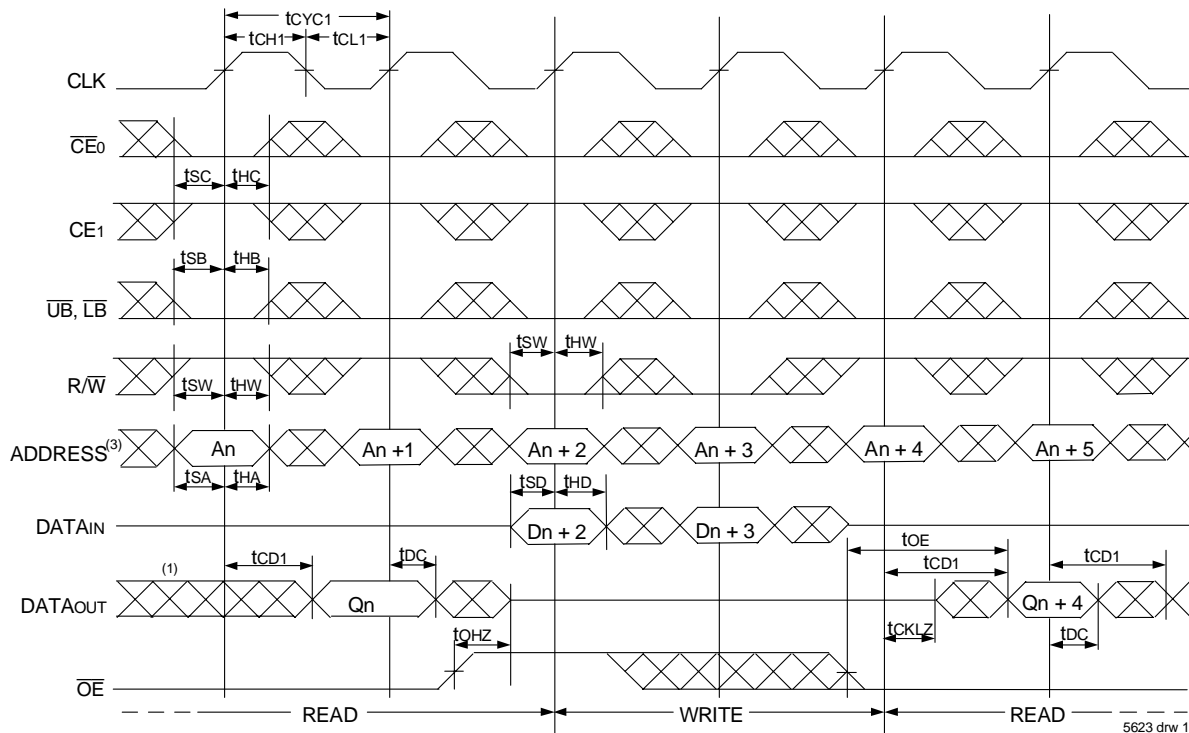
5623 drw 13

Timing Waveform of Flow-Through Read-to-Write-to-Read ($\overline{OE} = V_{IL}$)⁽²⁾



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Timing Waveform of Flow-Through Read-to-Write-to-Read (\overline{OE} Controlled)⁽²⁾

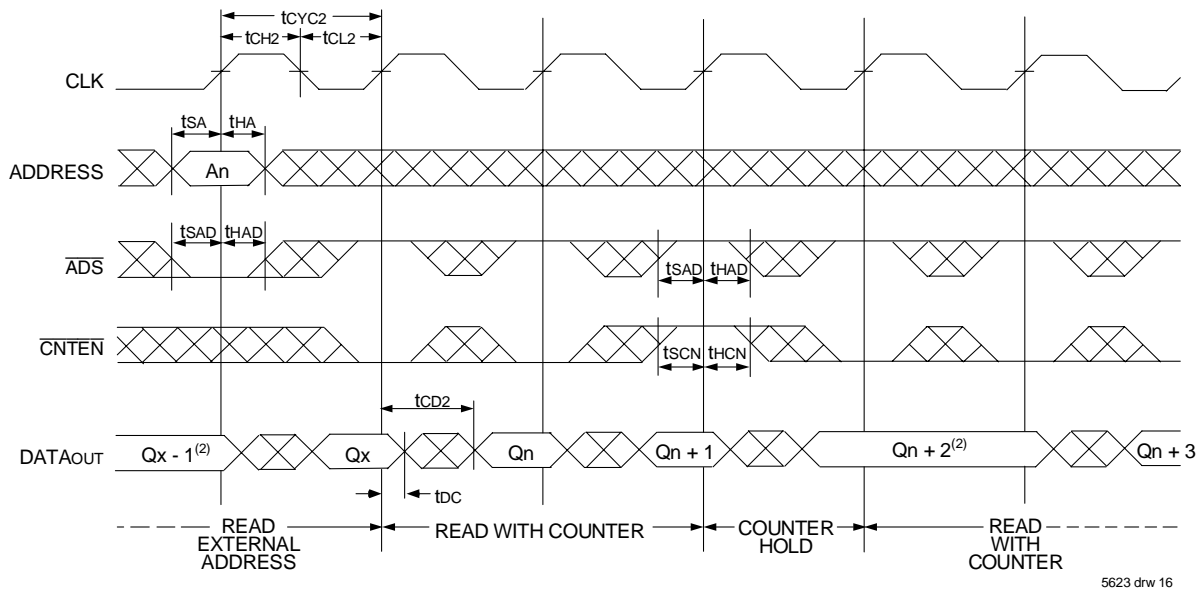


5623 drw 15

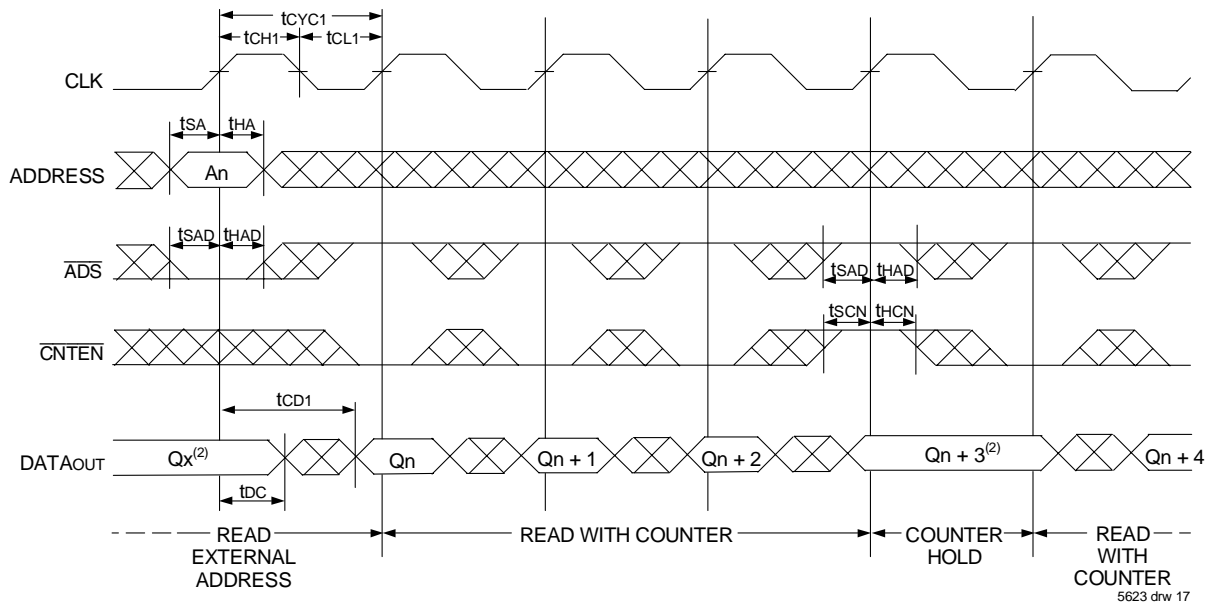
NOTES:

1. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
2. $\overline{CE0}$, \overline{UB} , \overline{LB} , and $\overline{ADS} = V_{IL}$; $\overline{CE1}$, \overline{CNTEN} , and $\overline{REPEAT} = V_{IH}$.
3. Addresses do not have to be accessed sequentially since $\overline{ADS} = V_{IL}$ constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
4. "NOP" is "No Operation." Data in memory at the selected address may be corrupted and should be re-written to guarantee data integrity.

Timing Waveform of Pipelined Read with Address Counter Advance⁽¹⁾



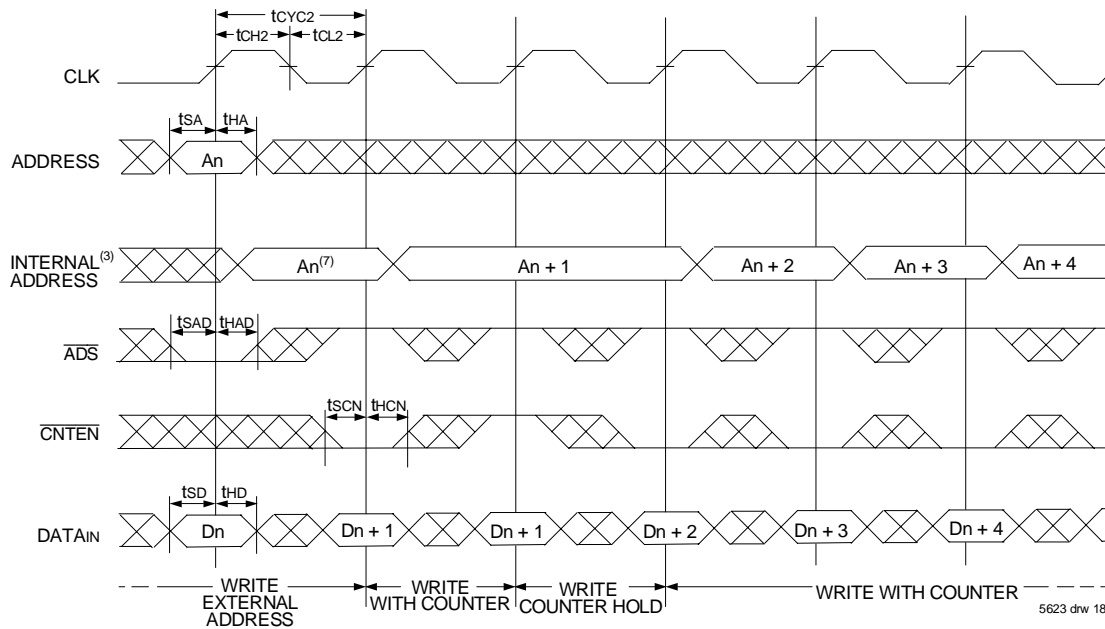
Timing Waveform of Flow-Through Read with Address Counter Advance⁽¹⁾



NOTES:

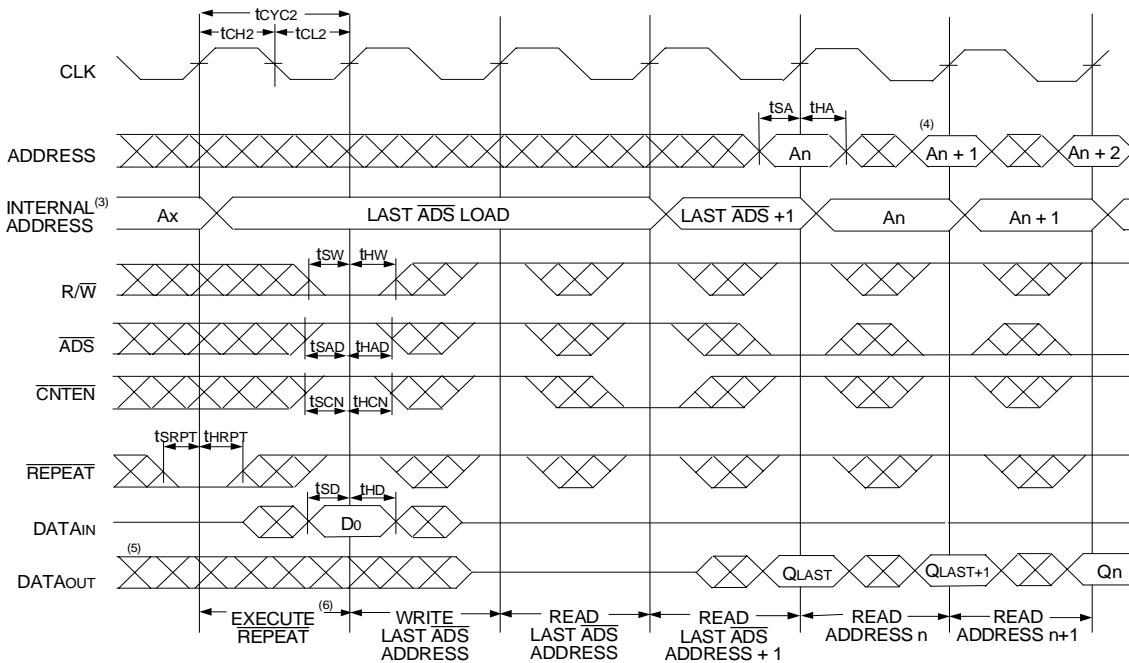
1. $\overline{CE}_0, \overline{OE}, \overline{UB}, \overline{LB} = V_{IL}$; $\overline{CE}_1, R/\overline{W}$, and $\overline{REPEAT} = V_{IH}$.
2. If there is no address change via $\overline{ADS} = V_{IL}$ (loading a new address) or $\overline{CNTEN} = V_{IL}$ (advancing the address), i.e. $\overline{ADS} = V_{IH}$ and $\overline{CNTEN} = V_{IH}$, then the data output remains constant for subsequent clocks.

Timing Waveform of Write with Address Counter Advance (Flow-through or Pipelined Inputs)⁽¹⁾



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Timing Waveform of Counter Repeat⁽²⁾



5623 drw 19

NOTES:

1. $\overline{CE_0}$, \overline{UB} , \overline{LB} , and $R/\overline{W} = V_{IL}$; CE_1 and $\overline{REPEAT} = V_{IH}$.
2. $\overline{CE_0}$, \overline{UB} , $\overline{LB} = V_{IL}$; $CE_1 = V_{IH}$.
3. The "Internal Address" is equal to the "External Address" when $\overline{ADS} = V_{IL}$ and equals the counter output when $\overline{ADS} = V_{IH}$.
4. Addresses do not have to be accessed sequentially since $\overline{ADS} = V_{IL}$ constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
6. No dead cycle exists during \overline{REPEAT} operation. A READ or WRITE cycle may be coincidental with the counter \overline{REPEAT} cycle: Address loaded by last valid \overline{ADS} load will be accessed. Extra cycles are shown here simply for clarification. For more information on \overline{REPEAT} function refer to Truth Table II.
7. $\overline{CNTEN} = V_{IL}$ advances Internal Address from 'An' to 'An +1'. The transition shown indicates the time required for the counter to advance. The 'An +1' Address is written to during this cycle.

Functional Description

The IDT70V3319/99 provides a true synchronous Dual-Port Static RAM interface. Registered inputs provide minimal set-up and hold times on address, data, and all critical control inputs. All internal registers are clocked on the rising edge of the clock signal, however, the self-timed internal write pulse is independent of the LOW to HIGH transition of the clock signal.

An asynchronous output enable is provided to ease asynchronous bus interfacing. Counter enable inputs are also provided to stall the operation of the address counters for fast interleaved memory applications.

A HIGH on $\overline{CE_0}$ or a LOW on CE_1 for one clock cycle will power down the internal circuitry to reduce static power consumption. Multiple chip enables allow easier banking of multiple IDT70V3319/99s for depth expansion configurations. Two cycles are required with $\overline{CE_0}$ LOW and CE_1 HIGH to re-activate the outputs.

Depth and Width Expansion

The IDT70V3319/99 features dual chip enables (refer to Truth Table I) in order to facilitate rapid and simple depth expansion with no requirements for external logic. Figure 4 illustrates how to control the various chip enables in order to expand two devices in depth.

The IDT70V3319/99 can also be used in applications requiring expanded width, as indicated in Figure 4. Through combining the control signals, the devices can be grouped as necessary to accommodate applications needing 36-bits or wider.

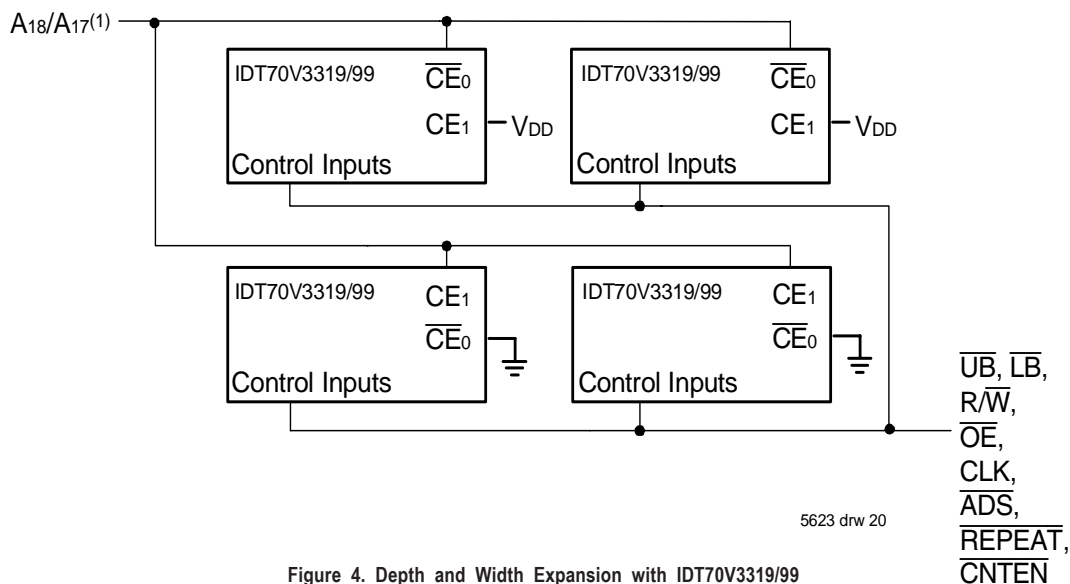
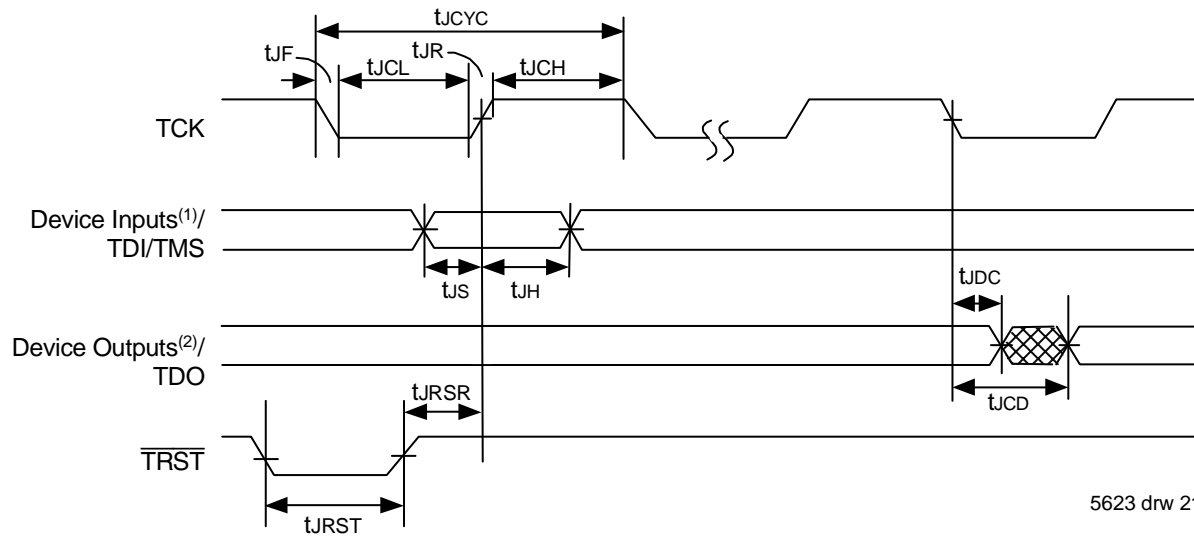


Figure 4. Depth and Width Expansion with IDT70V3319/99

NOTE:

1. A17 is for IDT70V3319, A16 is for IDT70V3399.

JTAG Timing Specifications



5623 drw 21

Figure 5. Standard JTAG Timing

NOTES:

1. Device inputs = All device inputs except TDI, TMS, and TRST.
2. Device outputs = All device outputs except TDO.

JTAG AC Electrical Characteristics^(1,2,3,4)

Symbol	Parameter	70V3319/99		
		Min.	Max.	Units
t_{JCYC}	JTAG Clock Input Period	100	—	ns
t_{JCH}	JTAG Clock HIGH	40	—	ns
t_{JCL}	JTAG Clock Low	40	—	ns
t_{JR}	JTAG Clock Rise Time	—	3 ⁽¹⁾	ns
t_{JF}	JTAG Clock Fall Time	—	3 ⁽¹⁾	ns
t_{JRST}	JTAG Reset	50	—	ns
t_{JRSR}	JTAG Reset Recovery	50	—	ns
t_{JCD}	JTAG Data Output	—	25	ns
t_{JDC}	JTAG Data Output Hold	0	—	ns
t_{JS}	JTAG Setup	15	—	ns
t_{JH}	JTAG Hold	15	—	ns

5623 tbl 12

NOTES:

1. Guaranteed by design.
2. 30pF loading on external output signals.
3. Refer to AC Electrical Test Conditions stated earlier in this document.
4. JTAG operations occur at one speed (10MHz). The base device may run at any speed specified in this datasheet.

Identification Register Definitions

Instruction Field	Value	Description
Revision Number (31:28)	0x0	Reserved for version number
IDT Device ID (27:12)	0x0314 ⁽¹⁾	Defines IDT part number
IDT JEDEC ID (11:1)	0x33	Allows unique identification of device vendor as IDT
ID Register Indicator Bit (Bit 0)	1	Indicates the presence of an ID register

5623 tbl 13

NOTE:

1. Device ID for IDT70V3399 is 0x0315.

Scan Register Sizes

Register Name	Bit Size
Instruction (IR)	4
Bypass (BYR)	1
Identification (IDR)	32
Boundary Scan (BSR)	Note (3)

5623 tbl 14

System Interface Parameters

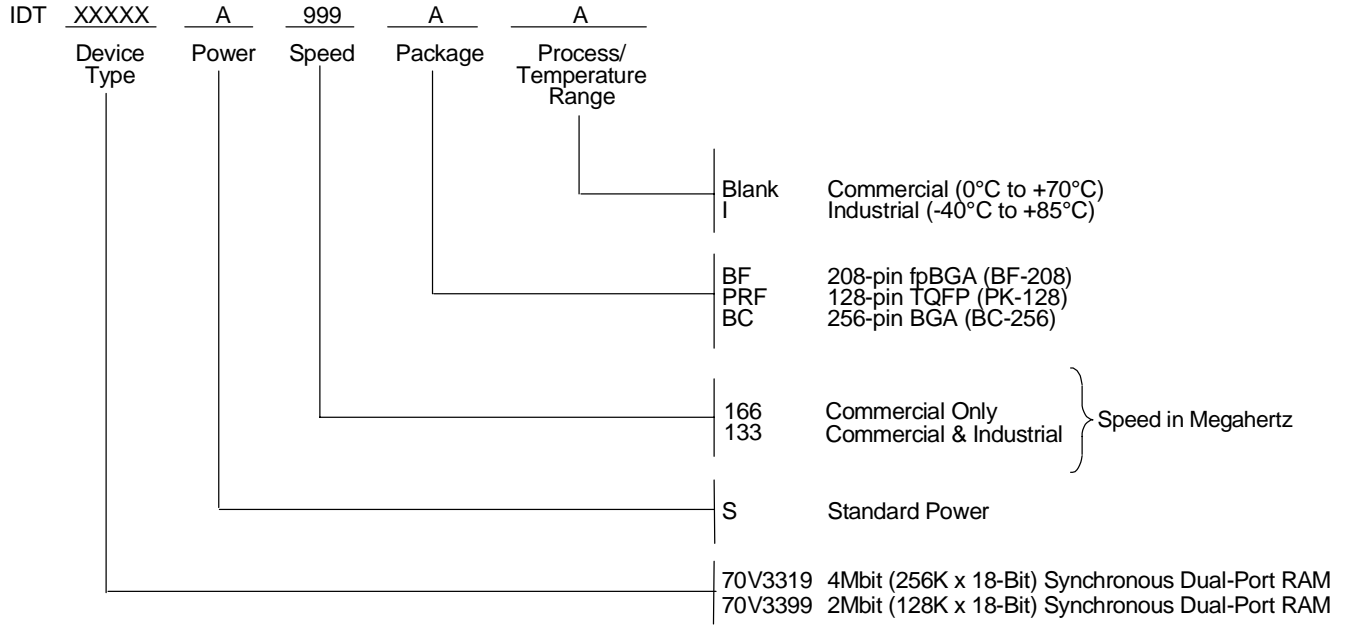
Instruction	Code	Description
EXTEST	0000	Forces contents of the boundary scan cells onto the device outputs ⁽¹⁾ . Places the boundary scan register (BSR) between TDI and TDO.
BYPASS	1111	Places the bypass register (BYR) between TDI and TDO.
IDCODE	0010	Loads the ID register (IDR) with the vendor ID code and places the register between TDI and TDO.
HIGHZ	0011	Places the bypass register (BYR) between TDI and TDO. Forces all device output drivers to a High-Z state.
SAMPLE/PRELOAD	0001	Places the boundary scan register (BSR) between TDI and TDO. SAMPLE allows data from device inputs ⁽²⁾ to be captured in the boundary scan cells and shifted serially through TDO. PRELOAD allows data to be input serially into the boundary scan cells via the TDI.
RESERVED	All other codes	Several combinations are reserved. Do not use codes other than those identified above.

5623 tbl 15

NOTES:

1. Device outputs = All device outputs except TDO.
2. Device inputs = All device inputs except TDI, TMS, and \overline{TRST} .
3. The Boundary Scan Descriptive Language (BSDL) file for this device is available on the IDT website (www.idt.com), or by contacting your local IDT sales representative.

Ordering Information



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IDT Clock Solution for IDT70V3319/99 Dual-Port

IDT Dual-Port Part Number	Dual-Port I/O Specifications		Clock Specifications				IDT PLL Clock Device
	Voltage	I/O	Input Capacitance	Input Duty Cycle Requirement	Maximum Frequency	Jitter Tolerance	
70V3319/99	3.3/2.5	LVTTL	8pF	40%	166	75ps	IDT5V2528

5623 tbl 16a

Datasheet Document History:

06/02/00:	Initial Public Offering
07/12/00:	Page 1 Added mux to functional block diagram
06/20/01:	Page 1 Added JTAG information for TQFP package Page 4 Corrected TQFP package size
07/30/01:	Page 1 Added PL/ \overline{FT} option Page 20 Changed maximum value for JTAG AC Electrical Characteristics for t_{CD} from 20ns to 25ns Page 9 Added Industrial Temperature DC Parameters
11/20/01:	Page 2, 3 & 4 Added date revision for pin configurations Page 11 Changed t_{OE} value in AC Electrical Characteristics, please refer to Errata #SMEN-01-05 Page 1 & 22 Replaced TM logo with ® logo Page 10 Changed AC Test Conditions Input Rise/Fall Times
08/06/02:	Consolidated multiple devices into one datasheet Page 1 & 5 Added DCD capability for Pipelined Outputs Page 7 Clarified T_{BIAS} and added T_{JN} Page 9 Changed DC Electrical Parameters Page 11 Removed Clock Rise & Fall Time from AC Electrical Characteristics Table Removed Preliminary status
05/19/03:	Page 11 Added Byte Enable Setup Time & Byte Enable Hold Time to AC Electrical Characteristics Table Page 22 Added IDT Clock Solution Table

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