



HIGH-SPEED 3.3V 16K x 36 SYNCHRONOUS PIPELINED DUAL-PORT STATIC RAM WITH 3.3V OR 2.5V INTERFACE

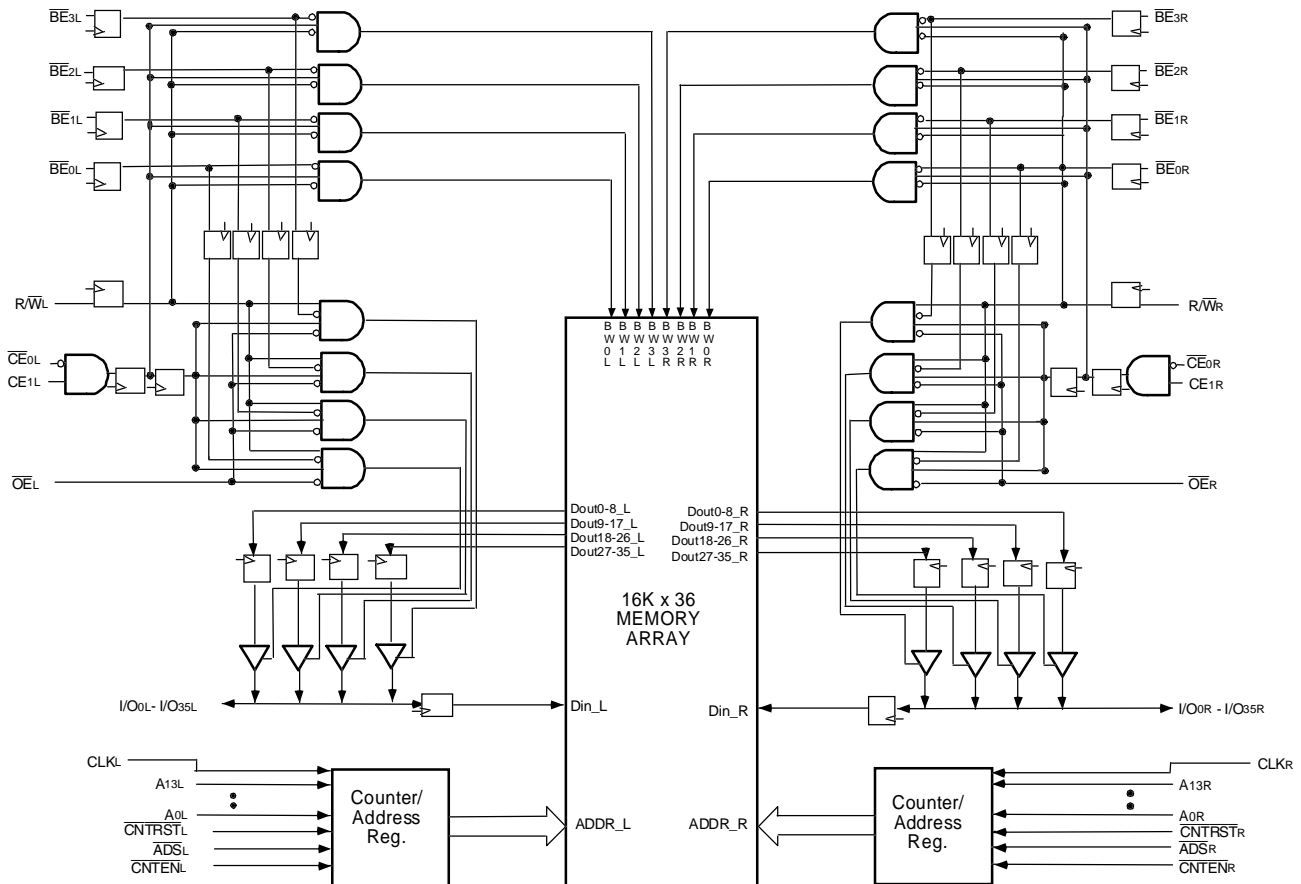
IDT70V3569S

Features:

- ◆ True Dual-Port memory cells which allow simultaneous access of the same memory location
- ◆ High-speed clock to data access
 - Commercial: 4.2/5/6ns (max.)
 - Industrial: 5/6ns (max)
- ◆ Pipelined output mode
- ◆ Counter enable and reset features
- ◆ Dual chip enables allow for depth expansion without additional logic
- ◆ Full synchronous operation on both ports
 - 7.5ns cycle time, 133MHz operation (9.6 Gbps bandwidth)
 - Fast 4.2ns clock to data out
 - 1.8ns setup to clock and 0.7ns hold on all control, data, and

- address inputs @ 133MHz
 - Data input, address, byte enable and control registers
 - Self-timed write allows fast cycle time
- ◆ Separate byte controls for multiplexed bus and bus matching compatibility
- ◆ LVTTTL-compatible, single 3.3V ($\pm 150\text{mV}$) power supply for core
- ◆ LVTTTL-compatible, selectable 3.3V ($\pm 150\text{mV}$)/2.5V ($\pm 125\text{mV}$) power supply for I/Os and control signals on each port
- ◆ Industrial temperature range (-40°C to +85°C) is available for selected speeds
- ◆ Available in a 208-pin Plastic Quad Flatpack (PQFP), 208-ball fine-pitch Ball Grid Array, and 256-pin Ball Grid Array

Functional Block Diagram



4831 tbi 01

APRIL 2001

Description:

The IDT70V3569 is a high-speed 16K x 36 bit synchronous Dual-Port RAM. The memory array utilizes Dual-Port memory cells to allow simultaneous access of any address from both ports. Registers on control, data, and address inputs provide minimal setup and hold times. The timing latitude provided by this approach allows systems to be designed with very short cycle times. With an input data register, the IDT70V3569 has been optimized for applications having unidirectional or bidirectional data flow

in bursts. An automatic power down feature, controlled by $\overline{CE0}$ and $CE1$, permits the on-chip circuitry of each port to enter a very low standby power mode.

The 70V3569 can support an operating voltage of either 3.3V or 2.5V on one or both ports, controllable by the OPT pins. The power supply for the core of the device (VDD) remains at 3.3V.

Pin Configuration(1,2,3,4)

| | | | | | | | | | | | | | | | | |
|-------------|-------------|-------------|-------------|---|--------------|-------------|-------------------------|-------------------------|-------------------------|-----------------------------|----------------------------|------------|--------------|--------------|--------------|--------------|
| A1 IO19L | A2 IO18L | A3 VSS | A4 NC | A5 NC | A6 NC | A7 A12L | A8 A8L | A9 $\overline{BE1L}$ | A10 VDD | A11 CLKL | A12 \overline{CNTENL} | A13 A4L | A14 A0L | A15 OPTL | A16 IO17L | A17 VSS |
| B1 IO20R | B2 VSS | B3 IO18R | B4 VSS | B5 NC | B6 A13L | B7 A9L | B8 $\overline{BE2L}$ | B9 $\overline{CE0L}$ | B10 VSS | B11 \overline{ADSL} | B12 A5L | B13 A1L | B14 VSS | B15 VDDQR | B16 IO16L | B17 IO15R |
| C1 VDDQL | C2 IO19R | C3 VDDQR | C4 VDD | C5 NC | C6 NC | C7 A10L | C8 $\overline{BE3L}$ | C9 CE1L | C10 VSS | C11 R/WL | C12 A6L | C13 A2L | C14 VDD | C15 IO16R | C16 IO15L | C17 VSS |
| D1 IO22L | D2 VSS | D3 IO21L | D4 IO20L | D5 NC | D6 A11L | D7 A7L | D8 $\overline{BE0L}$ | D9 VDD | D10 \overline{OEL} | D11 $\overline{CNTRSTL}$ | D12 A3L | D13 VDD | D14 IO17R | D15 VDDQL | D16 IO14L | D17 IO14R |
| E1 IO23L | E2 IO22R | E3 VDDQR | E4 IO21R | <p style="text-align: center;">70V3569BF BF-208⁽⁵⁾</p> <p style="text-align: center;">208-Pin fpBGA Top View⁽⁶⁾</p> | | | | | | | | | E14 IO12L | E15 IO13R | E16 VSS | E17 IO13L |
| F1 VDDQL | F2 IO23R | F3 IO24L | F4 VSS | | | | | | | | | | F14 VSS | F15 IO12R | F16 IO11L | F17 VDDQR |
| G1 IO26L | G2 VSS | G3 IO25L | G4 IO24R | | | | | | | | | | G14 IO9L | G15 VDDQL | G16 IO10L | G17 IO11R |
| H1 VDD | H2 IO26R | H3 VDDQR | H4 IO25R | | | | | | | | | | H14 VDD | H15 IO9R | H16 VSS | H17 IO10R |
| J1 VDDQL | J2 VDD | J3 VSS | J4 VSS | | | | | | | | | | J14 VSS | J15 VDD | J16 VSS | J17 VDDQR |
| K1 IO28R | K2 VSS | K3 IO27R | K4 VSS | | | | | | | | | | K14 IO7R | K15 VDDQL | K16 IO8R | K17 VSS |
| L1 IO29R | L2 IO28L | L3 VDDQR | L4 IO27L | | | | | | | | | | L14 IO6R | L15 IO7L | L16 VSS | L17 IO8L |
| M1 VDDQL | M2 IO29L | M3 IO30R | M4 VSS | | | | | | | | | | M14 VSS | M15 IO6L | M16 IO5R | M17 VDDQR |
| N1 IO31L | N2 VSS | N3 IO31R | N4 IO30L | N14 IO3R | N15 VDDQL | N16 IO4R | N17 IO5L | | | | | | | | | |
| P1 IO32R | P2 IO32L | P3 VDDQR | P4 IO35R | P5 NC | P6 NC | P7 A12R | P8 A8R | P9 $\overline{BE1R}$ | P10 VDD | P11 CLKR | P12 \overline{CNTENR} | P13 A4R | P14 IO2L | P15 IO3L | P16 VSS | P17 IO4L |
| R1 VSS | R2 IO33L | R3 IO34R | R4 NC | R5 NC | R6 A13R | R7 A9R | R8 $\overline{BE2R}$ | R9 $\overline{CE0R}$ | R10 VSS | R11 \overline{ADSR} | R12 A5R | R13 A1R | R14 VSS | R15 VDDQL | R16 IO1R | R17 VDDQR |
| T1 IO33R | T2 IO34L | T3 VDDQL | T4 VSS | T5 NC | T6 NC | T7 A10R | T8 $\overline{BE3R}$ | T9 CE1R | T10 VSS | T11 R/WR | T12 A6R | T13 A2R | T14 VSS | T15 IO0R | T16 VSS | T17 IO2R |
| U1 VSS | U2 IO35L | U3 VDD | U4 NC | U5 NC | U6 A11R | U7 A7R | U8 $\overline{BE0R}$ | U9 VDD | U10 \overline{OER} | U11 $\overline{CNTRSTR}$ | U12 A3R | U13 A0R | U14 VDD | U15 OPTR | U16 IO0L | U17 IO1L |

NOTES:

1. All VDD pins must be connected to 3.3V power supply.
2. All VDDQ pins must be connected to appropriate power supply: 3.3V if OPT pin for that port is set to VIH (3.3V), and 2.5V if OPT pin for that port is set to VIL (0V).
3. All VSS pins must be connected to ground supply.
4. Package body is approximately 15mm x 15mm x 1.4mm, with 0.8mm ball pitch.
5. This package code is used to reference the package diagram.
6. This text does not indicate orientation of the actual part-marking.

4831 drw 02c

Pin Configuration^(1,2,3,4) (con't.)

70V3569BC
BC-256⁽⁵⁾

256-Pin BGA
Top View⁽⁶⁾

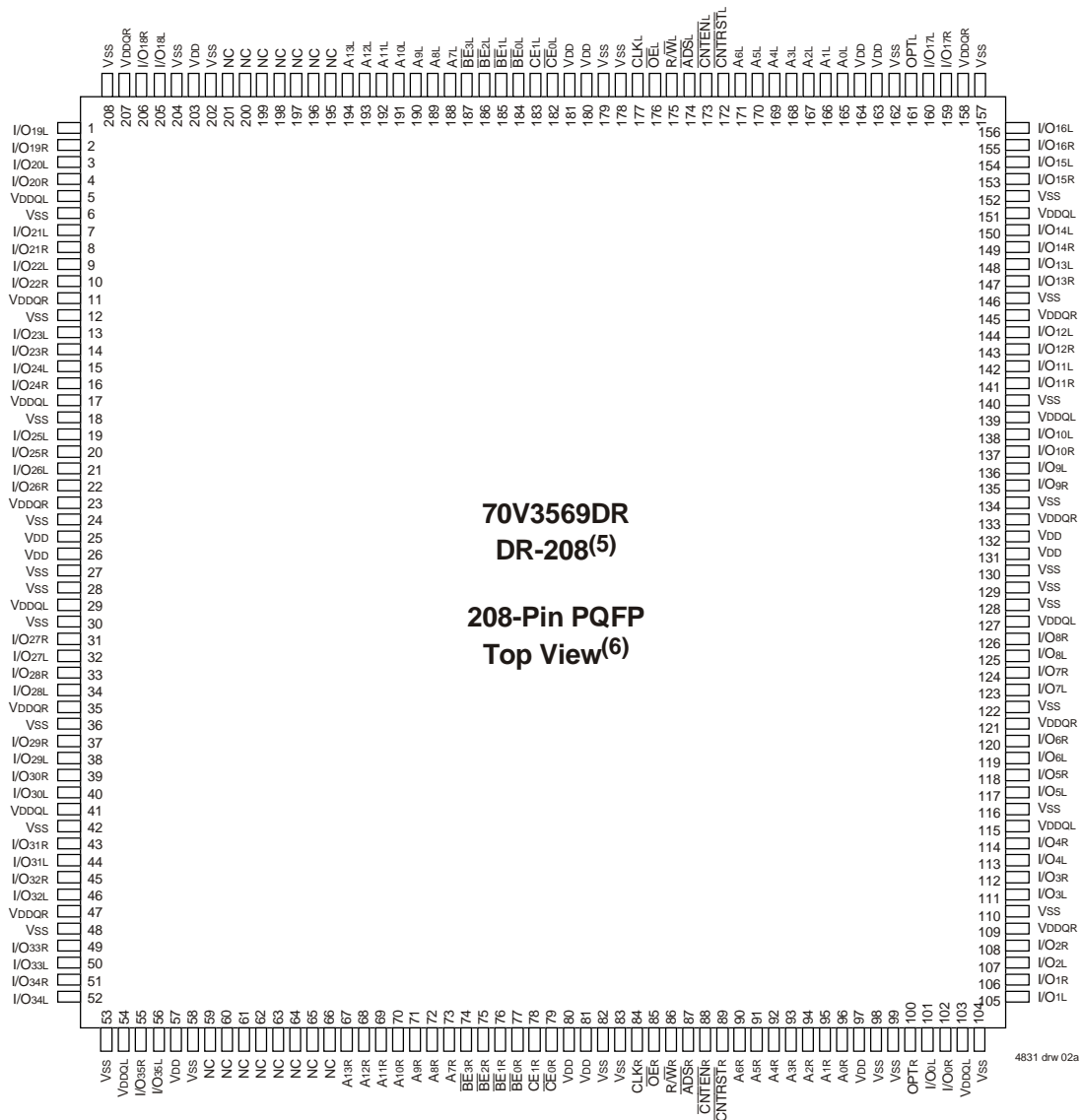
| | | | | | | | | | | | | | | | |
|--------------|--------------|--------------|-------------|-------------|-------------|-------------|-------------------------|-------------------------|-------------------------|-----------------------------|--------------|--------------|---------------|---------------|---------------|
| A1 NC | A2 NC | A3 NC | A4 NC | A5 NC | A6 A11L | A7 A8L | A8 $\overline{BE}2L$ | A9 CE1L | A10 $\overline{OE}L$ | A11 $\overline{CNTEN}L$ | A12 A5L | A13 A2L | A14 A0L | A15 NC | A16 NC |
| B1 I/O18L | B2 NC | B3 NC | B4 NC | B5 NC | B6 A12L | B7 A9L | B8 $\overline{BE}3L$ | B9 $\overline{CE}0L$ | B10 R/WL | B11 $\overline{CNTRST}L$ | B12 A4L | B13 A1L | B14 VDD | B15 I/O17L | B16 NC |
| C1 I/O18R | C2 I/O19L | C3 VSS | C4 NC | C5 A13L | C6 A10L | C7 A7L | C8 $\overline{BE}1L$ | C9 $\overline{BE}0L$ | C10 CLKL | C11 $\overline{ADS}L$ | C12 A6L | C13 A3L | C14 OPTL | C15 I/O17R | C16 I/O16L |
| D1 I/O20R | D2 I/O19R | D3 I/O20L | D4 VDD | D5 VDDQL | D6 VDDQL | D7 VDDQR | D8 VDDQR | D9 VDDQL | D10 VDDQL | D11 VDDQR | D12 VDDQR | D13 VDD | D14 I/O15R | D15 I/O15L | D16 I/O16R |
| E1 I/O21R | E2 I/O21L | E3 I/O22L | E4 VDDQL | E5 VDD | E6 VDD | E7 VSS | E8 VSS | E9 VSS | E10 VSS | E11 VDD | E12 VDD | E13 VDDQR | E14 I/O13L | E15 I/O14L | E16 I/O14R |
| F1 I/O23L | F2 I/O22R | F3 I/O23R | F4 VDDQL | F5 VDD | F6 VSS | F7 VSS | F8 VSS | F9 VSS | F10 VSS | F11 VSS | F12 VDD | F13 VDDQR | F14 I/O12R | F15 I/O13R | F16 I/O12L |
| G1 I/O24R | G2 I/O24L | G3 I/O25L | G4 VDDQR | G5 VSS | G6 VSS | G7 VSS | G8 VSS | G9 VSS | G10 VSS | G11 VSS | G12 VSS | G13 VDDQL | G14 I/O10L | G15 I/O11L | G16 I/O11R |
| H1 I/O26L | H2 I/O25R | H3 I/O26R | H4 VDDQR | H5 VSS | H6 VSS | H7 VSS | H8 VSS | H9 VSS | H10 VSS | H11 VSS | H12 VSS | H13 VDDQL | H14 I/O9R | H15 I/O9L | H16 I/O10R |
| J1 I/O27L | J2 I/O28R | J3 I/O27R | J4 VDDQL | J5 VSS | J6 VSS | J7 VSS | J8 VSS | J9 VSS | J10 VSS | J11 VSS | J12 VSS | J13 VDDQR | J14 I/O8R | J15 I/O7R | J16 I/O8L |
| K1 I/O29R | K2 I/O29L | K3 I/O28L | K4 VDDQL | K5 VSS | K6 VSS | K7 VSS | K8 VSS | K9 VSS | K10 VSS | K11 VSS | K12 VSS | K13 VDDQR | K14 I/O6R | K15 I/O6L | K16 I/O7L |
| L1 I/O30L | L2 I/O31R | L3 I/O30R | L4 VDDQR | L5 VDD | L6 VSS | L7 VSS | L8 VSS | L9 VSS | L10 VSS | L11 VSS | L12 VDD | L13 VDDQL | L14 I/O5L | L15 I/O4R | L16 I/O5R |
| M1 I/O32R | M2 I/O32L | M3 I/O31L | M4 VDDQR | M5 VDD | M6 VDD | M7 VSS | M8 VSS | M9 VSS | M10 VSS | M11 VDD | M12 VDD | M13 VDDQL | M14 I/O3R | M15 I/O3L | M16 I/O4L |
| N1 I/O33L | N2 I/O34R | N3 I/O33R | N4 VDD | N5 VDDQR | N6 VDDQR | N7 VDDQL | N8 VDDQL | N9 VDDQR | N10 VDDQL | N11 VDDQL | N12 VDDQL | N13 VDD | N14 I/O2L | N15 I/O1R | N16 I/O2R |
| P1 I/O35R | P2 I/O34L | P3 NC | P4 NC | P5 A13R | P6 A10R | P7 A7R | P8 $\overline{BE}1R$ | P9 $\overline{BE}0R$ | P10 CLKR | P11 $\overline{ADS}R$ | P12 A6R | P13 A3R | P14 I/O0L | P15 I/O0R | P16 I/O1L |
| R1 I/O35L | R2 NC | R3 NC | R4 NC | R5 NC | R6 A12R | R7 A9R | R8 $\overline{BE}3R$ | R9 $\overline{CE}0R$ | R10 R/WR | R11 $\overline{CNTRST}R$ | R12 A4R | R13 A1R | R14 OPTR | R15 NC | R16 NC |
| T1 NC | T2 NC | T3 NC | T4 NC | T5 NC | T6 A11R | T7 A8R | T8 $\overline{BE}2R$ | T9 CE1R | T10 $\overline{OE}R$ | T11 $\overline{CNTEN}R$ | T12 A5R | T13 A2R | T14 A0R | T15 NC | T16 NC |

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NOTES:

1. All VDD pins must be connected to 3.3V power supply.
2. All VDDQ pins must be connected to appropriate power supply: 3.3V if OPT pin for that port is set to VIH (3.3V), and 2.5V if OPT pin for that port is set to VIL (0V).
3. All VSS pins must be connected to ground supply.
4. Package body is approximately 17mm x 17mm x 1.4mm, with 1.0mm ball-pitch.
5. This package code is used to reference the package diagram.
6. This text does not indicate orientation of the actual part-marking.

Pin Configuration^(1,2,3,4) (con't.)



**70V3569DR
DR-208(5)
208-Pin PQFP
Top View⁽⁶⁾**

4831 drw 02a

NOTES:

1. All VDD pins must be connected to 3.3V power supply.
2. All VDDQ pins must be connected to appropriate power supply: 3.3V if OPT pin for that port is set to VIH (3.3V), and 2.5V if OPT pin for that port is set to VIL (0V).
3. All VSS pins must be connected to ground supply.
4. Package body is approximately 28mm x 28mm x 3.5mm.
5. This package code is used to reference the package diagram.
6. This text does not indicate orientation of the actual part-marking.

Pin Names

| Left Port | Right Port | Names |
|---|---|---|
| \overline{CE}_{0L} , CE1L | \overline{CE}_{0R} , CE1R | Chip Enables |
| R/ \overline{W} L | R/ \overline{W} R | Read/Write Enable |
| \overline{OE} L | \overline{OE} R | Output Enable |
| A0L - A13L | A0R - A13R | Address |
| I/O0L - I/O35L | I/O0R - I/O35R | Data Input/Output |
| CLKL | CLKR | Clock |
| \overline{ADS} L | \overline{ADS} R | Address Strobe Enable |
| \overline{CNTEN} L | \overline{CNTEN} R | Counter Enable |
| \overline{CNTRST} L | \overline{CNTRST} R | Counter Reset |
| \overline{BE}_{0L} - \overline{BE}_{3L} | \overline{BE}_{0R} - \overline{BE}_{3R} | Byte Enables (9-bit bytes) |
| VDDQL | VDDQR | Power (I/O Bus) (3.3V or 2.5V) ⁽¹⁾ |
| OPTL | OPTR | Option for selection VDDOX ^(1,2) |
| VDD | | Power (3.3V) ⁽¹⁾ |
| VSS | | Ground (0V) |

4831 tbl 01

NOTES:

- VDD, OPTx, and VDDOX must be set to appropriate operating levels prior to applying inputs on the I/Os and controls for that port.
- OPTx selects the operating voltage levels for the I/Os and controls on that port. If OPTx is set to VIH (3.3V), then that port's I/Os and controls will operate at 3.3V levels and VDDOX must be supplied at 3.3V. If OPTx is set to VIL (0V), then that port's I/Os and controls will operate at 2.5V levels and VDDOX must be supplied at 2.5V. The OPT pins are independent of one another—both ports can operate at 3.3V levels, both can operate at 2.5V levels, or either can operate at 3.3V with the other at 2.5V.

Truth Table I—Read/Write and Enable Control^(1,2,3,4)

| OE | CLK | \overline{CE}_0 | CE1 | \overline{BE}_3 | \overline{BE}_2 | \overline{BE}_1 | \overline{BE}_0 | R/ \overline{W} | Byte 3 I/O27-35 | Byte 2 I/O18-26 | Byte 1 I/O9-17 | Byte 0 I/O0-8 | MODE |
|----|-----|-------------------|-----|-------------------|-------------------|-------------------|-------------------|-------------------|--------------------|--------------------|-------------------|------------------|-----------------------------|
| X | ↑ | H | X | X | X | X | X | X | High-Z | High-Z | High-Z | High-Z | Deselected—Power Down |
| X | ↑ | X | L | X | X | X | X | X | High-Z | High-Z | High-Z | High-Z | Deselected—Power Down |
| X | ↑ | L | H | H | H | H | H | X | High-Z | High-Z | High-Z | High-Z | All Bytes Deselected |
| X | ↑ | L | H | H | H | H | L | L | High-Z | High-Z | High-Z | DIN | Write to Byte 0 Only |
| X | ↑ | L | H | H | L | H | H | L | High-Z | High-Z | DIN | High-Z | Write to Byte 1 Only |
| X | ↑ | L | H | H | L | H | H | L | High-Z | DIN | High-Z | High-Z | Write to Byte 2 Only |
| X | ↑ | L | H | L | H | H | H | L | DIN | High-Z | High-Z | High-Z | Write to Byte 3 Only |
| X | ↑ | L | H | H | H | L | L | L | High-Z | High-Z | DIN | DIN | Write to Lower 2 Bytes Only |
| X | ↑ | L | H | L | L | H | H | L | DIN | DIN | High-Z | High-Z | Write to Upper 2 bytes Only |
| X | ↑ | L | H | L | L | L | L | L | DIN | DIN | DIN | DIN | Write to All Bytes |
| L | ↑ | L | H | H | H | H | L | H | High-Z | High-Z | High-Z | DOUT | Read Byte 0 Only |
| L | ↑ | L | H | H | H | L | H | H | High-Z | High-Z | DOUT | High-Z | Read Byte 1 Only |
| L | ↑ | L | H | H | L | H | H | H | High-Z | DOUT | High-Z | High-Z | Read Byte 2 Only |
| L | ↑ | L | H | L | H | H | H | H | DOUT | High-Z | High-Z | High-Z | Read Byte 3 Only |
| L | ↑ | L | H | H | H | L | L | H | High-Z | High-Z | DOUT | DOUT | Read Lower 2 Bytes Only |
| L | ↑ | L | H | L | L | H | H | H | DOUT | DOUT | High-Z | High-Z | Read Upper 2 Bytes Only |
| L | ↑ | L | H | L | L | L | L | H | DOUT | DOUT | DOUT | DOUT | Read All Bytes |
| H | ↑ | L | H | L | L | L | L | X | High-Z | High-Z | High-Z | High-Z | Outputs Disabled |

NOTES:

- "H" = VIH, "L" = VIL, "X" = Don't Care.
- \overline{ADS} , \overline{CNTEN} , \overline{CNTRST} = VIH.
- OE is an asynchronous input signal.
- It is possible to read or write any combination of bytes during a given access. A few representative samples have been illustrated here.

4831 tbl 02

Truth Table II—Address Counter Control^(1,2)

| Address | Previous Address | Addr Used | CLK ⁽⁶⁾ | $\overline{\text{ADS}}$ | $\overline{\text{CNTEN}}$ | $\overline{\text{CNRST}}$ | I/O ⁽³⁾ | MODE |
|---------|------------------|-----------|--------------------|-------------------------|---------------------------|---------------------------|-----------------------|---|
| X | X | 0 | ↑ | X | X | L ⁽⁴⁾ | D _{IO} (0) | Counter Reset to Address 0 |
| An | X | An | ↑ | L ⁽⁴⁾ | X | H | D _{IO} (n) | External Address Used |
| An | Ap | Ap | ↑ | H | H | H | D _{IO} (p) | External Address Blocked—Counter disabled (Ap reused) |
| X | Ap | Ap + 1 | ↑ | H | L ⁽⁵⁾ | H | D _{IO} (p+1) | Counter Enabled—Internal Address generation |

4831 tbl 03

NOTES:

- "H" = V_{IH}, "L" = V_{IL}, "X" = Don't Care.
- Read and write operations are controlled by the appropriate setting of R $\overline{\text{W}}$, $\overline{\text{CE}}_0$, CE₁, $\overline{\text{B}}\overline{\text{E}}_n$ and $\overline{\text{O}}\overline{\text{E}}$.
- Outputs are in Pipelined mode: the data out will be delayed by one cycle.
- $\overline{\text{ADS}}$ and $\overline{\text{CNRST}}$ are independent of all other memory control signals including $\overline{\text{CE}}_0$, CE₁ and $\overline{\text{B}}\overline{\text{E}}_n$.
- The address counter advances if $\overline{\text{CNTEN}} = \text{V}_{\text{IL}}$ on the rising edge of CLK, regardless of all other memory control signals including $\overline{\text{CE}}_0$, CE₁, $\overline{\text{B}}\overline{\text{E}}_n$.

Recommended Operating Temperature and Supply Voltage^(1,2)

| Grade | Ambient Temperature | GND | V _{DD} |
|------------|---------------------|-----|-----------------|
| Commercial | 0°C to +70°C | 0V | 3.3V ± 150mV |
| Industrial | -40°C to +85°C | 0V | 3.3V ± 150mV |

4831 tbl 04

NOTES:

- Industrial temperature: for specific speeds, packages and powers contact your sales office.
- This is the parameter T_A. This is the "instant on" case temperature.

Absolute Maximum Ratings⁽¹⁾

| Symbol | Rating | Commercial & Industrial | Unit |
|----------------------------------|--------------------------------------|-------------------------|------|
| V _{TERM} ⁽²⁾ | Terminal Voltage with Respect to GND | -0.5 to +4.6 | V |
| T _{BIAS} | Temperature Under Bias | -55 to +125 | °C |
| T _{STG} | Storage Temperature | -65 to +150 | °C |
| I _{OUT} | DC Output Current | 50 | mA |

4831 tbl 05

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{TERM} must not exceed V_{DD} + 150mV for more than 25% of the cycle time or 4ns maximum, and is limited to ≤ 20mA for the period of V_{TERM} ≥ V_{DD} + 150mV.

Recommended DC Operating Conditions with V_{DDQ} at 2.5V

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|------------------|---|---------------------|------|---|------|
| V _{DD} | Core Supply Voltage | 3.15 | 3.3 | 3.45 | V |
| V _{DDQ} | I/O Supply Voltage ⁽³⁾ | 2.375 | 2.5 | 2.625 | V |
| V _{SS} | Ground | 0 | 0 | 0 | V |
| V _{IH} | Input High Voltage ⁽³⁾ (Address & Control Inputs) | 1.7 | — | V _{DDQ} + 125mV ⁽²⁾ | V |
| V _{IH} | Input High Voltage - I/O ⁽³⁾ | 1.7 | — | V _{DDQ} + 125mV ⁽²⁾ | V |
| V _{IL} | Input Low Voltage | -0.3 ⁽¹⁾ | — | 0.7 | V |

4831 tbl 05a

NOTES:

- V_{IL} ≥ -1.5V for pulse width less than 10 ns.
- V_{TERM} must not exceed V_{DDQ} + 125mV.
- To select operation at 2.5V levels on the I/Os and controls of a given port, the OPT pin for that port must be set to V_{IL} (0V), and V_{DDQX} for that port must be supplied as indicated above.

Recommended DC Operating Conditions with V_{DDQ} at 3.3V

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|------------------|---|---------------------|------|---|------|
| V _{DD} | Core Supply Voltage | 3.15 | 3.3 | 3.45 | V |
| V _{DDQ} | I/O Supply Voltage ⁽³⁾ | 3.15 | 3.3 | 3.45 | V |
| V _{SS} | Ground | 0 | 0 | 0 | V |
| V _{IH} | Input High Voltage (Address & Control Inputs) ⁽³⁾ | 2.0 | — | V _{DDQ} + 150mV ⁽²⁾ | V |
| V _{IH} | Input High Voltage - I/O ⁽³⁾ | 2.0 | — | V _{DDQ} + 150mV ⁽²⁾ | V |
| V _{IL} | Input Low Voltage | -0.3 ⁽¹⁾ | — | 0.8 | V |

4831 tbl 05b

NOTES:

- V_{IL} ≥ -1.5V for pulse width less than 10 ns.
- V_{TERM} must not exceed V_{DDQ} + 150mV.
- To select operation at 3.3V levels on the I/Os and controls of a given port, the OPT pin for that port must be set to V_{IH} (3.3V), and V_{DDQX} for that port must be supplied as indicated above.

Capacitance⁽¹⁾

(TA = +25°C, F = 1.0MHz) PQFP ONLY

| Symbol | Parameter | Conditions ⁽²⁾ | Max. | Unit |
|---------------------------------|--------------------|---------------------------|------|------|
| C _{IN} | Input Capacitance | V _{IN} = 3dV | 8 | pF |
| C _{OUT} ⁽³⁾ | Output Capacitance | V _{OUT} = 3dV | 10.5 | pF |

4831 tbl 07

NOTES:

- These parameters are determined by device characterization, but are not production tested.
- 3dV references the interpolated capacitance when the input and output switch from 0V to 3V or from 3V to 0V.
- C_{OUT} also references C_{IO}.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (V_{DD} = 3.3V ± 150mV)

| Symbol | Parameter | Test Conditions | 70V3569S | | Unit |
|------------------------|--------------------------------------|---|----------|------|------|
| | | | Min. | Max. | |
| I _L | Input Leakage Current ⁽¹⁾ | V _{DDQ} = Max., V _{IN} = 0V to V _{DDQ} | — | 10 | μA |
| I _O | Output Leakage Current | $\overline{CE_0} = V_{IH}$ or $CE_1 = V_{IL}$, V _{OUT} = 0V to V _{DDQ} | — | 10 | μA |
| V _{OL} (3.3V) | Output Low Voltage ⁽²⁾ | I _{OL} = +4mA, V _{DDQ} = Min. | — | 0.4 | V |
| V _{OH} (3.3V) | Output High Voltage ⁽²⁾ | I _{OH} = -4mA, V _{DDQ} = Min. | 2.4 | — | V |
| V _{OL} (2.5V) | Output Low Voltage ⁽²⁾ | I _{OL} = +2mA, V _{DDQ} = Min. | — | 0.4 | V |
| V _{OH} (2.5V) | Output High Voltage ⁽²⁾ | I _{OH} = -2mA, V _{DDQ} = Min. | 2.0 | — | V |

4831 tbl 08

NOTE:

- At V_{DD} ≤ -2.0V input leakages are undefined.
- V_{DDQ} is selectable (3.3V/2.5V) via OPT pins. Refer to p.4 for details.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range⁽³⁾ ($V_{DD} = 3.3V \pm 150mV$)

| Symbol | Parameter | Test Condition | Version | 70V3569S4 Com'l Only | | 70V3569S5 Com'l & Ind | | 70V3569S6 Com'l & Ind | | Unit | |
|--------|---|---|---------|-------------------------|------|-----------------------------|------|-----------------------------|------|------|----|
| | | | | Typ. ⁽⁴⁾ | Max. | Typ. ⁽⁴⁾ | Max. | Typ. ⁽⁴⁾ | Max. | | |
| IDD | Dynamic Operating Current (Both Ports Active) | \overline{CE}_L and $\overline{CE}_R = V_{IL}$, Outputs Disabled, $f = f_{MAX}^{(1)}$ | COM'L | S | 375 | 460 | 285 | 360 | 245 | 310 | mA |
| | | | IND | S | — | — | 285 | 415 | 245 | 360 | |
| ISB1 | Standby Current (Both Ports - TTL Level Inputs) | $\overline{CE}_L = \overline{CE}_R = V_{IH}$ $f = f_{MAX}^{(1)}$ | COM'L | S | 145 | 190 | 105 | 145 | 95 | 125 | mA |
| | | | IND | S | — | — | 105 | 175 | 95 | 150 | |
| ISB2 | Standby Current (One Port - TTL Level Inputs) | $\overline{CE}^*A = V_{IL}$ and $\overline{CE}^*B = V_{IH}^{(5)}$ Active Port Outputs Disabled, $f = f_{MAX}^{(1)}$ | COM'L | S | 265 | 325 | 190 | 260 | 175 | 225 | mA |
| | | | IND | S | — | — | 190 | 300 | 175 | 260 | |
| ISB3 | Full Standby Current (Both Ports - CMOS Level Inputs) | Both Ports \overline{CE}_L and $\overline{CE}_R \geq V_{DD} - 0.2V$, $V_{IN} \geq V_{DD} - 0.2V$ or $V_{IN} \leq 0.2V$, $f = 0^{(2)}$ | COM'L | S | 6 | 15 | 6 | 15 | 6 | 15 | mA |
| | | | IND | S | — | — | 6 | 30 | 6 | 30 | |
| ISB4 | Full Standby Current (One Port - CMOS Level Inputs) | $\overline{CE}^*A \leq 0.2V$ and $\overline{CE}^*B \geq V_{DD} - 0.2V^{(6)}$ $V_{IN} \geq V_{DD} - 0.2V$ or $V_{IN} \leq 0.2V$, Active Port, Outputs Disabled, $f = f_{MAX}^{(1)}$ | COM'L | S | 265 | 325 | 180 | 260 | 170 | 225 | mA |
| | | | IND | S | — | — | 180 | 300 | 170 | 260 | |

4831 tbl 09

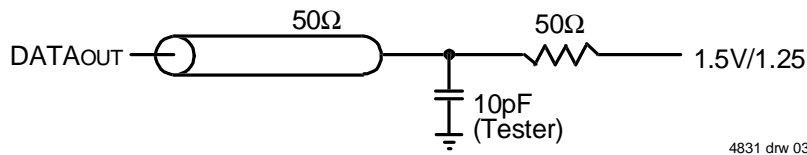
NOTES:

- At $f = f_{MAX}$, address and control lines (except Output Enable) are cycling at the maximum frequency clock cycle of $1/t_{cyc}$, using "AC TEST CONDITIONS" at input levels of GND to 3V.
- $f = 0$ means no address, clock, or control lines change. Applies only to input at CMOS level standby.
- Port "A" may be either left or right port. Port "B" is the opposite from port "A".
- $V_{DD} = 3.3V$, $T_A = 25^\circ C$ for Typ, and are not production tested. $I_{DD} \text{ dc}(f=0) = 120\text{mA}$ (Typ).
- $\overline{CE}_X = V_{IL}$ means $\overline{CE}_{0X} = V_{IL}$ and $CE_{1X} = V_{IH}$
 $\overline{CE}_X = V_{IH}$ means $\overline{CE}_{0X} = V_{IH}$ or $CE_{1X} = V_{IL}$
 $\overline{CE}_X \leq 0.2V$ means $\overline{CE}_{0X} \leq 0.2V$ and $CE_{1X} \geq V_{CC} - 0.2V$
 $\overline{CE}_X \geq V_{CC} - 0.2V$ means $\overline{CE}_{0X} \geq V_{CC} - 0.2V$ or $CE_{1X} \leq 0.2V$
 "X" represents "L" for left port or "R" for right port.

AC Test Conditions

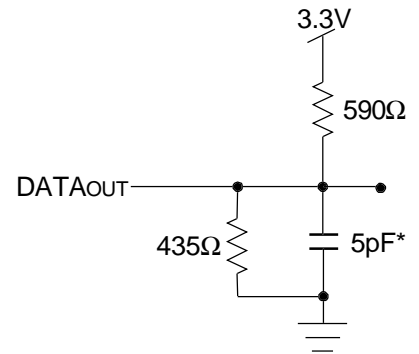
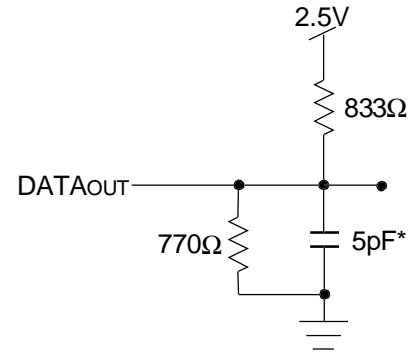
| | |
|---|--------------------------|
| Input Pulse Levels (Address & Controls) | GND to 3.0V/GND to 2.35V |
| Input Pulse Levels (I/Os) | GND to 3.0V/GND to 2.35V |
| Input Rise/Fall Times | 3ns |
| Input Timing Reference Levels | 1.5V/1.25V |
| Output Reference Levels | 1.5V/1.25V |
| Output Load | Figures 1, 2, and 3 |

4831 tbl 10



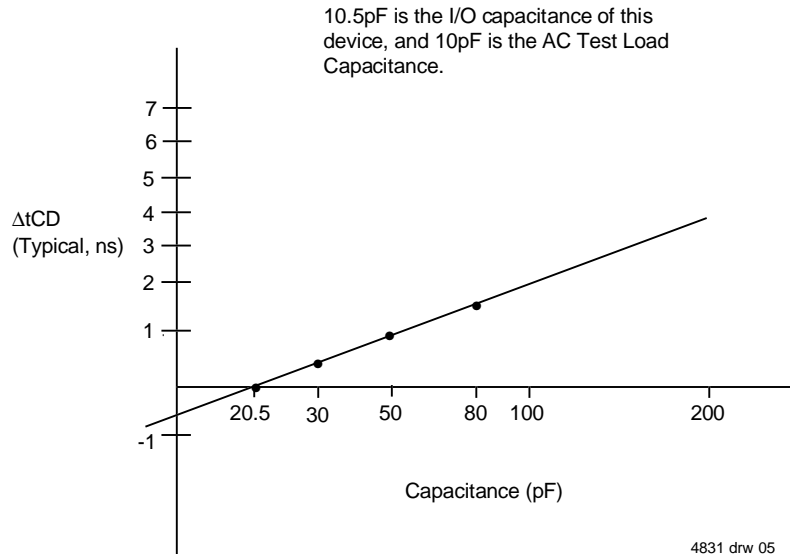
4831 drw 03

Figure 1. AC Output Test load.



4831 drw 04

Figure 2. Output Test Load
(For t_{CKLZ}, t_{CKHZ}, t_{OLZ}, and t_{OHZ}).
*Including scope and jig.



4831 drw 05

Figure 3. Typical Output Derating (Lumped Capacitive Load).

AC Electrical Characteristics Over the Operating Temperature Range (Read and Write Cycle Timing)^(1,2)

(V_{DD} = 3.3V ± 150mV, T_A = 0°C to +70°C)

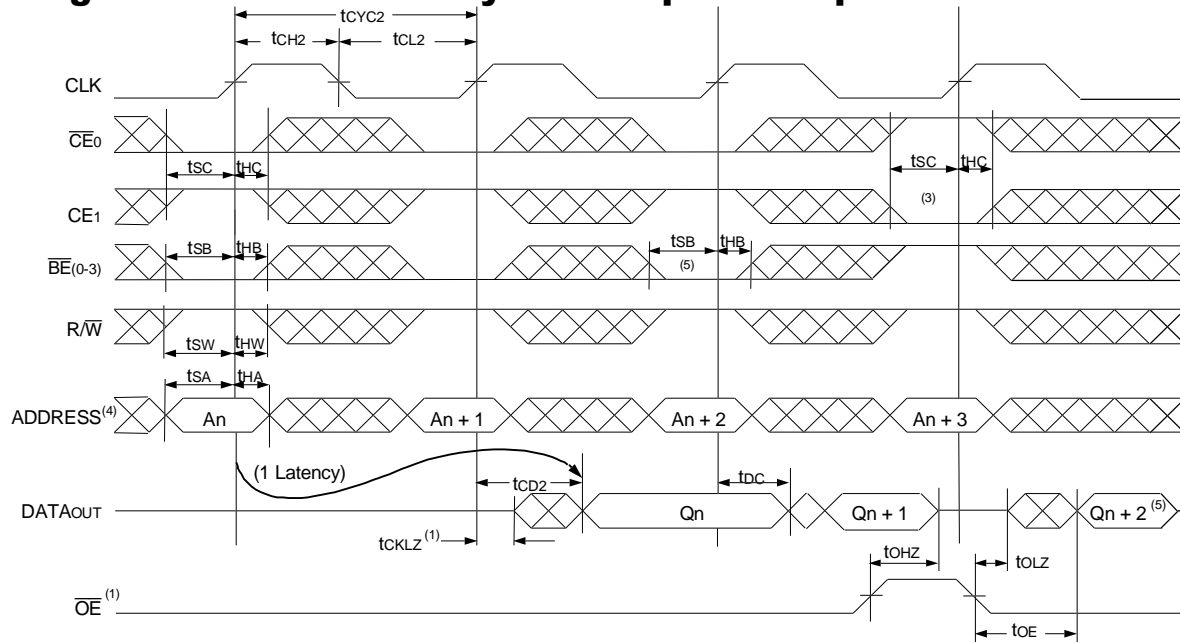
| Symbol | Parameter | 70V3569S4 Com'I Only | | 70V3569S5 Com'I & Ind | | 70V3569S6 Com'I & Ind | | Unit |
|-------------------------------|-----------------------------------|-------------------------|------|-----------------------------|------|-----------------------------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| t _{CYC2} | Clock Cycle Time (Pipelined) | 7.5 | — | 10 | — | 12 | — | ns |
| t _{CH2} | Clock High Time (Pipelined) | 3 | — | 4 | — | 5 | — | ns |
| t _{CL2} | Clock Low Time (Pipelined) | 3 | — | 4 | — | 5 | — | ns |
| t _R | Clock Rise Time | — | 3 | — | 3 | — | 3 | ns |
| t _F | Clock Fall Time | — | 3 | — | 3 | — | 3 | ns |
| t _{SA} | Address Setup Time | 1.8 | — | 2.0 | — | 2.0 | — | ns |
| t _{HA} | Address Hold Time | 0.7 | — | 0.7 | — | 1.0 | — | ns |
| t _{SC} | Chip Enable Setup Time | 1.8 | — | 2.0 | — | 2.0 | — | ns |
| t _{HC} | Chip Enable Hold Time | 0.7 | — | 0.7 | — | 1.0 | — | ns |
| t _{SB} | Byte Enable Setup Time | 1.8 | — | 2.0 | — | 2.0 | — | ns |
| t _{HB} | Byte Enable Hold Time | 0.7 | — | 0.7 | — | 1.0 | — | ns |
| t _{SW} | R/W Setup Time | 1.8 | — | 2.0 | — | 2.0 | — | ns |
| t _{HW} | R/W Hold Time | 0.7 | — | 0.7 | — | 1.0 | — | ns |
| t _{SD} | Input Data Setup Time | 1.8 | — | 2.0 | — | 2.0 | — | ns |
| t _{HD} | Input Data Hold Time | 0.7 | — | 0.7 | — | 1.0 | — | ns |
| t _{SAD} | \overline{ADS} Setup Time | 1.8 | — | 2.0 | — | 2.0 | — | ns |
| t _{HAD} | \overline{ADS} Hold Time | 0.7 | — | 0.7 | — | 1.0 | — | ns |
| t _{SCN} | \overline{CNTEN} Setup Time | 1.8 | — | 2.0 | — | 2.0 | — | ns |
| t _{HCN} | \overline{CNTEN} Hold Time | 0.7 | — | 0.7 | — | 1.0 | — | ns |
| t _{SRST} | \overline{CNTRST} Setup Time | 1.8 | — | 2.0 | — | 2.0 | — | ns |
| t _{HRST} | \overline{CNTRST} Hold Time | 0.7 | — | 0.7 | — | 1.0 | — | ns |
| t _{OE⁽¹⁾} | Output Enable to Data Valid | — | 4 | — | 5 | — | 6 | ns |
| t _{OLZ} | Output Enable to Output Low-Z | 0 | — | 0 | — | 0 | — | ns |
| t _{OHZ} | Output Enable to Output High-Z | 1 | 4 | 1 | 4.5 | 1 | 5 | ns |
| t _{CD2} | Clock to Data Valid (Pipelined) | — | 4.2 | — | 5 | — | 6 | ns |
| t _{DC} | Data Output Hold After Clock High | 1 | — | 1 | — | 1 | — | ns |
| t _{CKHZ} | Clock High to Output High-Z | 1 | 3 | 1 | 4.5 | 1.5 | 6 | ns |
| t _{CKLZ} | Clock High to Output Low-Z | 1 | — | 1 | — | 1 | — | ns |
| Port-to-Port Delay | | | | | | | | |
| t _{CO} | Clock-to-Clock Offset | 6 | — | 8 | — | 10 | — | ns |

4831 tbl 11

NOTES:

1. All input signals are synchronous with respect to the clock except for the asynchronous Output Enable (\overline{OE}).
2. These values are valid for either level of V_{DD0} (3.3V/2.5V). See page 4 for details on selecting the desired I/O voltage levels for each port.

Timing Waveform of Read Cycle for Pipelined Operation⁽²⁾

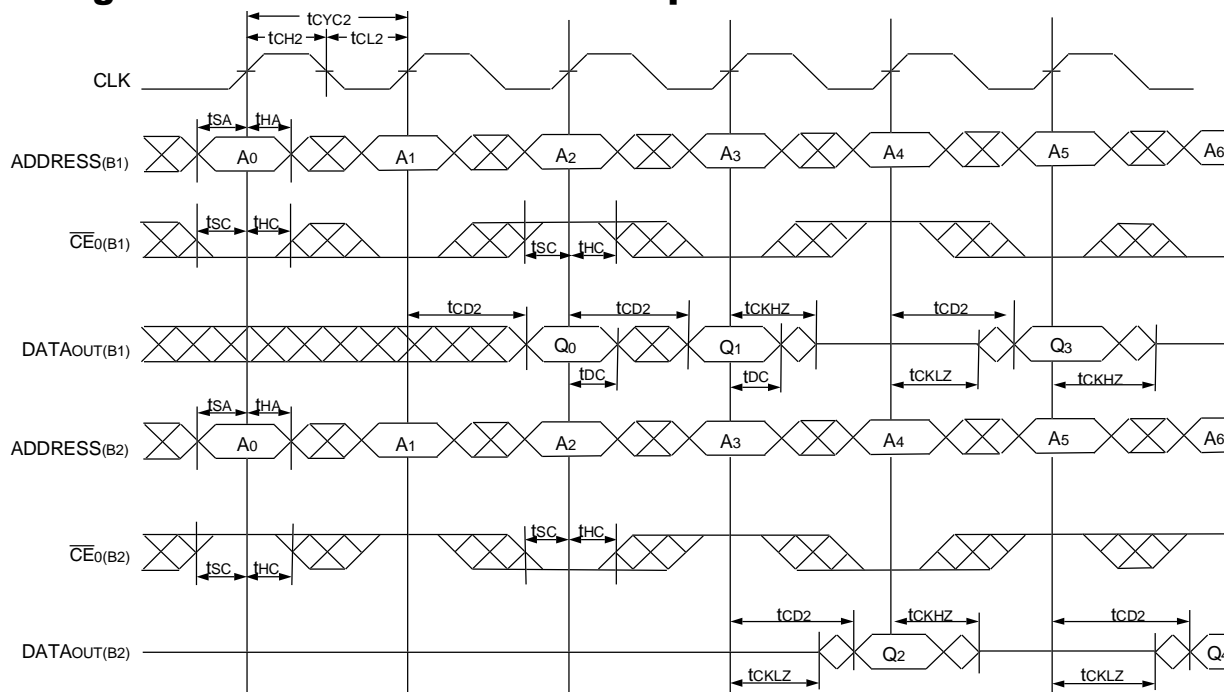


NOTES:

1. \overline{OE} is asynchronously controlled; all other inputs are synchronous to the rising clock edge.
2. $\overline{ADS} = V_{IL}$, \overline{CNTEN} and $\overline{CNRST} = V_{IH}$.
3. The output is disabled (High-Impedance state) by $\overline{CE}_0 = V_{IH}$, $CE_1 = V_{IL}$, $\overline{BE}_n = V_{IH}$ following the next rising edge of the clock. Refer to Truth Table 1.
4. Addresses do not have to be accessed sequentially since $\overline{ADS} = V_{IL}$ constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. If \overline{BE}_n was HIGH, then the appropriate Byte of DATAout for $Q_n + 2$ would be disabled (High-Impedance state).

4831 drw 06

Timing Waveform of a Multi-Device Pipelined Read^(1,2)

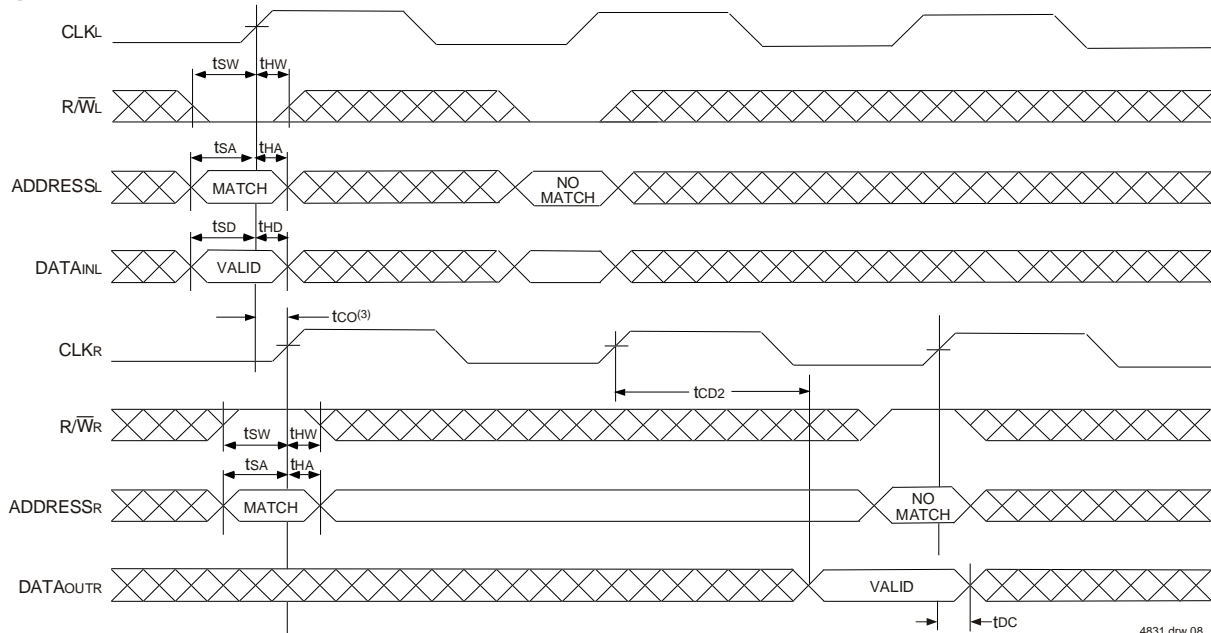


NOTES:

1. B1 Represents Device #1; B2 Represents Device #2. Each Device consists of one IDT70V3569 for this waveform, and are setup for depth expansion in this example. ADDRESS_(B1) = ADDRESS_(B2) in this situation.
2. \overline{BE}_n , \overline{OE} , and $\overline{ADS} = V_{IL}$; $CE_1(B_2)$, R/\overline{W} , \overline{CNTEN} , and $\overline{CNRST} = V_{IH}$.

4831 drw 07

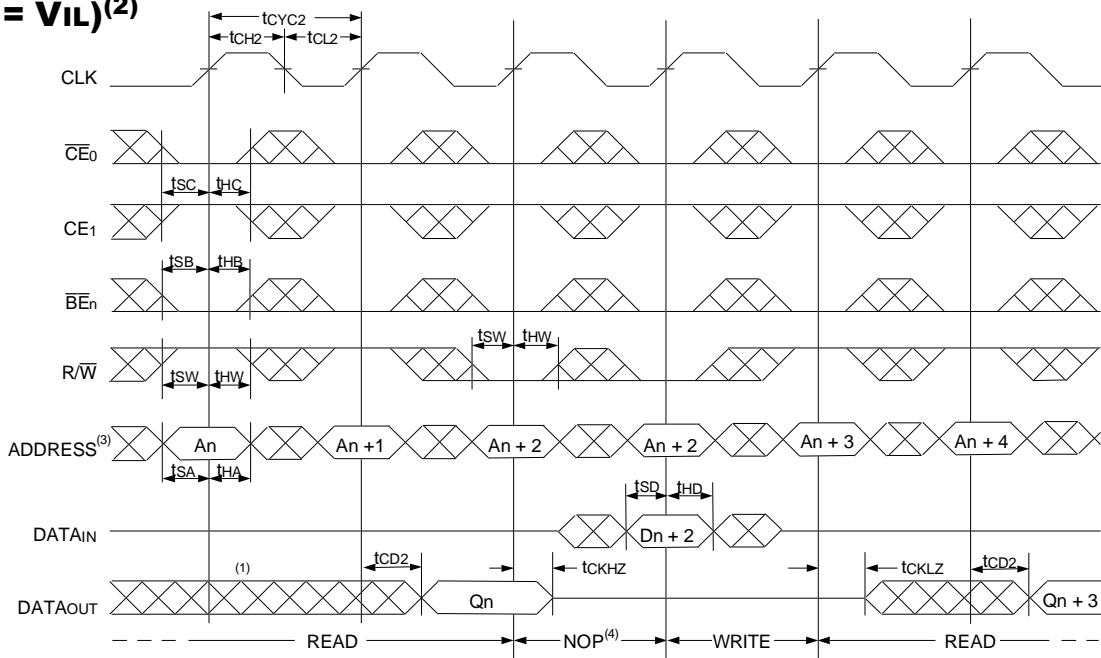
Timing Waveform of Left Port Write to Pipelined Right Port Read^(1,2)



NOTES:

1. \overline{CE}_0 , \overline{BE}_n , and $\overline{ADS} = V_{IL}$; CE_1 , \overline{CNTEN} , and $\overline{CNTRST} = V_{IH}$.
2. $\overline{OE} = V_{IL}$ for the Right Port, which is being read from. $\overline{OE} = V_{IH}$ for the Left Port, which is being written to.
3. If $t_{co} \leq$ minimum specified, then data from right port read is not valid until following right port clock cycle (ie, time from write to valid read on opposite port will be $t_{co} + 2 t_{CYC2} + t_{CD2}$). If $t_{co} >$ minimum, then data from right port read is available on first right port clock cycle (ie, time from write to valid read on opposite port will be $t_{co} + t_{CYC} + t_{CD2}$).

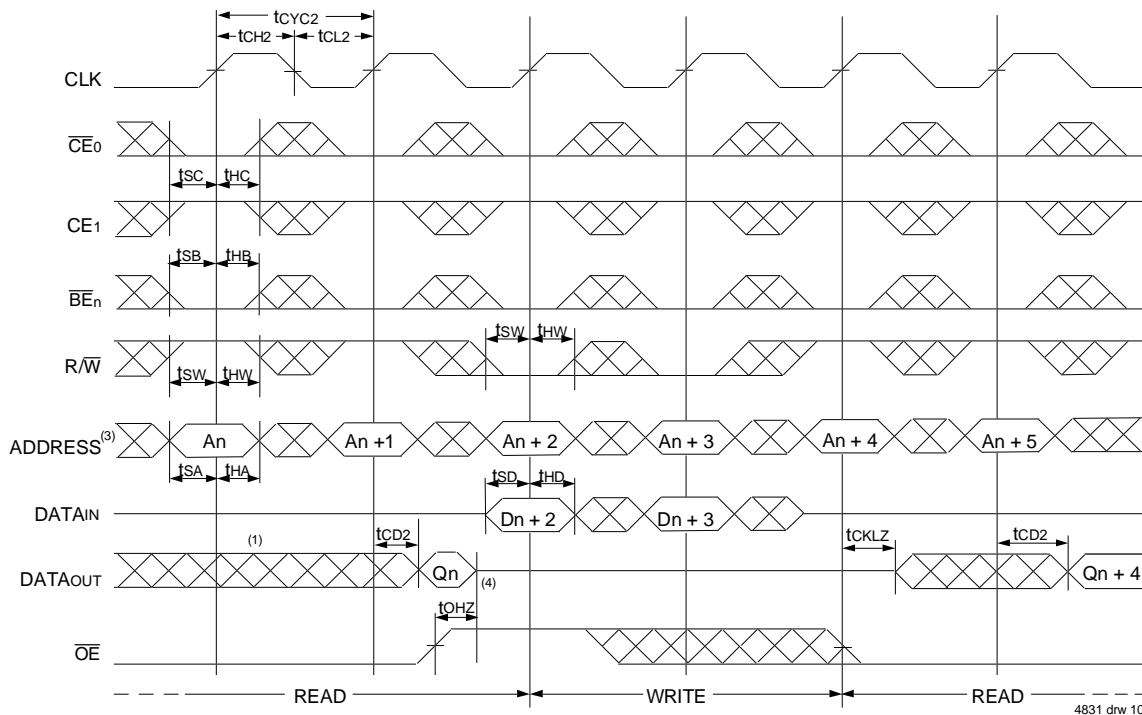
Timing Waveform of Pipelined Read-to-Write-to-Read ($\overline{OE} = V_{IL}$)⁽²⁾



NOTES:

1. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
2. \overline{CE}_0 , \overline{BE}_n , and $\overline{ADS} = V_{IL}$; CE_1 , \overline{CNTEN} , and $\overline{CNTRST} = V_{IH}$. "NOP" is "No Operation".
3. Addresses do not have to be accessed sequentially since $\overline{ADS} = V_{IL}$ constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
4. "NOP" is "No Operation." Data in memory at the selected address may be corrupted and should be re-written to guarantee data integrity.

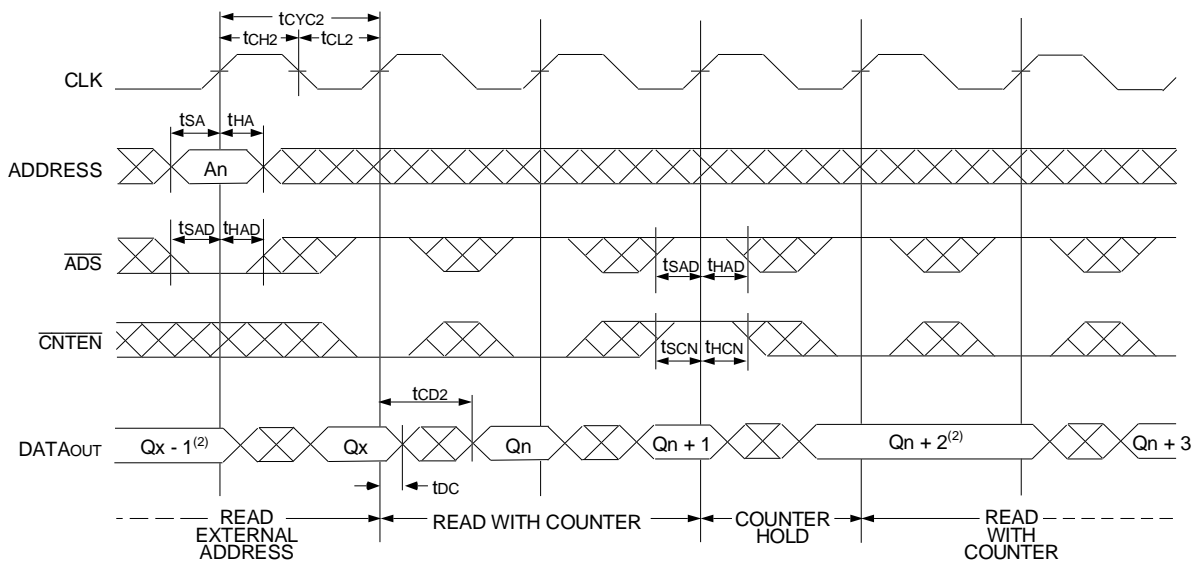
Timing Waveform of Pipelined Read-to-Write-to-Read (\overline{OE} Controlled)⁽²⁾



NOTES:

1. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
2. \overline{CE}_0 , \overline{BE}_n , and $\overline{ADS} = V_{IL}$; \overline{CE}_1 , \overline{CNTEN} , and $\overline{CNTRST} = V_{IH}$.
3. Addresses do not have to be accessed sequentially since $\overline{ADS} = V_{IL}$ constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
4. This timing does not meet requirements for fastest speed grade. This waveform indicates how logically it could be done if timing so allows.

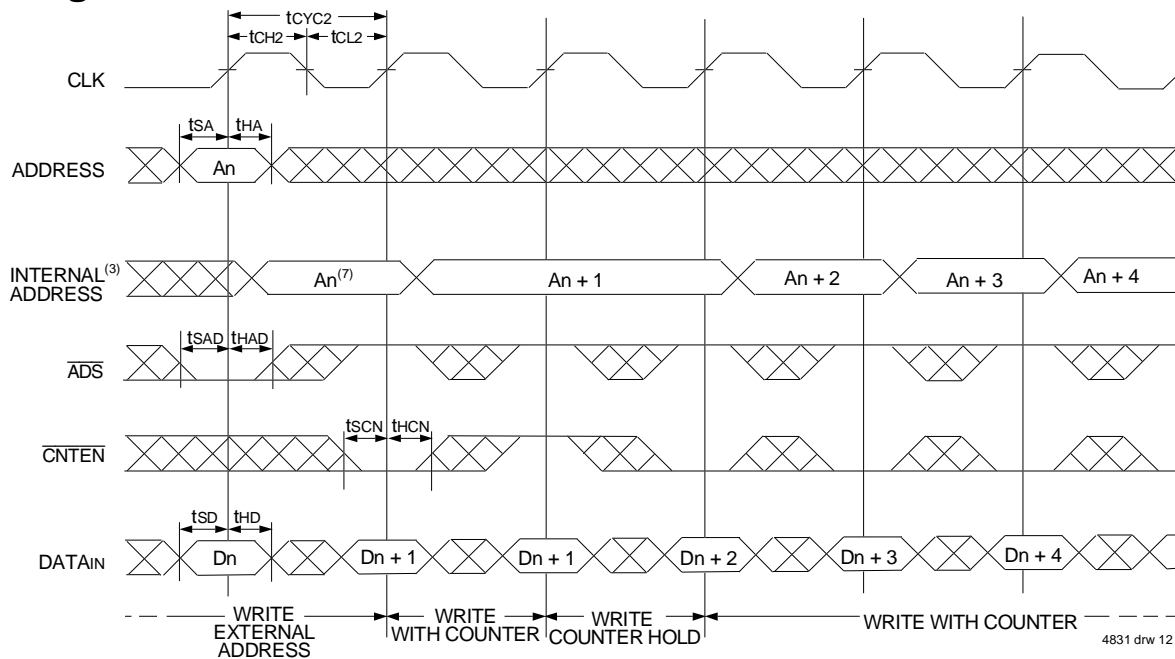
Timing Waveform of Pipelined Read with Address Counter Advance⁽¹⁾



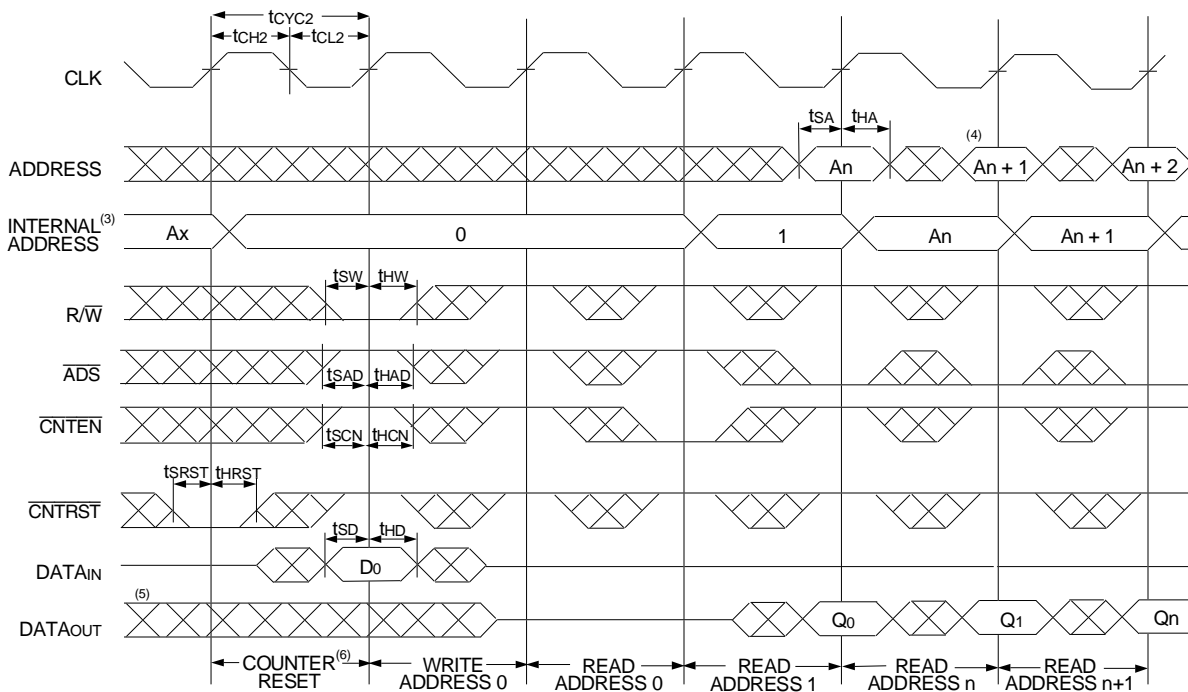
NOTES:

1. \overline{CE}_0 , \overline{OE} , $\overline{BE}_n = V_{IL}$; \overline{CE}_1 , $\overline{R/W}$, and $\overline{CNTRST} = V_{IH}$.
2. If there is no address change via $\overline{ADS} = V_{IL}$ (loading a new address) or $\overline{CNTEN} = V_{IL}$ (advancing the address), i.e. $\overline{ADS} = V_{IH}$ and $\overline{CNTEN} = V_{IH}$, then the data output remains constant for subsequent clocks.

Timing Waveform of Write with Address Counter Advance⁽¹⁾



Timing Waveform of Counter Reset⁽²⁾



NOTES:

1. \overline{CE}_0 , \overline{BE}_n , and $R/\overline{W} = V_{IL}$; CE_1 and $\overline{CNTRST} = V_{IH}$.
2. \overline{CE}_0 , $\overline{BE}_n = V_{IL}$; $CE_1 = V_{IH}$.
3. The "Internal Address" is equal to the "External Address" when $\overline{ADS} = V_{IL}$ and equals the counter output when $\overline{ADS} = V_{IH}$.
4. Addresses do not have to be accessed sequentially since $\overline{ADS} = V_{IL}$ constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
6. No dead cycle exists during counter reset. A READ or WRITE cycle may be coincidental with the counter reset cycle: Addr 0 will be accessed. Extra cycles are shown here simply for clarification.
7. $\overline{CNTEN} = V_{IL}$ advances Internal Address from 'An' to 'An + 1'. The transition shown indicates the time required for the counter to advance. The 'An + 1' Address is written to during this cycle.

Functional Description

The IDT70V3569 provides a true synchronous Dual-Port Static RAM interface. Registered inputs provide minimal set-up and hold times on address, data, and all critical control inputs. All internal registers are clocked on the rising edge of the clock signal, however, the self-timed internal write pulse is independent of the LOW to HIGH transition of the clock signal.

An asynchronous output enable is provided to ease asynchronous bus interfacing. Counter enable inputs are also provided to stall the operation of the address counters for fast interleaved memory applications.

A HIGH on $\overline{CE_0}$ or a LOW on CE_1 for one clock cycle will power down the internal circuitry to reduce static power consumption. Multiple chip enables allow easier banking of multiple IDT70V3569s for depth expansion configurations. Two cycles are required with $\overline{CE_0}$ LOW and CE_1 HIGH to re-activate the outputs.

Depth and Width Expansion

The IDT70V3569 features dual chip enables (refer to Truth Table I) in order to facilitate rapid and simple depth expansion with no requirements for external logic. Figure 4 illustrates how to control the various chip enables in order to expand two devices in depth.

The IDT70V3569 can also be used in applications requiring expanded width, as indicated in Figure 4. Through combining the control signals, the devices can be grouped as necessary to accommodate applications needing 72-bits or wider.

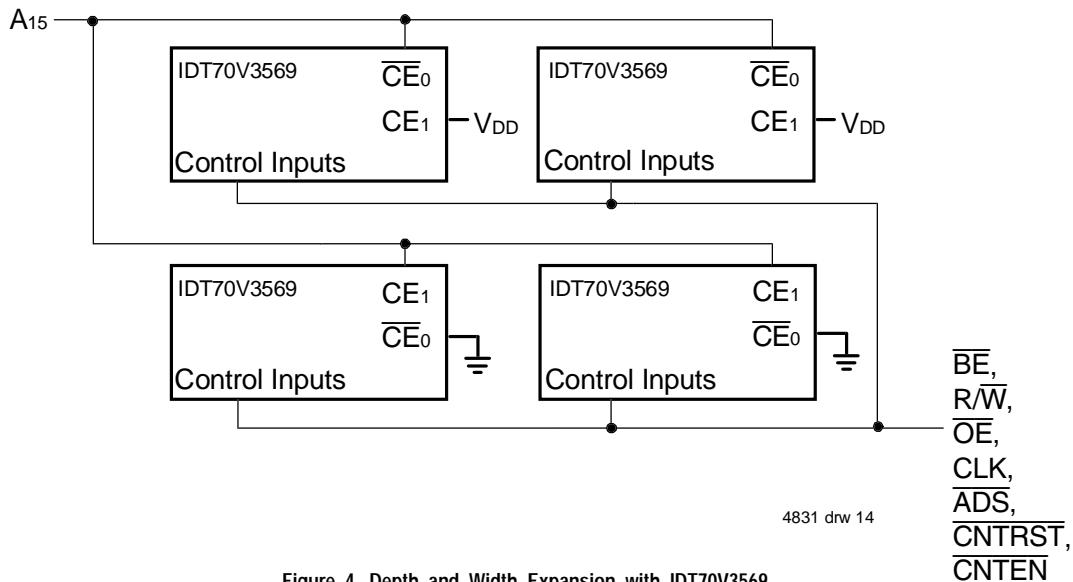
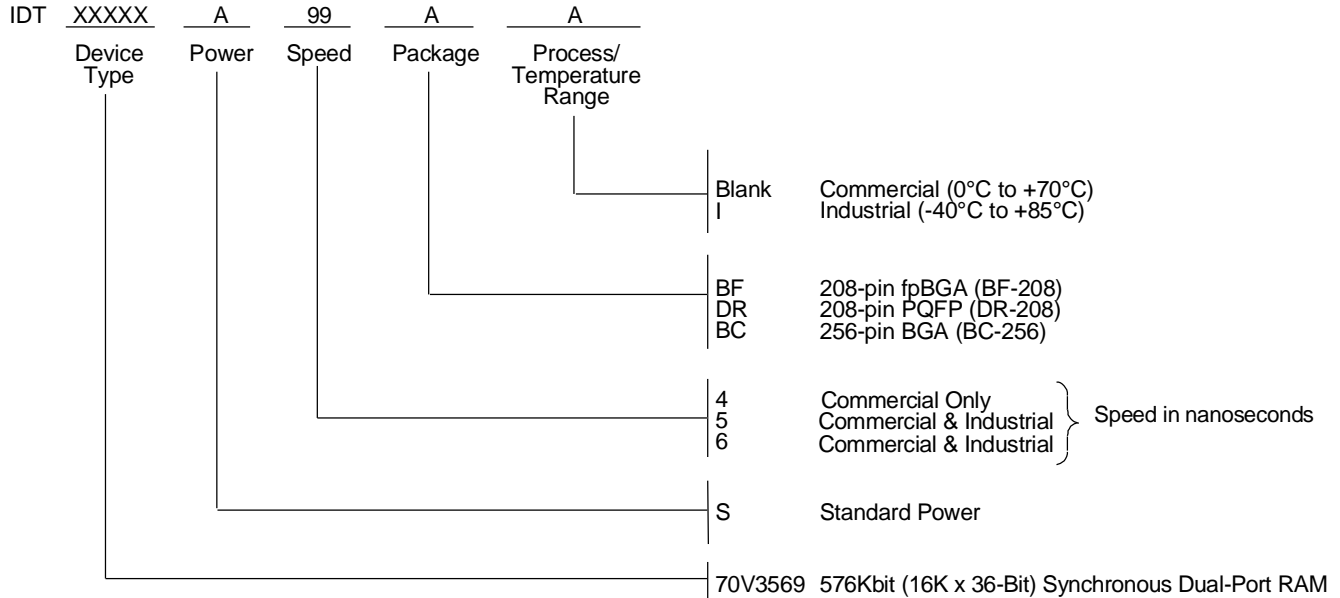


Figure 4. Depth and Width Expansion with IDT70V3569

Ordering Information



4831 drw 15A

Datasheet Document History

- 1/8/99: Initial Public Release
- 3/12/99: Added fpBGA package
- 4/28/99: Fixed typo on page 10
- 6/8/99: Changed drawing format
 - Page 2 Changed package body dimensions
 - Page 3 Fixed typo
- 6/15/99: Page 5 Deleted note 6 for Table II
- 8/4/99: Page 2 Fixed typographical error
 - Page 6 Improved power number
- 10/14/99: Upgraded speed to 133MHz, added 2.5V I/O capability
- 10/19/99: Page 4 Corrected I/O numbers in Truth Table I
- 11/12/99: Replaced IDT logo
- 4/10/00: Added new BGA packages, added full 2.5V interface capability
- 1/12/01: Page 6 Updated Truth Table II
 - Increated storage temperature parameter
 - Clarified TA Parameter
- Page 8 DC Electrical parameters—changed wording from "open" to "disabled"
 Removed note 7 on DC Electrical Characteristics table
- Removed Preliminary status
- 4/10/01: Added Industrial Temperature Ranges and removed related notes



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