



Integrated Device Technology, Inc.

# HIGH-SPEED 2K x 16 CMOS DUAL-PORT STATIC RAMS

IDT7133SA/LA  
IDT7143SA/LA

## FEATURES:

- High-speed access
  - Military: 25/35/45/55/70/90ns (max.)
  - Commercial: 20/25/35/45/55/70/90ns (max.)
- Low-power operation
  - IDT7133/43SA
    - Active: 500 mW (typ.)
    - Standby: 5mW (typ.)
  - IDT7133/43LA
    - Active: 500mW (typ.)
    - Standby: 1mW (typ.)
- Versatile control for write: separate write control for lower and upper byte of each port
- MASTER IDT7133 easily expands data bus width to 32 bits or more using SLAVE IDT7143
- On-chip port arbitration logic (IDT7133 only)
- $\overline{BUSY}$  output flag on IDT7133;  $\overline{BUSY}$  input on IDT7143
- Fully asynchronous operation from either port
- Battery backup operation—2V data retention
- TTL-compatible; single 5V ( $\pm 10\%$ ) power supply
- Available in 68-pin ceramic PGA, 68-pin Flatpack, 68-pin PLCC, and 100-pin TQFP
- Military product compliant to MIL-STD-883, Class B
- Industrial temperature range ( $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ) is available, tested to military electrical specifications

## DESCRIPTION:

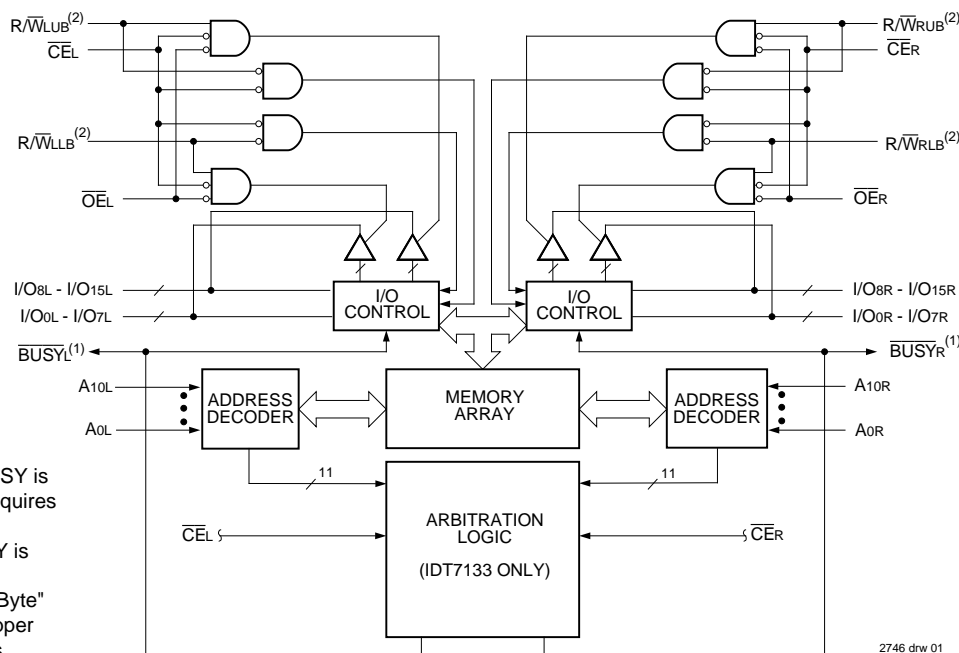
The IDT7133/7143 are high-speed 2K x 16 Dual-Port Static RAMs. The IDT7133 is designed to be used as a stand-alone 16-bit Dual-Port RAM or as a "MASTER" Dual-Port RAM together with the IDT7143 "SLAVE" Dual-Port in 32-bit-or-more word width systems. Using the IDT MASTER/SLAVE Dual-Port RAM approach in 32-bit-or-wider memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

Both devices provide two independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down feature, controlled by  $\overline{CE}$ , permits the on-chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CMOS high-performance technology, these devices typically operate on only 500mW of power. Low-power (LA) versions offer battery backup data retention capability, with each port typically consuming 200 $\mu\text{W}$  for a 2V battery.

The IDT7133/7143 devices have identical pinouts. Each is packaged in a 68-pin ceramic PGA, a 68-pin flatpack, a 68-pin PLCC, and a 100-pin TQFP. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

## FUNCTIONAL BLOCK DIAGRAM



### NOTES:

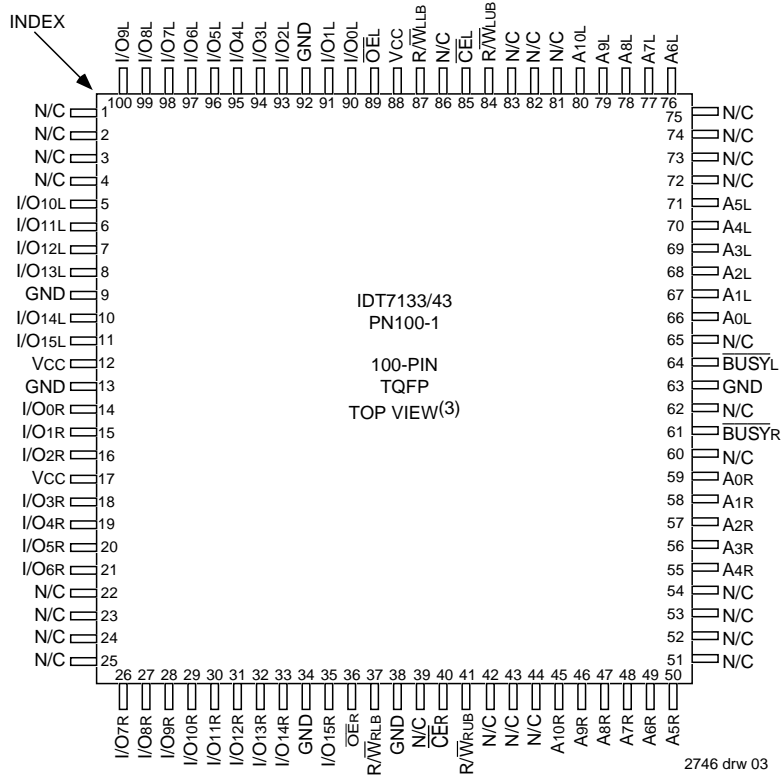
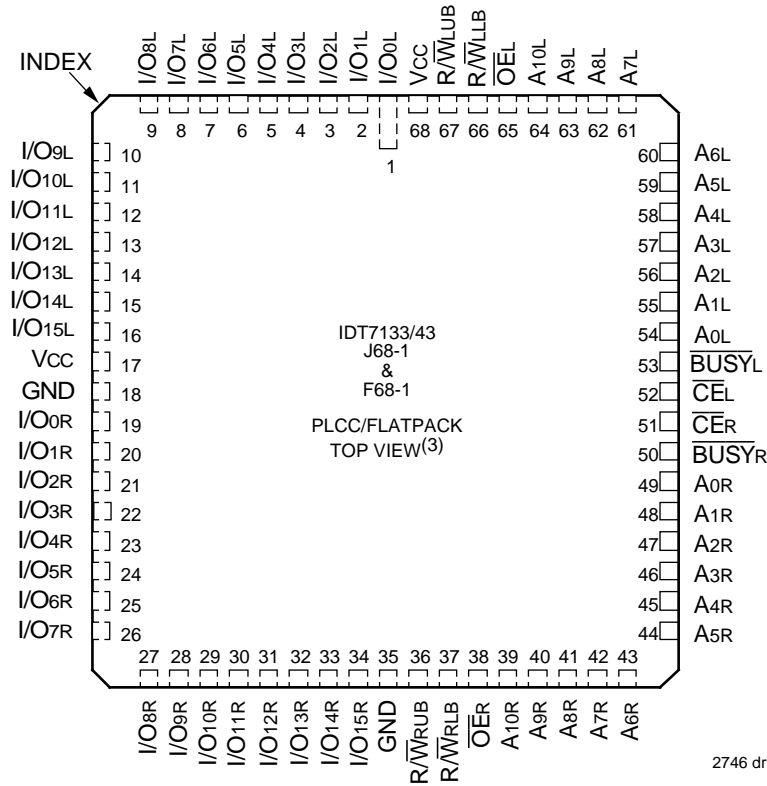
1. IDT7133 (MASTER):  $\overline{BUSY}$  is open drain output and requires pull-up resistor of 270 $\Omega$ . IDT7143 (SLAVE):  $\overline{BUSY}$  is input.
2. "LB" designates "Lower Byte" and "UB" designates "Upper Byte" for the R/W signals.

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**MILITARY AND COMMERCIAL TEMPERATURE RANGES**

**OCTOBER 1996**

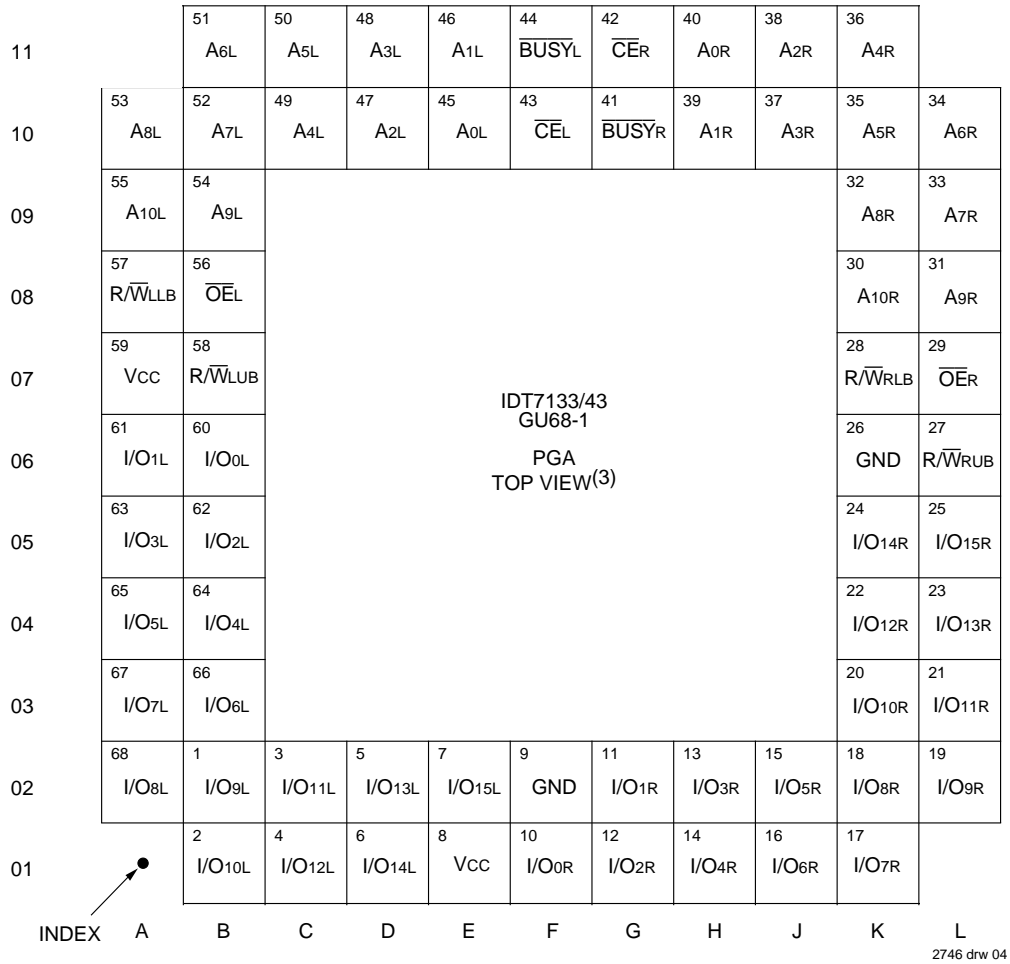
**PIN CONFIGURATIONS<sup>(1,2)</sup>**



**NOTES:**

1. Both Vcc pins must be connected to the supply to ensure reliable operation.
2. Both GND pins must be connected to the supply to ensure reliable operation.
3. This text does not indicate orientation of the actual part-marking.

**PIN CONFIGURATIONS (CONT'D)<sup>(1,2)</sup>**



**NOTES:**

1. Both Vcc pins must be connected to the supply to ensure reliable operation.
2. Both GND pins must be connected to the supply to ensure reliable operation.
3. This text does not indicate orientation of the actual part-marking.

**PIN NAMES**

Left Port	Right Port	Names
$\overline{\text{CE}}\text{L}$	$\overline{\text{CE}}\text{R}$	Chip Enable
$\text{R}/\overline{\text{W}}\text{LUB}$	$\text{R}/\overline{\text{W}}\text{RUB}$	Upper Byte Read/Write Enable
$\text{R}/\overline{\text{W}}\text{LLB}$	$\text{R}/\overline{\text{W}}\text{RLB}$	Lower Byte Read/Write Enable
$\overline{\text{OE}}\text{L}$	$\overline{\text{OE}}\text{R}$	Output Enable
A0L – A10L	A0R – A10R	Address
I/O0L – I/O15L	I/O0R – I/O15R	Data Input/Output
$\overline{\text{BUSY}}\text{L}$	$\overline{\text{BUSY}}\text{R}$	Busy Flag
VCC		Power
GND		Ground

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

Symbol	Rating	Commercial	Military	Unit
V <sub>TERM</sub> <sup>(2)</sup>	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T <sub>A</sub>	Operating Temperature	0 to +70	-55 to +125	°C
T <sub>BIAS</sub>	Temperature Under Bias	-55 to +125	-65 to +135	°C
T <sub>STG</sub>	Storage Temperature	-55 to +125	-65 to +150	°C
P <sub>T</sub> <sup>(3)</sup>	Power Dissipation	2.0	2.0	W
I <sub>OUT</sub>	DC Output Current	50	50	mA

- NOTES:** 2746 tbl 02
- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
  - V<sub>TERM</sub> must not exceed V<sub>CC</sub> + 0.5V for more than 25% of the cycle time or 10ns maximum, and is limited to ≤ 20mA for the period of V<sub>TERM</sub> ≥ V<sub>CC</sub> + 0.5V.

**CAPACITANCE<sup>(1)</sup>**

(T<sub>A</sub> = +25°C, f = 1.0MHz) TQFP ONLY

Symbol	Parameter	Conditions <sup>(2)</sup>	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 3dV	9	pF
C <sub>OUT</sub>	Input/Output Capacitance	V <sub>OUT</sub> = 3dV	10	pF

- NOTES:** 2746 tbl 03
- This parameter is determined by device characterization but is not production tested.
  - 3dV represents the interpolated capacitance when the input and output signals switch from 0V to 3V or from 3V to 0V.

**RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE**

Grade	Ambient Temperature	GND	V <sub>CC</sub>
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2746 tbl 04

**RECOMMENDED DC OPERATING CONDITIONS**

Symbol	Parameter	Min.	Typ.	Max.	Unit
V <sub>CC</sub>	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V <sub>IH</sub>	Input High Voltage	2.2	—	6.0	V
V <sub>IL</sub>	Input Low Voltage	-0.5 <sup>(1)</sup>	—	0.8	V

- NOTES:** 2746 tbl 05
- V<sub>IL</sub> (min.) = -1.5V for pulse width less than 10ns.
  - V<sub>TERM</sub> must not exceed V<sub>CC</sub> + 0.5V.

**DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE** (Either port, V<sub>CC</sub> = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	IDT7133SA IDT7143SA		IDT7133LA IDT7143LA		Unit
			Min.	Max.	Min.	Max.	
I <sub>LI</sub>	Input Leakage Current <sup>(1)</sup>	V <sub>CC</sub> = 5.5V, V <sub>IN</sub> = 0V to V <sub>CC</sub>	—	10	—	5	μA
I <sub>LO</sub>	Output Leakage Current	$\overline{CE} = V_{IH}$ , V <sub>OUT</sub> = 0V to V <sub>CC</sub>	—	10	—	5	μA
V <sub>OL</sub>	Output Low Voltage (I/O <sub>0</sub> -I/O <sub>15</sub> )	I <sub>OL</sub> = 4mA	—	0.4	—	0.4	V
V <sub>OL</sub>	Open Drain Output Low Voltage (BUSY)	I <sub>OL</sub> = 16mA	—	0.5	—	0.5	V
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -4mA	2.4	—	2.4	—	V

- NOTE:** 2746 tbl 06
- At V<sub>CC</sub> ≤ 2.0V, input leakages are undefined.

**DC ELECTRICAL CHARACTERISTICS**

**OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE<sup>(3)</sup> ( $V_{CC} = 5.0V \pm 10\%$ )**

Symbol	Parameter	Test Condition	Version	IDT7133X20 <sup>(1)</sup> IDT7143X20 <sup>(1)</sup>		IDT7133X25 IDT7143X25		IDT7133X35 IDT7143X35		Unit
				Typ. <sup>(2)</sup>	Max.	Typ. <sup>(2)</sup>	Max.	Typ. <sup>(2)</sup>	Max.	
I <sub>CC</sub>	Dynamic Operating Current (Both Ports Active)	$\overline{CE} = V_{IL}$ Outputs Open $f = f_{MAX}^{(4)}$	MIL. S	–	–	250	330	240	325	mA
			L	–	–	230	300	220	295	
			COM'L. S	250	310	250	300	240	295	
			L	230	280	230	270	210	250	
I <sub>SB1</sub>	Standby Current (Both Ports — TTL Level Inputs)	$\overline{CE}_L$ and $\overline{CE}_R = V_{IH}$ $f = f_{MAX}^{(4)}$	MIL. S	–	–	25	90	25	75	mA
			L	–	–	25	80	25	65	
			COM'L. S	25	80	25	80	25	70	
			L	25	70	25	70	25	60	
I <sub>SB2</sub>	Standby Current (One Port — TTL Level Inputs)	$\overline{CE}^*A = V_{IL}$ and $\overline{CE}^*B = V_{IH}^{(5)}$ , $f = f_{MAX}^{(4)}$ , Active Port Outputs Open	MIL. S	–	–	140	230	120	200	mA
			L	–	–	100	190	100	180	
			COM'L. S	140	200	140	200	120	180	
			L	120	180	100	170	100	160	
I <sub>SB3</sub>	Full Standby Current (Both Ports — CMOS Level Inputs)	Both Ports $\overline{CE}_L$ & $\overline{CE}_R > V_{CC} - 0.2V$ $V_{IN} > V_{CC} - 0.2V$ or $V_{IN} < 0.2V$ , $f = 0^{(5)}$	MIL. S	–	–	1	30	1	30	mA
			L	–	–	0.2	10	0.2	10	
			COM'L. S	1	15	1	15	1	15	
			L	0.2	5	0.2	4	0.2	4	
I <sub>SB4</sub>	Full Standby Current (One Port — All CMOS Level Inputs)	$\overline{CE}^*A < 0.2V$ and $\overline{CE}^*B > V_{CC} - 0.2V^{(6)}$ $V_{IN} > V_{CC} - 0.2V$ or $V_{IN} < 0.2V$ Active Port Outputs Open, $f = f_{MAX}^{(4)}$	MIL. S	–	–	140	220	120	190	mA
			L	–	–	120	200	100	170	
			COM'L. S	140	190	140	190	120	170	
			L	120	170	120	170	100	150	

**NOTES:**

- Commercial only, 0°C to +70°C temperature range.
- $V_{CC} = 5V$ ,  $T_A = +25^\circ C$  for Typ., and are not production tested.  $I_{CCDC} = 180mA$  (Typ.)
- "X" in part numbers indicates power rating (SA or LA).
- At  $f = f_{MAX}$ , address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1/trc, and using "AC Test Conditions" of input levels of GND to 3V.
- $f = 0$  means no address or control lines change. Applies only to inputs at CMOS level standby.
- Port "A" may be either left or right port. Port "B" is the opposite from port "A".

2746 tbl 07

## DC ELECTRICAL CHARACTERISTICS

### OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE<sup>(3)</sup> ( $V_{CC} = 5.0V \pm 10\%$ )

Symbol	Parameter	Test Condition	Version	IDT7133X45 IDT7143X45		IDT7133X55 IDT7143X55		IDT7133X70/90 IDT7143X70/90		Unit	
				Typ. <sup>(2)</sup>	Max.	Typ. <sup>(2)</sup>	Max.	Typ. <sup>(2)</sup>	Max.		
I <sub>CC</sub>	Dynamic Operating Current (Both Ports Active)	$\overline{CE} = V_{IL}$ Outputs Open $f = f_{MAX}^{(4)}$	MIL. S	230	320	230	315	230	310	mA	
				L	210	290	210	285	210		280
			COM'L. S	230	290	230	285	230	280		210
				L	210	260	210	255	210		
ISB1	Standby Current (Both Ports — TTL Level Inputs)	$\overline{CE}_L$ and $\overline{CE}_R = V_{IH}$ $f = f_{MAX}^{(4)}$	MIL. S	25	80	25	80	25	75	mA	
				L	25	70	25	70	25		65
			COM'L. S	25	75	25	70	25	70		25
				L	25	65	25	60	25		
ISB2	Standby Current (One Port — TTL Level Inputs)	$\overline{CE}^A = V_{IL}$ and $\overline{CE}^B = V_{IH}^{(5)}$ , $f = f_{MAX}^{(4)}$ , Active Port Outputs Open	MIL. S	120	210	120	210	120	200	mA	
				L	100	190	100	190	100		180
			COM'L. S	120	190	120	180	120	180		100
				L	100	170	100	160	100		
ISB3	Full Standby Current (Both Ports — CMOS Level Inputs)	Both Ports $\overline{CE}_L$ & $\overline{CE}_R > V_{CC} - 0.2V$ $V_{IN} > V_{CC} - 0.2V$ or $V_{IN} < 0.2V$ , $f = 0^{(5)}$	MIL. S	1	30	1	30	1	30	mA	
				L	0.2	10	0.2	10	0.2		10
			COM'L. S	1	15	1	15	1	15		0.2
				L	0.2	4	0.2	4	0.2		
ISB4	Full Standby Current (One Port — All CMOS Level Inputs)	$\overline{CE}^A < 0.2V$ and $\overline{CE}^B > V_{CC} - 0.2V^{(6)}$ $V_{IN} > V_{CC} - 0.2V$ or $V_{IN} < 0.2V$ Active Port Outputs Open, $f = f_{MAX}^{(4)}$	MIL. S	120	200	120	200	120	190	mA	
				L	100	180	100	180	100		170
			COM'L. S	120	180	120	170	120	170		100
				L	100	160	100	150	100		

**NOTES:**

2746 tbl 07

- Commercial only, 0°C to +70°C temperature range.
- $V_{CC} = 5V$ ,  $T_A = +25^\circ C$  for Typ., and are not production tested.  $I_{CCDC} = 180mA$  (Typ.)
- "X" in part numbers indicates power rating (SA or LA).
- At  $f = f_{MAX}$ , address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1 / trc, and using "AC Test Conditions" of input levels of GND to 3V.
- $f = 0$  means no address or control lines change. Applies only to inputs at CMOS level standby.
- Port "A" may be either left or right port. Port "B" is the opposite from port "A".

### DATA RETENTION CHARACTERISTICS

(LA Version Only)  $V_{LC} = 0.2V$ ,  $V_{HC} = V_{CC} - 0.2V$

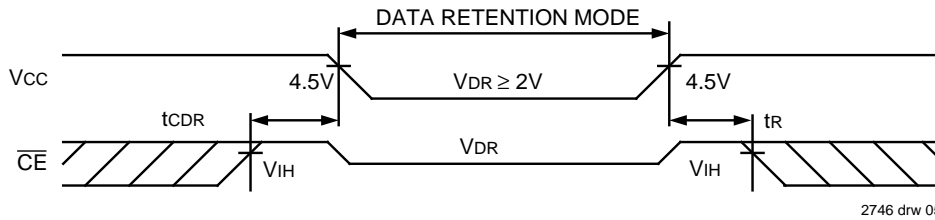
Symbol	Parameter	Test Condition	IDT7133LA/IDT7143LA			Unit
			Min.	Typ.	Max.	
VDR	VCC for Data Retention	$V_{CC} = 2V$	2.0	—	—	V
I <sub>CCDR</sub>	Data Retention Current	$\overline{CE} \geq V_{HC}$ $V_{IN} \geq V_{HC}$ or $\leq V_{LC}$	MIL. —	100	4000	$\mu A$
t <sub>CDR</sub> <sup>(3)</sup>	Chip Deselect to Data Retention Time		0	—	—	ns
t <sub>R</sub> <sup>(3)</sup>	Operation Recovery Time		t <sub>RC</sub> <sup>(2)</sup>	—	—	ns

**NOTES:**

1.  $V_{CC} = 2V$ ,  $T_A = +25^\circ C$ , and are not production tested.
2. t<sub>RC</sub> = Read Cycle Time.
3. This parameter is guaranteed but is not production tested.

2746 tbl 08

### DATA RETENTION WAVEFORM



2746 drw 05

### AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	Figures 1, 2, and 3

2746 tbl 09

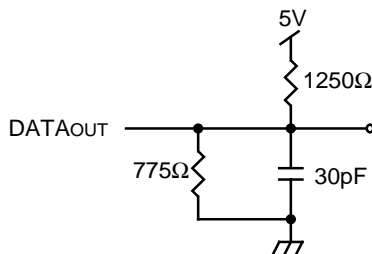


Figure 1. AC Output Load

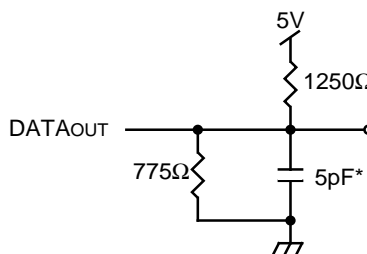


Figure 2. Output Load  
(for t<sub>LZ</sub>, t<sub>HZ</sub>, t<sub>WZ</sub>, t<sub>OW</sub>)  
\*Including scope and jig

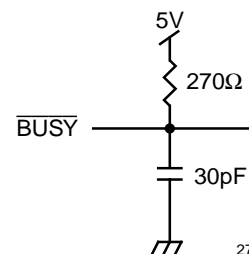


Figure 3.  $\overline{BUSY}$  AC Output Load  
(IDT7133 only)

2746 drw 06

**AC ELECTRICAL CHARACTERISTICS OVER THE  
OPERATING TEMPERATURE AND SUPPLY VOLTAGE<sup>(4)</sup>**

Symbol	Parameter	IDT7133X20 <sup>(2)</sup> IDT7143X20 <sup>(2)</sup>		IDT7133X25 IDT7143X25		IDT7133X35 IDT7143X35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
<b>READ CYCLE</b>								
t <sub>RC</sub>	Read Cycle Time	20	—	25	—	35	—	ns
t <sub>AA</sub>	Address Access Time	—	20	—	25	—	35	ns
t <sub>ACE</sub>	Chip Enable Access Time	—	20	—	25	—	35	ns
t <sub>AOE</sub>	Output Enable Access Time	—	12	—	15	—	20	ns
t <sub>OH</sub>	Output Hold from Address Change	3	—	0	—	0	—	ns
t <sub>LZ</sub>	Output Low-Z Time <sup>(1, 3)</sup>	3	—	0	—	0	—	ns
t <sub>HZ</sub>	Output High-Z Time <sup>(1, 3)</sup>	—	12	—	15	—	20	ns
t <sub>PU</sub>	Chip Enable to Power Up Time <sup>(3)</sup>	0	—	0	—	0	—	ns
t <sub>PD</sub>	Chip Disable to Power Down Time <sup>(3)</sup>	—	20	—	50	—	50	ns

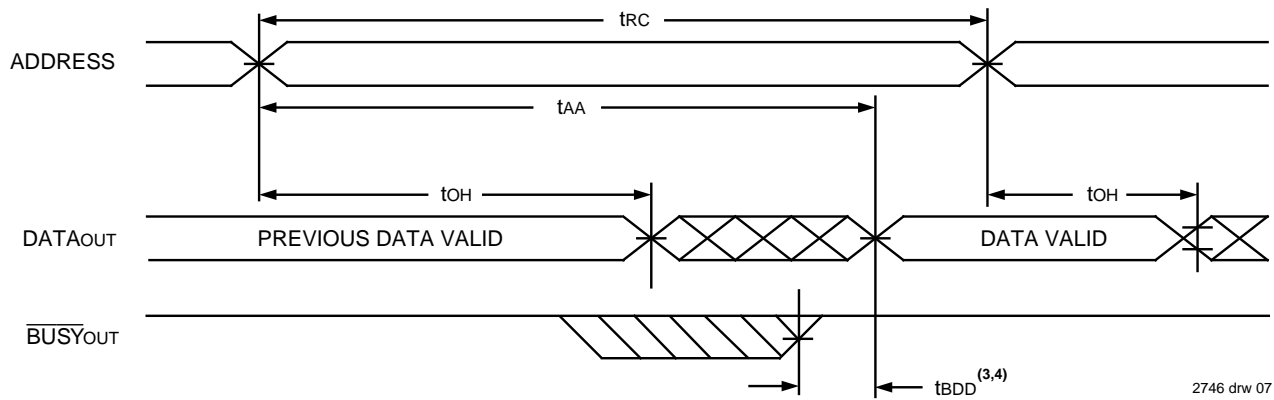
Symbol	Parameter	IDT7133X45 IDT7143X45		IDT7133X55 IDT7143X55		IDT7133X70/90 IDT7143X70/90		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
<b>READ CYCLE</b>								
t <sub>RC</sub>	Read Cycle Time	45	—	55	—	70/90	—	ns
t <sub>AA</sub>	Address Access Time	—	45	—	55	—	70/90	ns
t <sub>ACE</sub>	Chip Enable Access Time	—	45	—	55	—	70/90	ns
t <sub>AOE</sub>	Output Enable Access Time	—	25	—	30	—	40/40	ns
t <sub>OH</sub>	Output Hold from Address Change	0	—	0	—	0/0	—	ns
t <sub>LZ</sub>	Output Low-Z Time <sup>(1, 3)</sup>	0	—	5	—	5/5	—	ns
t <sub>HZ</sub>	Output High-Z Time <sup>(1, 3)</sup>	—	20	—	20	—	25/25	ns
t <sub>PU</sub>	Chip Enable to Power Up Time <sup>(3)</sup>	0	—	0	—	0/0	—	ns
t <sub>PD</sub>	Chip Disable to Power Down Time <sup>(3)</sup>	—	50	—	50	—	50/50	ns

**NOTES:**

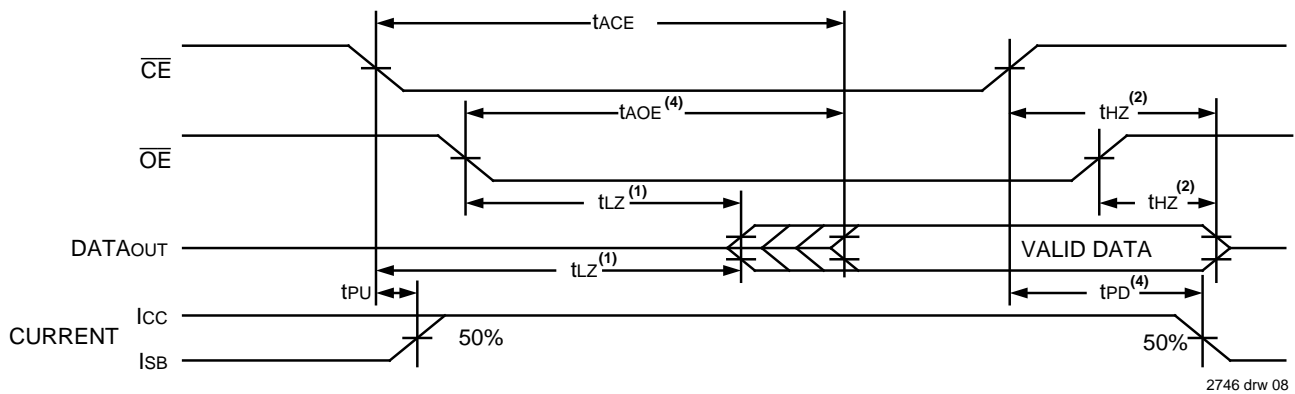
1. Transition is measured ±500mV from Low or High-impedance voltage with Output Test Load (Figure 2).
2. 0°C to +70°C temperature range only.
3. This parameter is guaranteed by device characterization, but is not production tested.
4. "X" in part number indicates power rating (SA or LA).

2746 tbl 10

**TIMING WAVEFORM OF READ CYCLE NO. 1, EITHER SIDE<sup>(1, 2, 4, 5)</sup>**



**TIMING WAVEFORM OF READ CYCLE NO. 2, EITHER SIDE<sup>(1, 3, 5)</sup>**



**NOTES:**

1. Timing depends on which signal is asserted last,  $\overline{OE}$  or  $\overline{CE}$ .
2. Timing depends on which signal is deasserted last,  $\overline{OE}$  or  $\overline{CE}$ .
3.  $t_{BDD}$  delay is required only in a case where the opposite port is completing a write operation to the same address location. For simultaneous read operations,  $\overline{BUSY}$  has no relationship to valid output data.
4. Start of valid data depends on which timing becomes effective last,  $t_{AOE}$ ,  $t_{ACE}$ ,  $t_{AA}$ , or  $t_{BDD}$ .
5.  $R/\overline{W} = V_{IH}$  and the address is valid prior to or coincident with  $\overline{CE}$  transition Low.

### AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE<sup>(7)</sup>

Symbol	Parameter	IDT7133X20 <sup>(2)</sup> IDT7143X20 <sup>(2)</sup>		IDT7133X25 IDT7143X25		IDT7133X35 IDT7143X35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
<b>WRITE CYCLE</b>								
tWC	Write Cycle Time <sup>(4)</sup>	20	—	25	—	35	—	ns
tEW	Chip Enable to End-of-Write	15	—	20	—	25	—	ns
tAW	Address Valid to End-of-Write	15	—	20	—	25	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	ns
tWP	Write Pulse Width <sup>(6)</sup>	15	—	20	—	25	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	ns
tDW	Data Valid to End-of-Write	15	—	15	—	20	—	ns
tHZ	Output High-Z Time <sup>(1,3)</sup>	—	12	—	15	—	20	ns
tDH	Data Hold Time <sup>(5)</sup>	0	—	0	—	0	—	ns
twZ	Write Enable to Output in High-Z <sup>(1,3)</sup>	—	12	—	15	—	20	ns
tOW	Output Active from End-of-Write <sup>(1,3,5)</sup>	0	—	0	—	0	—	ns

### AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE<sup>(7)</sup>

Symbol	Parameter	IDT7133X45 IDT7143X45		IDT7133X55 IDT7143X55		IDT7133X70/90 IDT7143X70/90		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
<b>WRITE CYCLE</b>								
tWC	Write Cycle Time <sup>(4)</sup>	45	—	55	—	70/90	—	ns
tEW	Chip Enable to End-of-Write	30	—	40	—	50/50	—	ns
tAW	Address Valid to End-of-Write	30	—	40	—	50/50	—	ns
tAS	Address Set-up Time	0	—	0	—	0/0	—	ns
tWP	Write Pulse Width <sup>(6)</sup>	30	—	40	—	50/50	—	ns
tWR	Write Recovery Time	0	—	0	—	0/0	—	ns
tDW	Data Valid to End-of-Write	20	—	25	—	30/30	—	ns
tHZ	Output High-Z Time <sup>(1,3)</sup>	—	20	—	20	—	25/25	ns
tDH	Data Hold Time <sup>(5)</sup>	5	—	5	—	5/5	—	ns
twZ	Write Enable to Output in High-Z <sup>(1,3)</sup>	—	20	—	20	—	25/25	ns
tOW	Output Active from End-of-Write <sup>(1,3,5)</sup>	5	—	5	—	5/5	—	ns

**NOTES:**

1. Transition is measured  $\pm 500\text{mV}$  from Low or High-impedance voltage from the Output Test Load (Figure 2)..
2. 0° C to +70°C temperature range only.
3. This parameter is guaranteed by device characterization but is not production tested.
4. For MASTER/SLAVE combination,  $t_{WC} = t_{BAA} + t_{WR} + t_{WP}$ , since  $R\bar{W} = V_{IL}$  must occur after  $t_{BAA}$ .
5. The specification for  $t_{DH}$  must be met by the device supplying write data to the RAM under all operation conditions. Although  $t_{DH}$  and  $t_{OW}$  values will vary over voltage and temperature, the actual  $t_{DH}$  will always be smaller than the actual  $t_{OW}$ .
6. This parameter is determined by device characterization, but is not production tested. Transition is measured  $\pm 200\text{mV}$  from steady state with the Output Test Load (Figure 2).
7. "X" in part number indicates power rating (SA or LA).

2746 tbl 11

**AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE<sup>(7)</sup>**

Symbol	Parameter	IDT7133X20 <sup>(1)</sup> IDT7143X20 <sup>(1)</sup>		IDT7133X25 IDT7143X25		IDT7133X35 IDT7143X35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
<b>BUSY TIMING (For MASTER IDT7133)</b>								
tBAA	$\overline{\text{BUSY}}$ Access Time from Address	—	20	—	20	—	30	ns
tBDA	$\overline{\text{BUSY}}$ Disable Time from Address	—	20	—	20	—	30	ns
tBAC	$\overline{\text{BUSY}}$ Access Time from Chip Enable	—	20	—	20	—	25	ns
tBDC	$\overline{\text{BUSY}}$ Disable Time from Chip Enable	—	17	—	20	—	25	ns
tWDD	Write Pulse to Data Delay <sup>(2)</sup>	—	40	—	50	—	60	ns
tDDD	Write Data Valid to Read Data Delay <sup>(2)</sup>	—	30	—	35	—	45	ns
tBDD	$\overline{\text{BUSY}}$ Disable to Valid Data <sup>(3)</sup>	—	25	—	30	—	35	ns
tAPS	Arbitration Priority Set Up Time <sup>(4)</sup>	5	—	5	—	5	—	ns
tWH	Write Hold After $\overline{\text{BUSY}}$ <sup>(6)</sup>	20	—	20	—	25	—	ns
<b>BUSY INPUT TIMING (For SLAVE IDT7143)</b>								
tWB	$\overline{\text{BUSY}}$ Input to Write <sup>(5)</sup>	0	—	0	—	0	—	ns
tWH	Write Hold After $\overline{\text{BUSY}}$ <sup>(6)</sup>	20	—	20	—	25	—	ns
tWDD	Write Pulse to Data Delay <sup>(2)</sup>	—	40	—	50	—	60	ns
tDDD	Write Data Valid to Read Data Delay <sup>(2)</sup>	—	30	—	35	—	45	ns

2746 tbl 12

**AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE<sup>(7)</sup>**

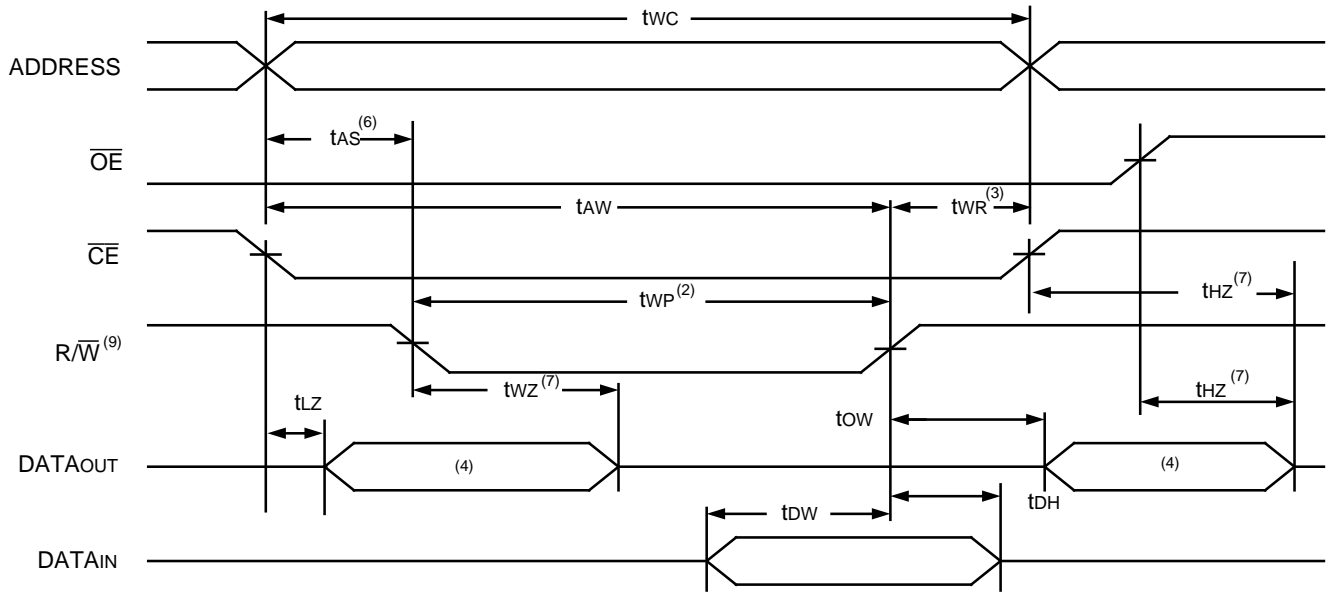
Symbol	Parameter	IDT7133X45 IDT7143X45		IDT7133X55 IDT7143X55		IDT7133X70/90 IDT7143X70/90		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
<b>BUSY TIMING (For MASTER IDT7133)</b>								
tBAA	$\overline{\text{BUSY}}$ Access Time from Address	—	40	—	40	—	45/45	ns
tBDA	$\overline{\text{BUSY}}$ Disable Time from Address	—	40	—	40	—	45/45	ns
tBAC	$\overline{\text{BUSY}}$ Access Time from Chip Enable	—	30	—	35	—	35/35	ns
tBDC	$\overline{\text{BUSY}}$ Disable Time from Chip Enable	—	25	—	30	—	30/30	ns
tWDD	Write Pulse to Data Delay <sup>(2)</sup>	—	80	—	80	—	90/90	ns
tDDD	Write Data Valid to Read Data Delay <sup>(2)</sup>	—	55	—	55	—	70/70	ns
tBDD	$\overline{\text{BUSY}}$ Disable to Valid Data <sup>(3)</sup>	—	40	—	40	—	40/40	ns
tAPS	Arbitration Priority Set Up Time <sup>(4)</sup>	5	—	5	—	5/5	—	ns
tWH	Write Hold After $\overline{\text{BUSY}}$ <sup>(6)</sup>	30	—	30	—	30/30	—	ns
<b>BUSY INPUT TIMING (For SLAVE IDT7143)</b>								
tWB	$\overline{\text{BUSY}}$ Input to Write <sup>(5)</sup>	0	—	0	—	0/0	—	ns
tWH	Write Hold After $\overline{\text{BUSY}}$ <sup>(6)</sup>	30	—	30	—	30/30	—	ns
tWDD	Write Pulse to Data Delay <sup>(2)</sup>	—	80	—	80	—	90/90	ns
tDDD	Write Data Valid to Read Data Delay <sup>(2)</sup>	—	55	—	55	—	70/70	ns

**NOTES:**

- 0°C to +70°C temperature range only.
- Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Write with Port-to-Port Read and Busy".
- tBDD is calculated parameter and is greater of 0, tWDD - tWP (actual), or tDDD - tDW (actual).
- To ensure that the earlier of the two ports wins.
- To ensure that the write cycle is inhibited on port "B" during contention on port "A".
- To ensure that a write cycle is completed on port "B" after contention on port "A".
- "X" in part number indicates power rating (SA or LA).

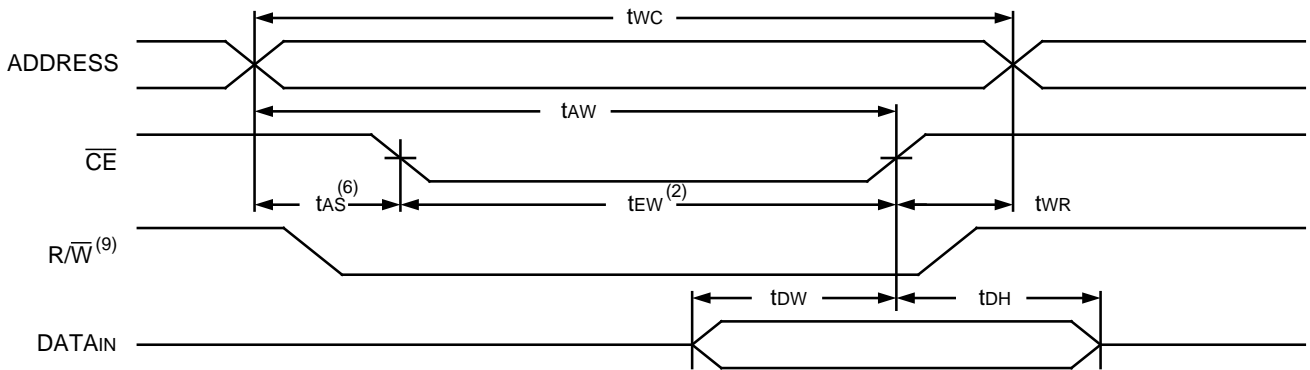
2746 tbl 12

**TIMING WAVEFORM OF WRITE CYCLE NO. 1 ( $\overline{R/\overline{W}}$  CONTROLLED TIMING)<sup>(1, 5, 8)</sup>**



2746 drw 09

**WRITE CYCLE NO. 2 ( $\overline{CE}$  CONTROLLED TIMING)<sup>(1, 5)</sup>**

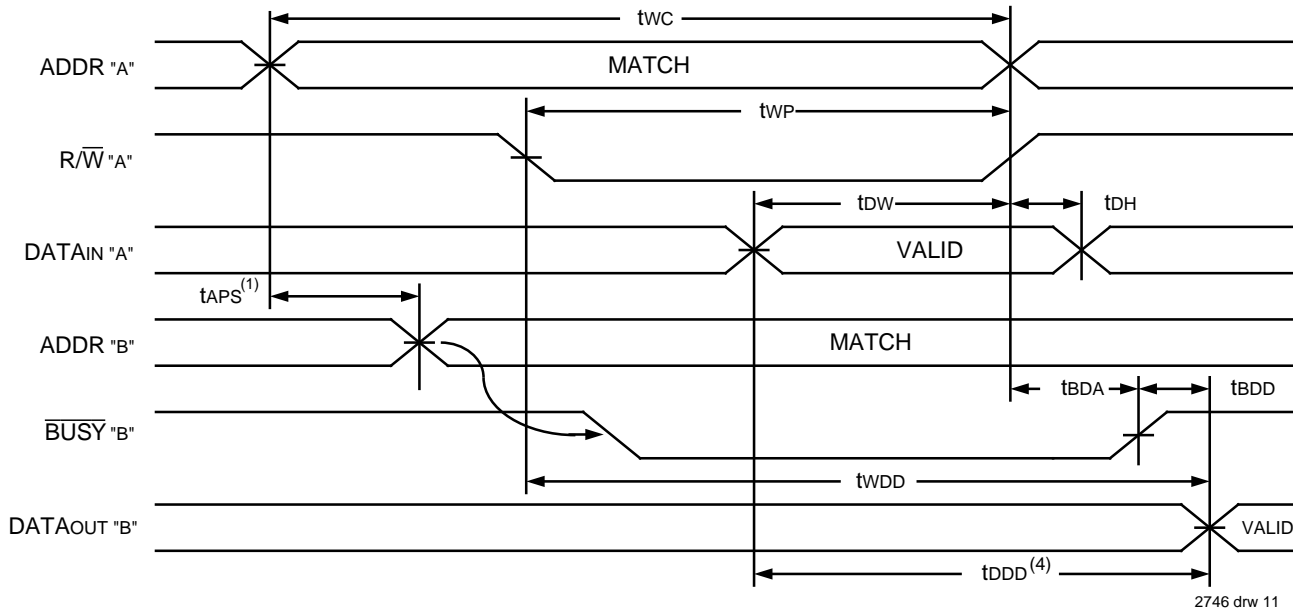


2746 drw 10

**NOTES:**

1.  $\overline{R/\overline{W}}$  or  $\overline{CE}$  must be High during all address transitions.
2. A write occurs during the overlap ( $t_{EW}$  or  $t_{WP}$ ) of a  $\overline{CE} = V_{IL}$  and a  $\overline{R/\overline{W}} = V_{IL}$ .
3.  $t_{WR}$  is measured from the earlier of  $\overline{CE}$  or  $\overline{R/\overline{W}}$  going High to the end of the write cycle.
4. During this period, the I/O pins are in the output state, and input signals must not be applied.
5. If the  $\overline{CE}$  low transition occurs simultaneously with or after the  $\overline{R/\overline{W}}$  low transition, the outputs remain in the High-impedance state.
6. Timing depends on which enable signal ( $\overline{CE}$  or  $\overline{R/\overline{W}}$ ) is asserted last.
7. This parameter is determined by device characterization, but is not production tested. Transition is measured  $\pm 200mV$  from steady state with the Output Test Load (Figure 2).
8. If  $\overline{OE}$  is low during a  $\overline{R/\overline{W}}$  controlled write cycle, the write pulse width must be the larger of  $t_{WP}$  or  $(t_{WZ} + t_{DW})$  to allow the I/O drivers to turn off and data to be placed on the bus for the required  $t_{DW}$ . If  $\overline{OE}$  is High during an  $\overline{R/\overline{W}}$  controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified  $t_{WP}$ .
9.  $\overline{R/\overline{W}}$  for either upper or lower byte.

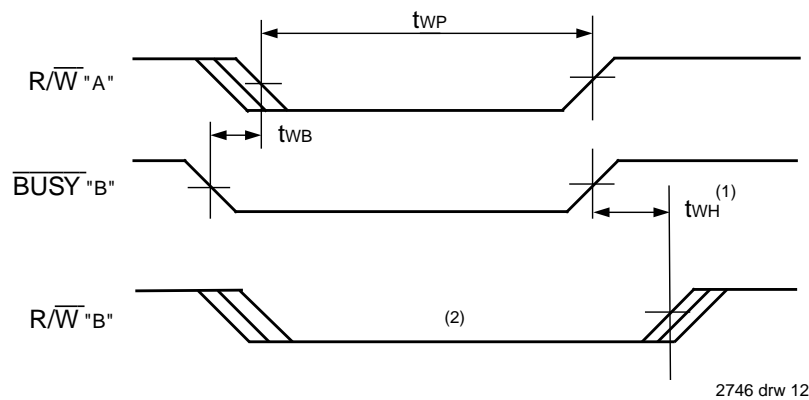
**TIMING WAVEFORM OF WRITE WITH PORT-TO-PORT READ AND  $\overline{\text{BUSY}}$  (1, 2, 3)**



**NOTES:**

1. To ensure that the earlier of the two ports wins,  $t_{APS}$  is ignored for Slave (IDT7143).
2.  $\overline{\text{CE}}_L = \overline{\text{CE}}_R = V_{IL}$
3.  $\overline{\text{OE}} = V_{IL}$  for the reading port.
4. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from port "A".

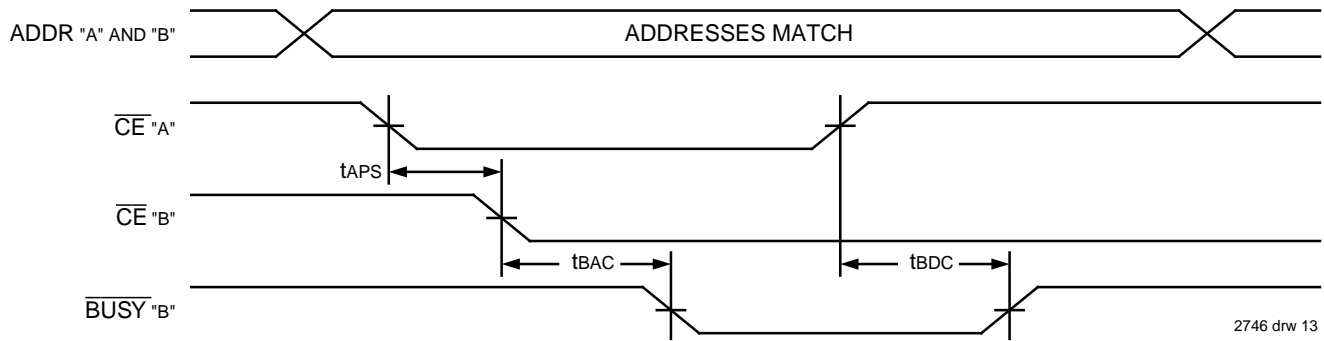
**TIMING WAVEFORM OF WRITE WITH  $\overline{\text{BUSY}}$  ( $M/\overline{\text{S}} = V_{IL}$ )**



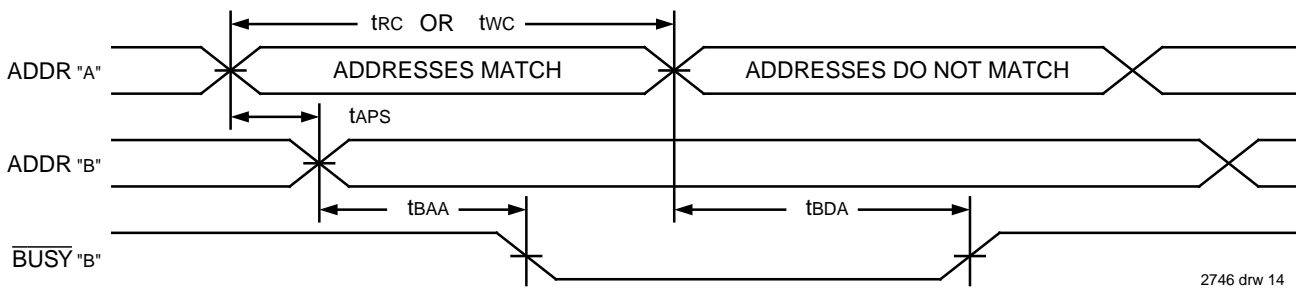
**NOTES:**

1.  $t_{WH}$  must be met for both  $\overline{\text{BUSY}}$  input (SLAVE) and output (MASTER).
2.  $\overline{\text{BUSY}}$  is asserted on port "B" blocking  $R/\overline{W}$  "B", until  $\overline{\text{BUSY}}$  "B" goes High.
3. All timing is the same for left and right ports. Port "A" may be either left or right port. Port "B" is the opposite from port "A".

**TIMING WAVEFORM OF BUSY ARBITRATION CONTROLLED BY  $\overline{CE}$  TIMING (1)**



**TIMING WAVEFORM OF BUSY ARBITRATION CONTROLLED BY ADDRESSES (1)**



**NOTES:**

1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from port "A".
2. If tAPS is not satisfied, the  $\overline{BUSY}$  will be asserted on one side or the other, but there is no guarantee on which side  $\overline{BUSY}$  will be asserted (IDT7133 only).

**FUNCTIONAL DESCRIPTION:**

The IDT7133/43 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. The IDT7133/43 has an automatic power down feature controlled by  $\overline{CE}$ . The  $\overline{CE}$  controls on-chip power down circuitry that permits the respective port to go into a standby mode when not selected ( $\overline{CE}$  High). When a port is enabled, access to the entire memory array is permitted. Non-contention READ/WRITE conditions are illustrated in Truth Table I.

**BUSY LOGIC**

Busy Logic provides a hardware indication that both ports of the RAM have accessed the same location at the same time. It also allows one of the two accesses to proceed and signals the other side that the RAM is "Busy". The busy pin can then be used to stall the access until the operation on the other side is completed. If a write operation has been attempted from the side that receives a busy indication, the write signal is gated internally to prevent the write from proceeding.

The use of busy logic is not required or desirable for all applications. In some cases it may be useful to logically OR the busy outputs together and use any busy indication as an interrupt source to flag the event of an illegal or illogical operation. If the write inhibit function of busy logic is not desirable, the busy logic can be disabled by using the IDT7143 (SLAVE). In the IDT7143, the busy pin operates solely as a write inhibit input pin. Normal operation can be programmed by tying the  $\overline{BUSY}$  pins high. If desired, unintended write operations can be prevented to a port by tying the busy pin for that port low. The busy outputs on the IDT7133 RAM are open drain and require pull-up resistors.

**WIDTH EXPANSION WITH BUSY LOGIC MASTER/SLAVE ARRAYS**

When expanding an IDT7133/43 RAM array in width while using busy logic, one master part is used to decide which side of the RAM array will receive a busy indication, and to output that indication. Any number of slaves to be addressed in the same address range as the master, use the busy signal as a write inhibit signal. Thus on the IDT7133 RAM the busy pin is an output and on the IDT7143 RAM, the busy pin is an input (see Figure 4).

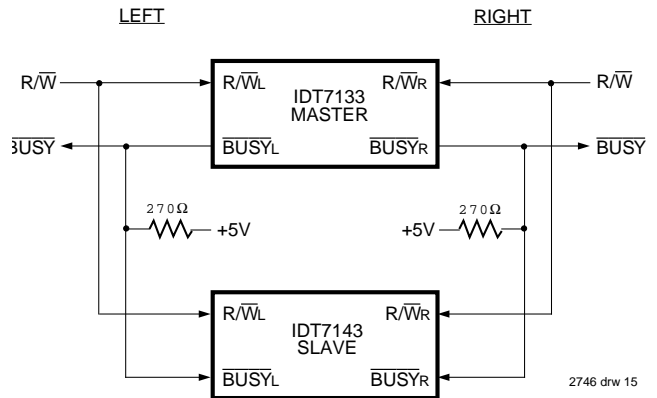


Figure 4. Busy and chip enable routing for both width and depth expansion with the IDT7133 (MASTER) and the IDT7143 (SLAVE).

Expanding the data bus width to 32 bits or more in a Dual-Port RAM system implies that several chips will be active at the same time. If each chip includes a hardware arbitrator, and the addresses for each chip arrive at the same time, it is possible that one will activate its  $\overline{BUSYL}$  while another activates its  $\overline{BUSYr}$  signal. Both sides are now busy and the CPUs will await indefinitely for their port to become free.

To avoid the "Busy Lock-Out" problem, IDT has developed a MASTER/SLAVE approach where only one hardware arbitrator, in the MASTER, is used. The SLAVE has  $\overline{BUSY}$  inputs which allow an interface to the MASTER with no external components and with a speed advantage over other systems.

When expanding Dual-Port RAMs in width, the writing of the SLAVE RAMs must be delayed until after the  $\overline{BUSY}$  input has settled. Otherwise, the SLAVE chip may begin a write cycle during a contention situation. Conversely, the write pulse must extend a hold time past  $\overline{BUSY}$  to ensure that a write cycle takes place after the contention is resolved. This timing is inherent in all Dual-Port memory systems where more than one chip is active at the same time.

The write pulse to the SLAVE should be delayed by the maximum arbitration time of the MASTER. If, then, a contention occurs, the write to the SLAVE will be inhibited due to  $\overline{BUSY}$  from the MASTER.

**TRUTH TABLE I — NON-CONTENTION READ/WRITE CONTROL<sup>(4)</sup>**

LEFT OR RIGHT PORT <sup>(1)</sup>						Function
R/W <sub>LB</sub>	R/W <sub>UB</sub>	$\overline{CE}$	$\overline{OE}$	I/O <sub>0-7</sub>	I/O <sub>8-15</sub>	
X	X	H	X	Z	Z	Port Disabled and in Power Down Mode, ISB <sub>2</sub> , ISB <sub>4</sub>
X	X	H	X	Z	Z	$\overline{CE}_R = \overline{CE}_L = V_{IH}$ , Power Down Mode, ISB <sub>1</sub> or ISB <sub>3</sub>
L	L	L	X	DATA <sub>IN</sub>	DATA <sub>IN</sub>	Data on Lower Byte and Upper Byte Written into Memory <sup>(2)</sup>
L	H	L	L	DATA <sub>IN</sub>	DATA <sub>OUT</sub>	Data on Lower Byte Written into Memory <sup>(2)</sup> , Data in Memory Output on Upper Byte <sup>(3)</sup>
H	L	L	L	DATA <sub>OUT</sub>	DATA <sub>IN</sub>	Data in Memory Output on Lower Byte <sup>(3)</sup> , Data on Upper Byte Written into Memory <sup>(2)</sup>
L	H	L	H	DATA <sub>IN</sub>	Z	Data on Lower Byte Written into Memory <sup>(2)</sup>
H	L	L	H	Z	DATA <sub>IN</sub>	Data on Upper Byte Written into Memory <sup>(2)</sup>
H	H	L	L	DATA <sub>OUT</sub>	DATA <sub>OUT</sub>	Data in Memory Output on Lower Byte and Upper Byte
H	H	L	H	Z	Z	High Impedance Outputs

**NOTES:**

1. A<sub>0L</sub> - A<sub>10L</sub> ≠ A<sub>0R</sub> - A<sub>10R</sub>.
2. If  $\overline{BUSY} = V_{IL}$ , data is not written.
3. If  $\overline{BUSY} = V_{IL}$ , data may not be valid, see *twDD* and *tDD* timing.
4. "H" = V<sub>IH</sub>, "L" = V<sub>IL</sub>, "X" = Don't Care, "Z" = High-Impedance, "LB" = Lower Byte, "UB" = Upper Byte.

2746 tbl 13

**TRUTH TABLE II —  
ADDRESS BUSY ARBITRATION**

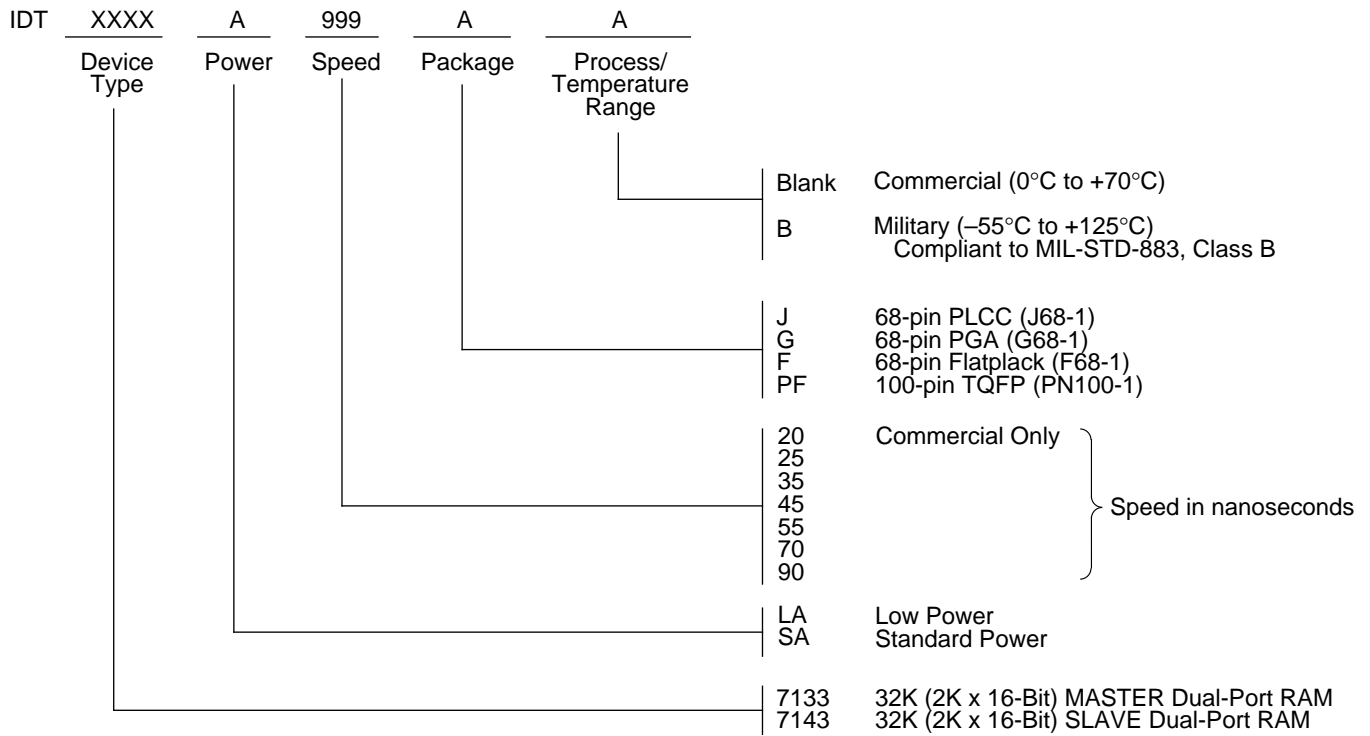
Inputs			Outputs		Function
$\overline{CE}_L$	$\overline{CE}_R$	A <sub>0L</sub> -A <sub>10L</sub> A <sub>0R</sub> -A <sub>10R</sub>	$\overline{BUSY}_L$ <sup>(1)</sup>	$\overline{BUSY}_R$ <sup>(1)</sup>	
X	X	NO MATCH	H	H	Normal
H	X	MATCH	H	H	Normal
X	H	MATCH	H	H	Normal
L	L	MATCH	(2)	(2)	Write Inhibit <sup>(3)</sup>

**NOTES:**

2746 tbl 14

1. Pins  $\overline{BUSY}_L$  and  $\overline{BUSY}_R$  are both outputs on the IDT7133 (MASTER). Both are inputs on the IDT7143 (SLAVE). On Slaves the  $\overline{BUSY}$  input internally inhibits writes.
2. "L" if the inputs to the opposite port were stable prior to the address and enable inputs of this port. "H" if the inputs to the opposite port became stable after the address and enable inputs of this port. If *tAPS* is not met, either  $\overline{BUSY}_L$  or  $\overline{BUSY}_R = \text{LOW}$  will result.  $\overline{BUSY}_L$  and  $\overline{BUSY}_R$  outputs can not be LOW simultaneously.
3. Writes to the left port are internally ignored when  $\overline{BUSY}_L$  outputs are driving LOW regardless of actual logic level on the pin. Writes to the right port are internally ignored when  $\overline{BUSY}_R$  outputs are driving LOW regardless of actual logic level on the pin.

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