Integrated Device Technology, Inc.

# 16-BIT TRI-PORT BUS EXCHANGER

**IDT73720/A**

## FEATURES:

- High-speed 16-bit bus exchange for interbus communication in the following environments:
  - — Multi-way interleaving memory
  - — Multiplexed address and data busses
- Direct interface to R3051 family RISChipSet™
  - — R3051™ family of integrated RISController™ CPUs
  - — R3721 DRAM controller
- Data path for read and write operations
- Low noise 12mA TTL level outputs
- Bidirectional 3-bus architecture: X, Y, Z
  - — One CPU bus: X
  - — Two (interleaved or banked) memory busses:Y & Z
  - — Each bus can be independently latched
- Byte control on all three busses
- Source terminated outputs for low noise and undershoot control
- 68-pin PLCC and 80-pin PQFP package
- High-performance CMOS technology.

## DESCRIPTION:

The IDT73720/A Bus Exchanger is a high speed 16-bit bus exchange device intended for inter-bus communication in interleaved memory systems and high performance multiplexed address and data busses.

The Bus Exchanger is responsible for interfacing between the CPU A/D bus (CPU address/data bus) and multiple memory data busses.

The 73720/A uses a three bus architecture (X, Y, Z), with control signals suitable for simple transfer between the CPU bus (X) and either memory bus (Y or Z). The Bus Exchanger features independent read and write latches for each memory bus, thus supporting a variety of memory strategies. All three ports support byte enable to independently enable upper and lower bytes.

## FUNCTIONAL BLOCK DIAGRAM

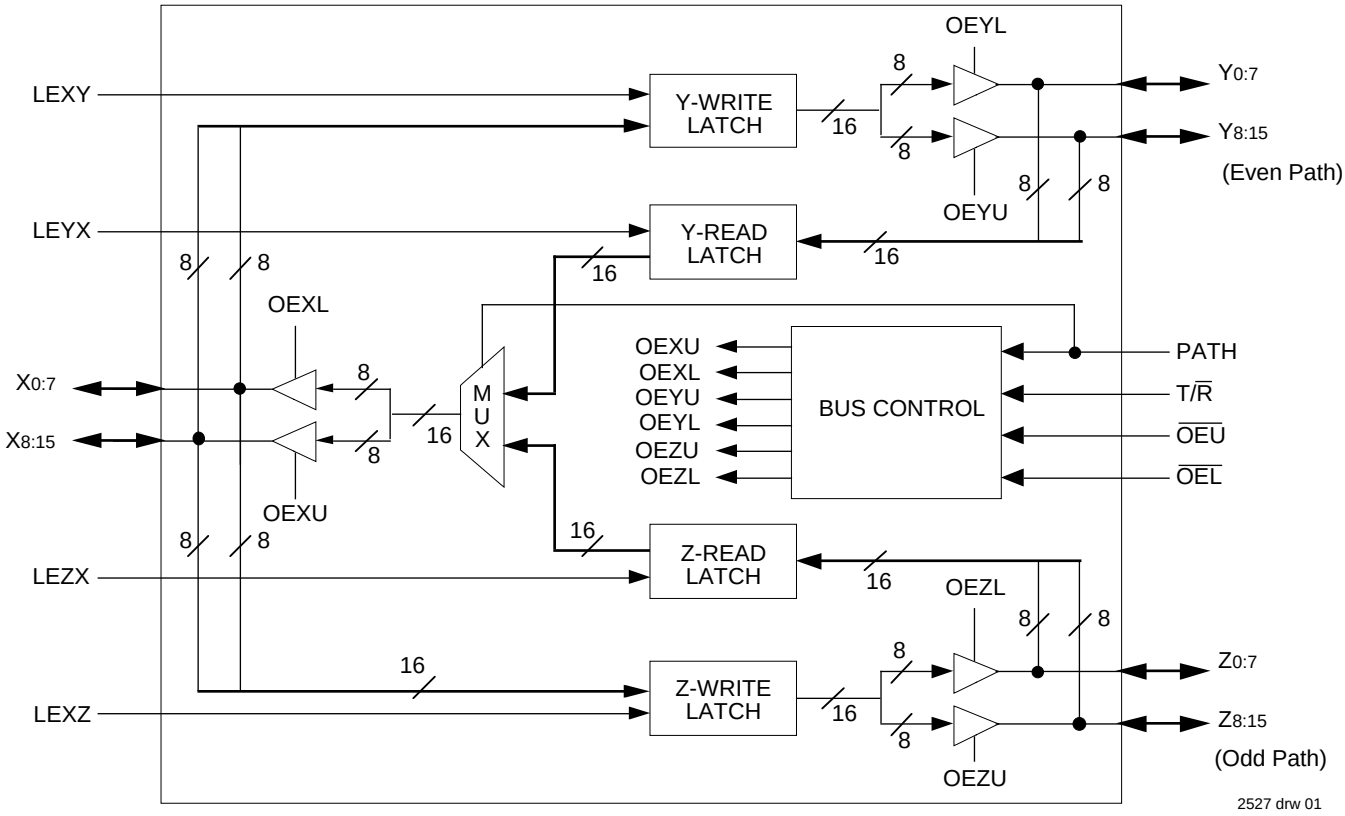
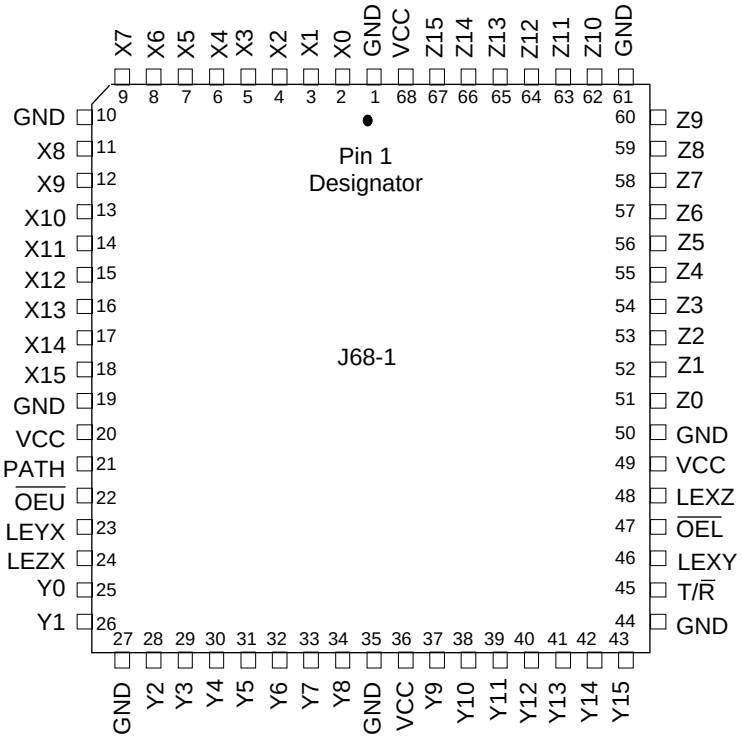



**Figure 1. 73720 Block Diagram**

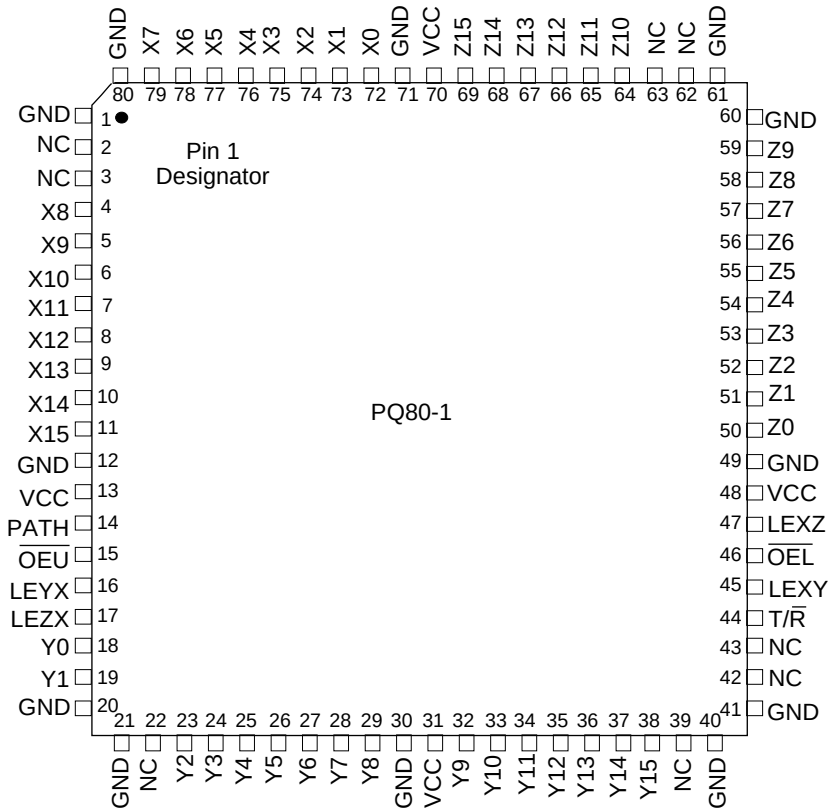
**NOTE:**

1. Logic equations for bus control:
   OEXU = T/$\overline{R}$* . $\overline{OEU}$*; OEXL = T/$\overline{R}$* . $\overline{OEL}$*; OEYU = T/$\overline{R}$ . PATH . $\overline{OEU}$*
   OEYL = T/$\overline{R}$ . PATH . $\overline{OEL}$*; OEZU = T/$\overline{R}$ . PATH* . $\overline{OEU}$*; OEZL = T/$\overline{R}$ . PATH* . $\overline{OEL}$*

## PIN CONFIGURATIONS




**PLCC**
**TOP VIEW**




**PQFP**
**TOP VIEW**

## PIN DESCRIPTION

| Signal | I/O | Description |
|---|---|---|
| X(0:15) | I/O | Bidirectional Data Port X. Usually connected to the CPU's A/D (Address/Data) bus. |
| Y(0:15) | I/O | Bidirectional Data port Y. Connected to the even path or even bank of memory. |
| Z(0:15) | I/O | Bidirectional Data port Z. Connected to the odd path or odd bank of memory. |
| LEXY | I | Latch Enable input for Y-Write Latch. The Y-Write Latch is open when LEXY is HIGH. Data from the X-port (CPU) is latched on the HIGH-to-LOW transition of LEXY |
| LEXZ | I | Latch Enable input for Z-Write Latch. The Z-Write Latch is open when LEXZ is HIGH. Data from the X-port (CPU) is latched on the HIGH-to-LOW transition of LEXZ. |
| LEYX | I | Latch Enable input for the Y-Read Latch. The Y-Read Latch is open when LEYX is HIGH. Data from the even path Y is latched on the HIGH-to-LOW transition of LEYX. |
| LEZX | I | Latch Enable input for the Z-Read Latch. The Z-Read Latch is open when LEZX is HIGH. Data from the odd path Z is latched on the HIGH-to-LOW transition of LEZX |
| PATH | I | Even/Odd Path Selection. When high, PATH enables data transfer between the X-Port and the Y-port (even path). When LOW, PATH enables data transfer between the X-Port and the Z-Port (odd path). |
| T/$\overline{R}$ | I | Transmit/Receive Data. When high, Port X is an input Port and either Port Y or Z is an output Port. When LOW, Port X is an output Port while Ports Y & Z are input Ports |
| $\overline{OEU}$ | I | Output Enable for Upper byte. When LOW, the Upper byte of data is transfered to the port specified by PATH in the direction specified by T/$\overline{R}$ . |
| $\overline{OEL}$ | I | Output Enable for Lower byte. When LOW, the Lower byte of data is transfered to the port specified by PATH in the direction specified by T/$\overline{R}$ . |

2527 tbl 02

## ABSOLUTE MAXIMUM RATINGS(1)

| Symbol | Rating | Com'l. | Mil. | Unit |
|---|---|---|---|---|
| $V_{TERM}$ | Terminal Voltage with Respect to GND | –0.5 to +7.0 | –0.5 to +7.0 | V |
| $T_A$ | Operating Temperature | 0 to +70 | –55 to +125 | °C |
| $T_{BIAS}$ | Temperature Under Bias | –55 to +125 | –65 to +135 | °C |
| $T_{STG}$ | Storage Temperature | –55 to +125 | –65 to +125 | °C |
| $P_T$ | Power Dissipation | 1.0 | 1.0 | W |
| $I_{OUT}$ | DC Output Current | 50 | 50 | mA |

**NOTE:** 2527 tbl 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## CAPACITANCE ($T_A$ = +25°C, F = 1.0MHz)

| Symbol | Parameter(1) | Conditions | Max. | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 0V | 8 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 0V | 12 | pF |

**NOTE:** 2527 tbl 04

1. This parameter is guaranteed by device characterization, but is not production tested.

## TRUTH TABLE

| Path | T/$\overline{R}$ | $\overline{OEU}$ | $\overline{OEL}$ | Functionality |
|---|---|---|---|---|
| L | L | L | L | Z→X (16-bits)–Read Z(1) |
| L | H | L | L | X→Z (16 bits)–Write Z(1) |
| H | L | L | L | Y→X (16-bits)–Read Y(2) |
| H | H | L | L | X→Y (16 bits)–Write Y(2) |
| X | X | H | H | All output buffers are disabled |
| X | X | H | L | Transfer of lower 8 bits (0:7) as per PATH & T/$\overline{R}$ |
| X | X | L | H | Transfer of upper 8 bits (8:15) as per PATH & T/$\overline{R}$ |

**NOTES:** 2527 tbl 01

1. For Z→X and X→Z transfers, Y-port output buffers are tristated.
2. For Y→X and X→Y transfers, Z-port output buffers are tristated.

## ARCHITECTURE OVERVIEW

The Bus Exchanger is used to service both read and write operations between the CPU and the dual memory busses. It includes independent data path elements for reads from and writes to each of the memory banks (Y and Z). Data flow control is managed by a simple set of control signals, analogous to a simple transceiver. In short, the Bus Exchanger allows bidirectional communication between ports X and Y and ports X and Z as illustrated in figure 1.

The data path elements for each port include:

**Read Latch**: Each of the memory ports Y and Z contains a transparent latch to capture the contents of the memory bus. Each latch features an independent latch enable.

**Write Latch**: Each memory port Y and Z contains an independent latch to capture data from the CPU bus during writes. Each memory port write latch features an independent latch enable, allowing write data to be directed to a specific memory port without disrupting the other memory port.

### Data Flow Control Signals

**T/$\overline{R}$** (Transmit/$\overline{\text{Receive}}$). This signal controls the direction of data transfer. A transmit is used for CPU writes, and a receive is used for read operations.

$\overline{OEU}$, $\overline{OEL}$ are the output enable control signals to select upper or lower bytes of all three ports.

**Path**: The path control signal is used to select between the even memory path Y and the odd memory path Z during read or write operations. Path selects the memory port to be connected to the CPU bus (X-port), and is independent of the latch enable signals. Thus, it is possible to transfer data from one memory port to the CPU bus (X) while capturing data from the other memory port.

## MEMORY READ OPERATIONS

### Latch Mode

In this mode the read operation consists of two stages. During the first stage, the data present at the memory port is captured by the read latch for that memory port. During a subsequent stage, data is brought from a selected memory port to the CPU A/D port X by using output enable control.

The read operation is selected by driving T/$\overline{R}$ LOW. The read is managed using the Path input to select the memory port (Y or Z); the LEYX/LEZX enable the data capture into the corresponding Read Latch.

In this way, memory interleaving can be performed. While data from one bank is output onto the CPU bus, data on the other bank is captured in the other memory port. In the next cycle, the Path input is changed, enabling the next data element onto the CPU bus, while the first bank is presented with a new data element.

### Transparent Mode

The Bus Exchanger may be used as a data transceiver by leaving all latches open or transparent.

### Memory Write Operations

Memory write operations also consist of two distinct stages. During one stage, the write data is captured into the selected memory port write latch. During a later stage, the memory is presented on the memory port bus

The write operation is selected by driving T/$\overline{R}$ HIGH. Writes are thus performed using the Path input to select the memory port (Y or Z). The LEXY/LEXZ capture data in the corresponding Write Latch.

Note that it is possible to utilize the bus exchanger's write resources as an additional write buffer, if desired; the CPU A/D bus can be freed up once the data has been captured by the Bus Exchanger.

## APPLICATIONS

### Use as Part of the R3051 Family ChipSet

Figure 2 shows the use of the Bus Exchanger in a typical R3051 based system.

In write transactions, the R3051 drives data on the CPU bus. The latch enables are held open through the entire write; thus, the bus exchanger is used like a transceiver. The appropriate LEXY/LEXZ signal is derived from ALE (Logic LOW- indicating that the processor is driving data) and the low order address bit. The rising edge of $\overline{Wr}$ from the CPU, ends the write operation.

During read transactions, the memory system is responsible for generating the input control signals to cause data to be captured at the memory ports. The memory controller is also responsible for acknowledging back to the CPU that the data is available, and causing the appropriate path to be selected.

The R3721 DRAM controller for the R3051 family uses the transparent latches of the read ports. The R3721 directly controls the inputs of the bus exchanger, during both reads and writes. Consult the R3721 data sheet for more information on these control signals.

### Use in a general 32-bit System

Figures 3 and 4 illustrate the use of the Bus Exchanger in a 32-bit microprocessor based system. Note the reduced pin count achieved with the Bus Exchanger.

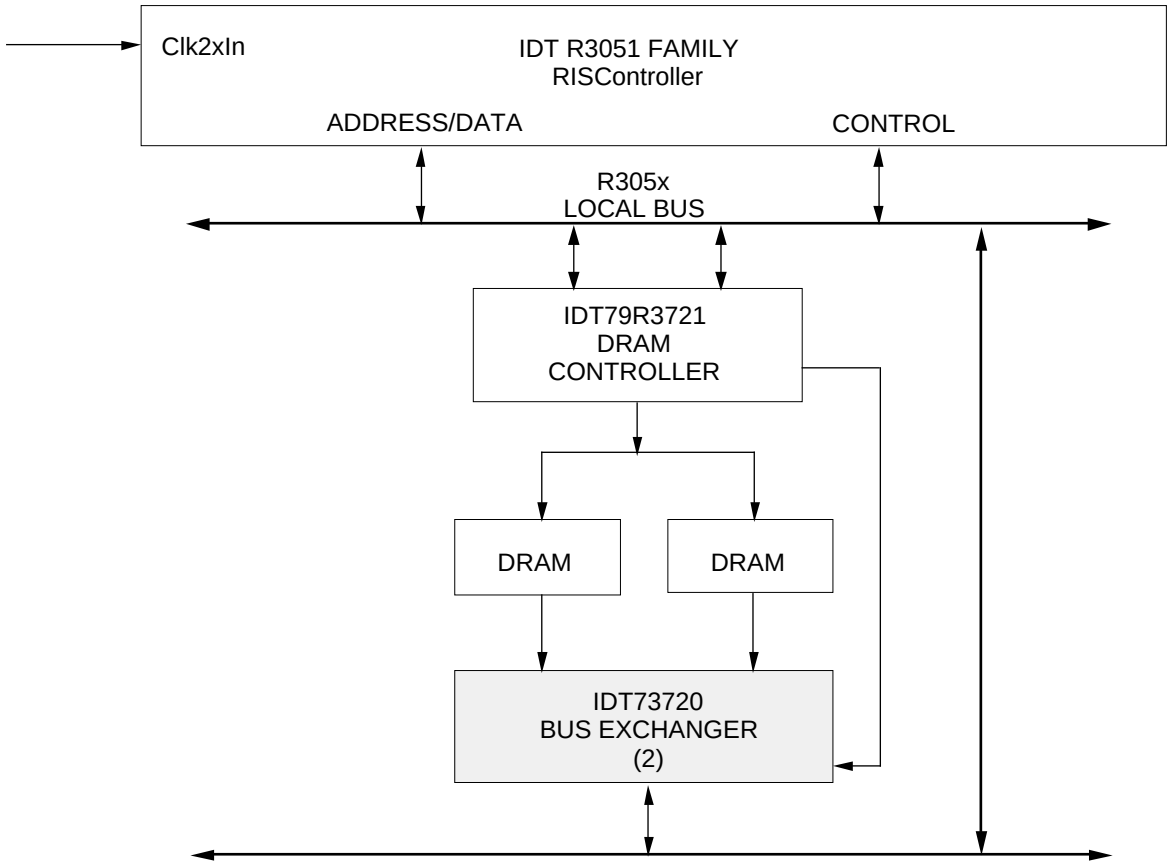
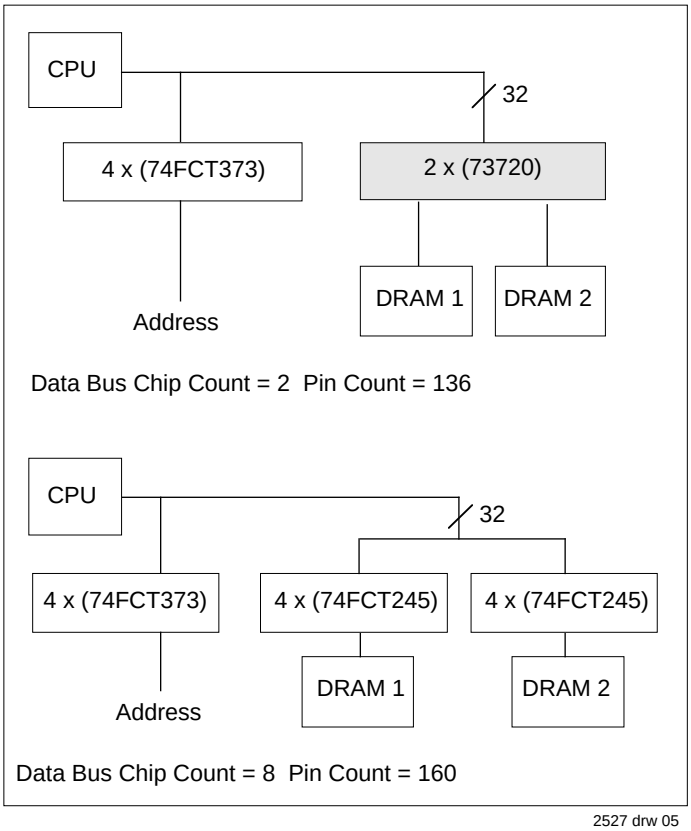


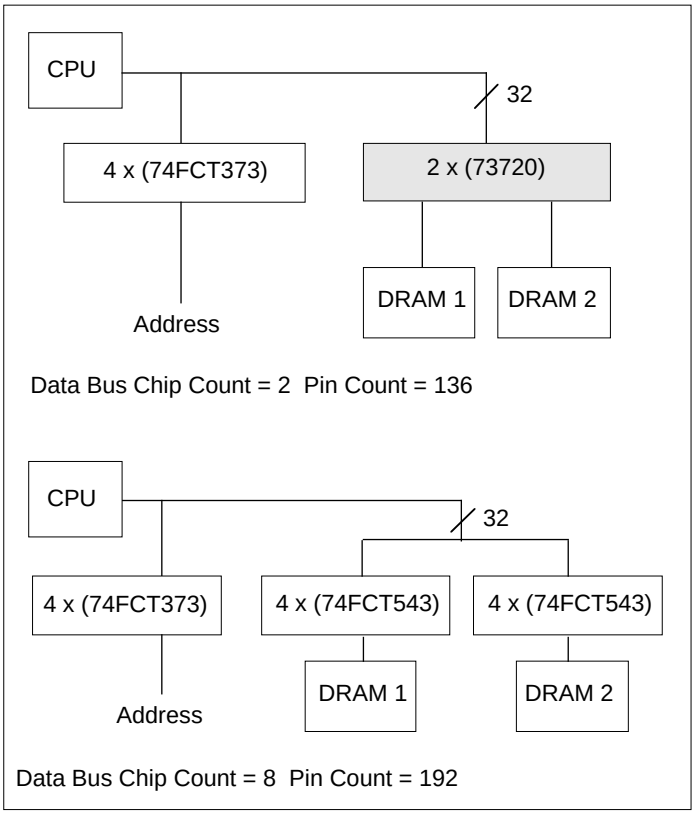

**Figure 2. Bus Exchanger Used in R3051 Family System**

2527 drw 04




2527 drw 05

**Figure 3. CPU System with Transparent Data Path (2-way Interleaving)**




2527 drw 06

**Figure 4. CPU System with Latched Data Path (2-way Interleaving)**

## DC ELECTRICAL CHARACTERISTICS ($V_{CC}$ = 5.0V ± 5%, $T_A$ = 0°C to +70°C)

| Symbol | Parameter | Test Conditions[1] | | Min. | Typ.[2] | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Level | | | 2.0 | — | — | V |
| $V_{IL}$ | Input LOW Level | | | — | — | 0.8 | V |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = Max., $V_{IH}$ = 2.7V | Inputs only | — | — | 5.0 | µA |
| | | | I/O pins | — | — | 5.0 | |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = Max., $V_{IL}$ = 0.5V | Inputs only | — | — | –5.0 | µA |
| | | | I/O pins | — | — | –5.0 | |
| $V_{IK}$ | Clamp Diode Voltage | $V_{CC}$ = Min., $I_{IN}$ = –18mA | | — | –0.7 | –1.2 | V |
| $I_{OS}$[3] | Short Circuit Current | $V_{CC}$ = Max., $V_O$ = GND | | –60 | — | –200 | mA |
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = Min., $V_{IN}$ = $V_{IH}$ or $V_{IL}$, $I_{OH}$ = –12mA | | 2.4 | 3.3 | — | V |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = Min., $V_{IN}$ = $V_{IH}$ or $V_{IL}$, $I_{OL}$ = 12mA | | — | 0.3 | 0.5 | V |
| $V_H$ | Input Hysteresis All inputs | $V_{CC}$ = 5V | | — | 200 | — | mV |
| $I_{CC}$ | Quiescent Power Supply Current | $V_{CC}$ = Max.<br>$V_{IN}$ = GND or $V_{CC}$ | | — | 0.2 | 1.5 | mA |
| $\Delta I_{CC}$ | Quiescent Power Supply Current | $V_{CC}$ = Max.<br>$V_{IN}$ =3.4 V[4] | | — | 0.5 | 2.0 | mA/ Input |
| $I_{CCD}$ | Dynamic Power Supply Current[5] | $V_{CC}$ = Max.<br>$V_{IN}$ = $V_{CC}$ or GND<br>Outputs Disabled<br>$\overline{OE}$ = $V_{CC}$<br>One Input Toggling<br>50 % Duty Cycle | | — | 0.25 | 0.5 | mA/ MHz |
| $I_C$ | Total Power Supply Current[6] | $V_{CC}$ = Max.<br>$V_{IN}$ = $V_{CC}$ or GND<br>Outputs Disabled<br>50 % Duty Cycle<br>$\overline{OE}$ = $V_{CC}$<br>fi = 10MHz<br>One Bit Toggling | | — | 2.7 | 6.5 | mA |

**NOTES:**

2527 tbl 05

1. For conditions shown as max. or min., use appropriate $V_{CC}$ value.
2. Typical values are at $V_{CC}$ = 5.0V, +25°C ambient.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Per TTL driven input ($V_{IN}$ = 3.4V); all other inputs at $V_{CC}$ or GND.
5. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   $I_{CC}$ = Quiescent Current
   $\Delta I_{CC}$ = Power Supply Current for a TTL High Input ($V_{IN}$ = 3.4V)
   $D_H$ = Duty Cycle for TTL Inputs High
   $N_T$ = Number of TTL Inputs at $D_H$
   $I_{CCD}$ = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   $f_{CP}$ = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   $f_i$ = Input Frequency
   $N_i$ = Number of Inputs at $f_i$
   All currents are in milliamps and all frequencies are in megaherz.

## AC TEST CONDITIONS

| | |
|---|---|
| Input Pulse Levels | GND to 3.0V |
| Input Rise/Fall Times | 5ns |
| Input Timing Reference Levels | 1.5V |
| Output Reference Levels | 1.5V |
| Output Load | See Figure 5 |

2527 tbl 06

## AC ELECTRICAL CHARACTERISTICS ($V_{CC}$ = 5.0V ± 5%, $T_A$ = 0° to +70°C)

| Symbol | Parameter | Test Conditions[1] | 73720A Min.[2] | 73720A Max. | 73720 Min.[2] | 73720 Max. | Units |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ $t_{PHL}$ | X to Y & X to Z Latches enabled | $C_L$ = 50pF $R_L$ = 500 Ohms | 2.0 | 6.0 | 2.0 | 7.5 | ns |
| $t_{PLH}$ $t_{PHL}$ | Y to X & Z to X Latches enabled | | 2.0 | 6.0 | 2.0 | 7.5 | ns |
| $t_{PLH}$ $t_{PHL}$ | Latch Enable to Y & Z Port LEXY to Y LEXZ to Z | | 2.0 | 7.0 | 2.0 | 8.5 | ns |
| $t_{PLH}$ $t_{PHL}$ | Latch Enable to X LEYX to X LEZX to X | | 2.0 | 7.0 | 2.0 | 8.5 | ns |
| $t_{PLH}$ $t_{PHL}$ | Path to X Port Propagation Delay | | 2.0 | 7.0 | 2.0 | 8.5 | ns |
| $t_{HZ}$ $t_{LZ}$ | Y & Z Port Disable Time (T/$\overline{R}$, PATH, $\overline{OEU}$, $\overline{OEL}$)[3] | | 2.0 | 8.5 | 2.0 | 9.5 | ns |
| $t_{ZH}$ $t_{ZL}$ | Y & Z Port Enable Time (T/$\overline{R}$, PATH, $\overline{OEU}$, $\overline{OEL}$)[3] | | 2.0 | 9.5 | 2.0 | 10.5 | ns |
| $t_{HZ}$ $t_{LZ}$ | X-Port DisableTime (T/$\overline{R}$, $\overline{OEU}$, $\overline{OEL}$)[3] | | 2.0 | 8.5 | 2.0 | 9.5 | ns |
| $t_{ZH}$ $t_{ZL}$ | X-Port Enable Time (T/$\overline{R}$, $\overline{OEU}$, $\overline{OEL}$)[3] | | 2.0 | 9.5 | 2.0 | 10.5 | ns |
| $t_{SU}$ | Port to LE Set-up time | | 2.0 | — | 2.0 | — | ns |
| $t_H$ | Port to LE Hold time | | 1.5 | — | 1.5 | — | ns |
| $t_W$ | LE Pulse Width, HIGH or LOW[2] | | 3 | — | 4 | — | ns |

**NOTES:**

2527 tbl 07

1. All timings are referenced to 1.5 V.
2. Minimum Delay Times, Enable Times, Disable Times and Pulse Width are guaranteed by design, but not tested.
3. Bus turnaround times are guaranteed by design, but not tested. (T/$\overline{R}$ enable/disable times).

## TEST CIRCUITS AND WAVEFORMS

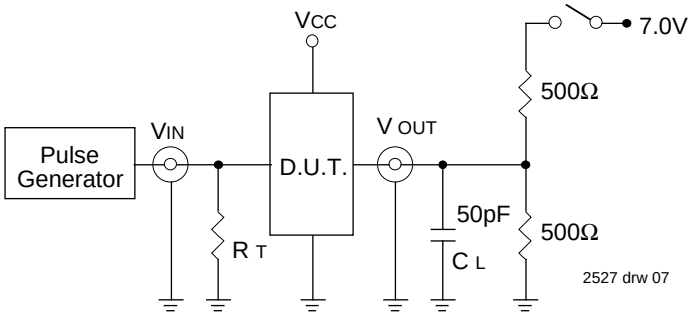



**Figure 5. Test Circuit for all outputs**

## SWITCH POSITION

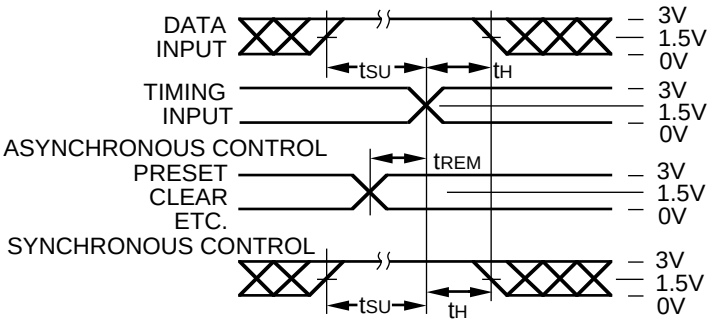
| Test | Switch |
|---|---|
| Disable LOW<br>Enable LOW | Closed |
| All Other Tests | Open |

2527 tbl 08

**DEFINITIONS:**

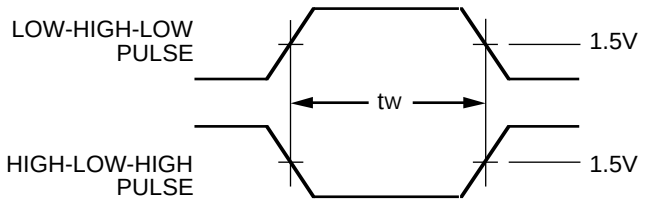
$C_L$ = Load capacitance: includes jig and probe capacitance.
$R_T$ = Termination resistance: should be equal to $Z_{OUT}$ of the Pulse Generator.

## SET-UP, HOLD AND RELEASE TIMES



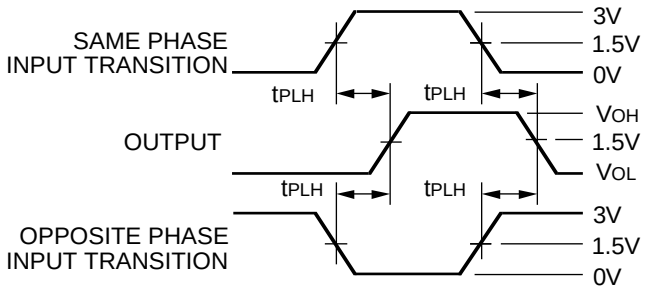

2527 drw 08

## PULSE WIDTH



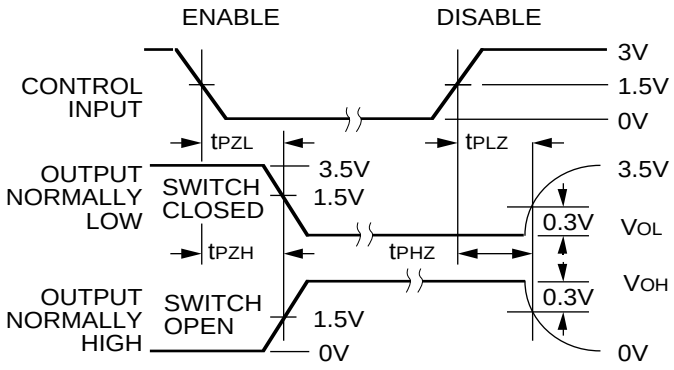

2527 drw 09

## PROPAGATION DELAY




2527 drw 10

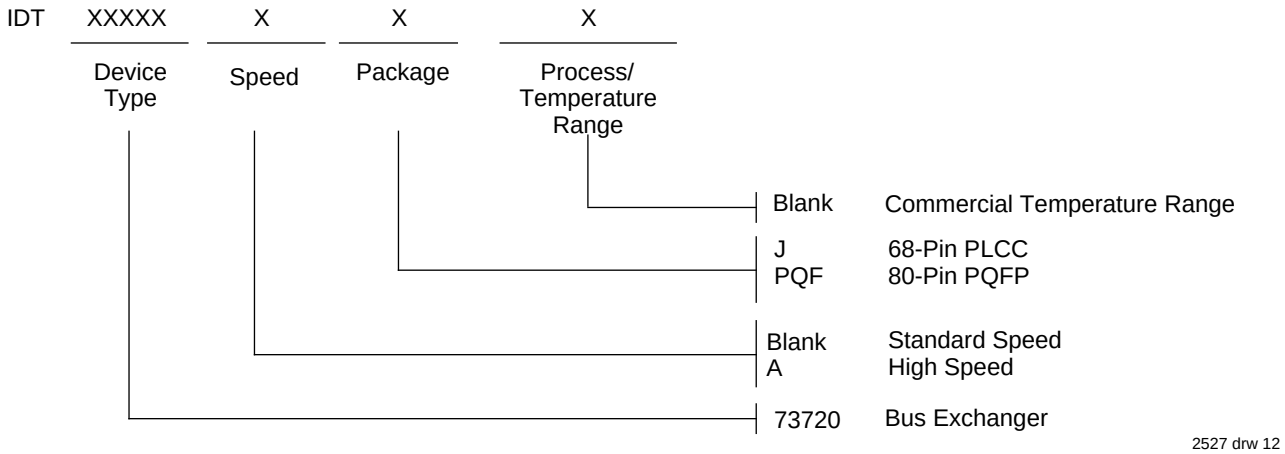
## ENABLE AND DISABLE TIMES




2527 drw 11

**NOTES:**
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; ZO ≤ 50Ω; tF ≤ 2.5ns; tR ≤ 2.5ns.

## ORDERING INFORMATION




2527 drw 12

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