



3.3V CMOS 32-BIT BUS TRANSCEIVER WITH 3-STATE OUTPUTS AND BUS-HOLD

IDT74ALVCH32245

FEATURES:

- 0.5 MICRON CMOS Technology
- Typical $t_{sk(o)}$ (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- $V_{cc} = 3.3V \pm 0.3V$, Normal Range
- $V_{cc} = 2.7V$ to $3.6V$, Extended Range
- $V_{cc} = 2.5V \pm 0.2V$
- CMOS power levels (0.4 μ W typ. static)
- Rail-to-Rail output swing for increased noise margin
- Available in 96-ball LFBGA package

DRIVE FEATURES:

- High Output Drivers: $\pm 24mA$
- Suitable for Heavy Loads

APPLICATIONS:

- 3.3V high speed systems
- 3.3V and lower voltage computing systems

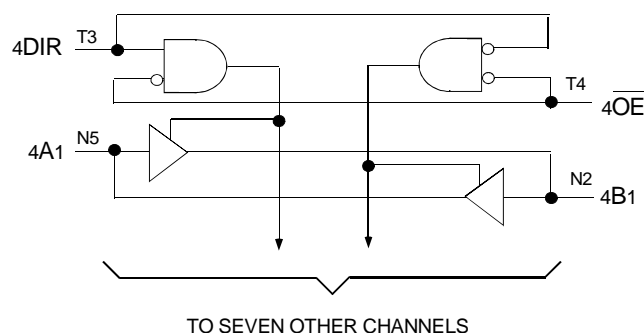
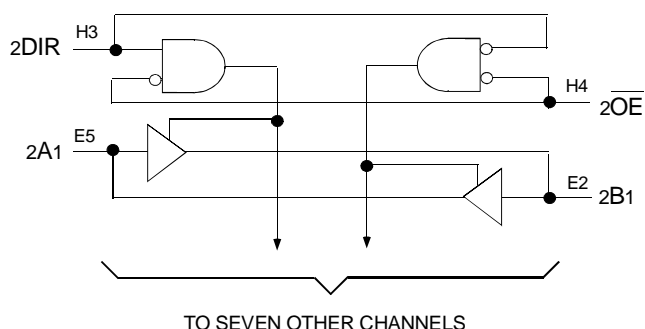
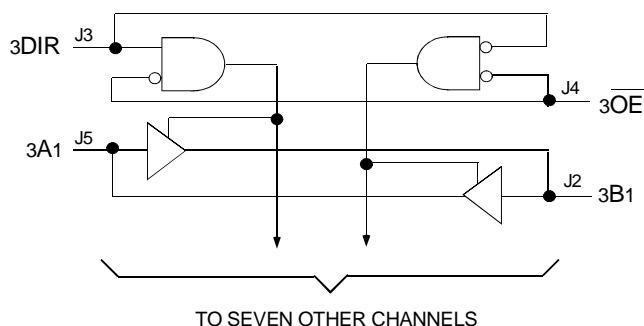
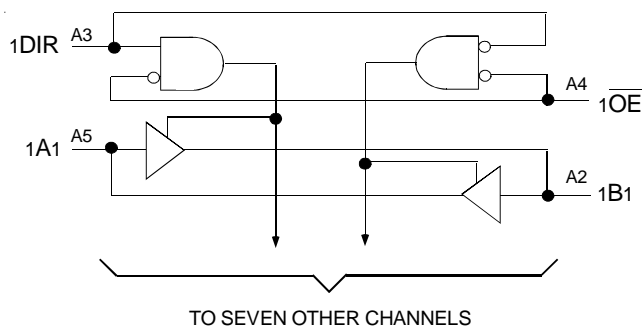
DESCRIPTION:

This 32-bit bus transceiver is built using advanced dual metal CMOS technology. This high-speed, low power transceiver is ideal for asynchronous communication between two busses (A and B). The Direction and Output Enable controls are designed to operate the device as either four independent 8-bit transceivers or one 32-bit transceiver. The direction control pins (DIR) control the direction of data flow. The output enable pins (\overline{OE}) override the direction control and disable both ports. All inputs are designed with hysteresis for improved noise margin.

The ALVCH32245 has been designed with a $\pm 24mA$ output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

The ALVCH32245 has "bus-hold" which retains the inputs' last state whenever the input bus goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistors.

FUNCTIONAL BLOCK DIAGRAM



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INDUSTRIAL TEMPERATURE RANGE

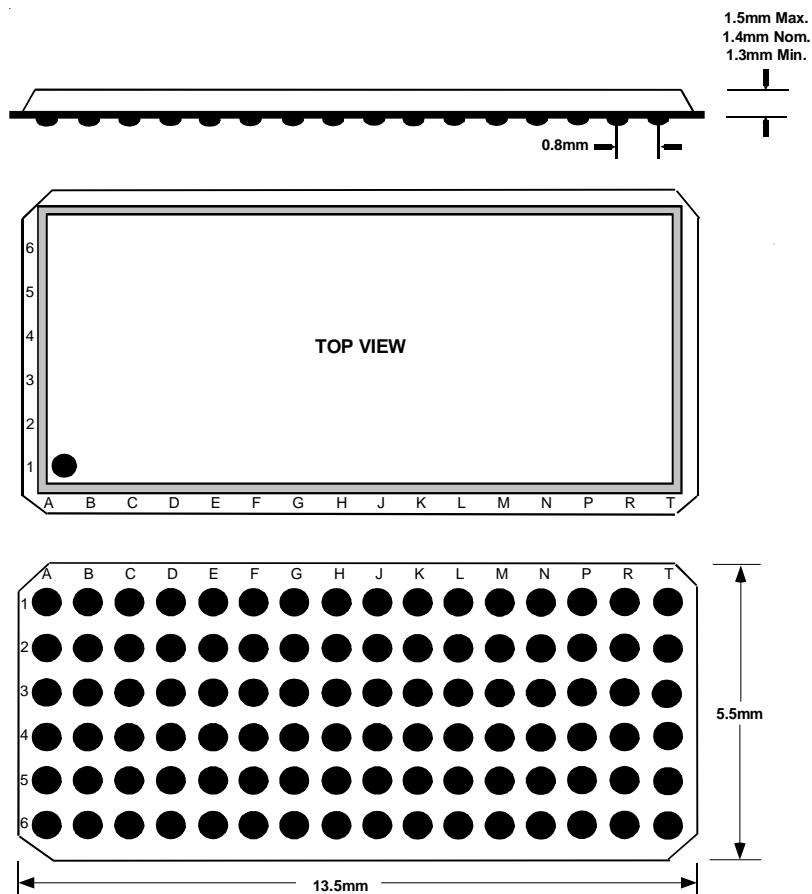
FEBRUARY 2000

PIN CONFIGURATION

| | | | | | | | | | | | | | | | | |
|---|-------------------|-----|-----|-----|-----|-----|-----|-------------------|-------------------|-----|-----|-----|-----|-----|-----|-------------------|
| 6 | 1A2 | 1A4 | 1A6 | 1A8 | 2A2 | 2A4 | 2A6 | 2A7 | 3A2 | 3A4 | 3A6 | 3A8 | 4A2 | 4A4 | 4A6 | 4A7 |
| 5 | 1A1 | 1A3 | 1A5 | 1A7 | 2A1 | 2A3 | 2A5 | 2A8 | 3A1 | 3A3 | 3A5 | 3A7 | 4A1 | 4A3 | 4A5 | 4A8 |
| 4 | 1 \overline{OE} | GND | VCC | GND | GND | VCC | GND | 2 \overline{OE} | 3 \overline{OE} | GND | VCC | GND | GND | VCC | GND | 4 \overline{OE} |
| 3 | 1DIR | GND | VCC | GND | GND | VCC | GND | 2DIR | 3DIR | GND | VCC | GND | GND | VCC | GND | 4DIR |
| 2 | 1B1 | 1B3 | 1B5 | 1B7 | 2B1 | 2B3 | 2B5 | 2B8 | 3B1 | 3B3 | 3B5 | 3B7 | 4B1 | 4B3 | 4B5 | 4B8 |
| 1 | 1B2 | 1B4 | 1B6 | 1B8 | 2B2 | 2B4 | 2B6 | 2B7 | 3B2 | 3B4 | 3B6 | 3B8 | 4B2 | 4B4 | 4B6 | 4B7 |
| | A | B | C | D | E | F | G | H | J | K | L | M | N | P | R | T |

LFBGA
TOPVIEW

96 BALL LFBGA PACKAGE ATTRIBUTES



ABSOLUTE MAXIMUM RATINGS⁽¹⁾

| Symbol | Description | Max | Unit |
|------------------------------------|--|------------------------------|------|
| V _{TERM} ⁽²⁾ | Terminal Voltage with Respect to GND | -0.5 to +4.6 | V |
| V _{TERM} ⁽³⁾ | Terminal Voltage with Respect to GND | -0.5 to V _{CC} +0.5 | V |
| T _{STG} | Storage Temperature | -65 to +150 | °C |
| I _{OUT} | DC Output Current | -50 to +50 | mA |
| I _{IK} | Continuous Clamp Current, V _i < 0 or V _i > V _{CC} | ±50 | mA |
| I _{OK} | Continuous Clamp Current, V _o < 0 | -50 | mA |
| I _{CC} I _{SS} | Continuous Current through each V _{CC} or GND | ±100 | mA |

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{CC} terminals.
- All terminals except V_{CC}.

CAPACITANCE (T_A = +25°C, F = 1.0MHz)

| Symbol | Parameter ⁽¹⁾ | Conditions | Typ. | Max. | Unit |
|------------------|--------------------------|-----------------------|------|------|------|
| C _{IN} | Input Capacitance | V _{IN} = 0V | 5 | 7 | pF |
| C _{OUT} | Output Capacitance | V _{OUT} = 0V | 7 | 9 | pF |
| C _{I/O} | I/O Port Capacitance | V _{IN} = 0V | 7 | 9 | pF |

NOTE:

- As applicable to the device type.

PIN DESCRIPTION

| Pin Names | Description |
|------------------|---|
| \overline{xOE} | Output Enable Inputs (Active LOW) |
| xDIR | Direction Control Inputs |
| xAx | Side A Inputs or 3-State Outputs ⁽¹⁾ |
| xBx | Side B Inputs or 3-State Outputs ⁽¹⁾ |

NOTE:

- These pins have "Bus-Hold". All other pins are standard inputs, outputs, or I/Os.

FUNCTION TABLE (EACH 8-BIT SECTION)⁽¹⁾

| Inputs | | Outputs |
|-------------------|------|---------------------|
| x \overline{OE} | xDIR | |
| L | L | Bus B Data to Bus A |
| L | H | Bus A Data to Bus B |
| H | X | High Z State |

NOTE:

- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High Impedance

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$

| Symbol | Parameter | Test Conditions | | Min. | Typ. ⁽¹⁾ | Max. | Unit |
|--|--|---|----------------------------------|------|---------------------|------|------|
| V _{IH} | Input HIGH Voltage Level | V _{CC} = 2.3V to 2.7V | | 1.7 | — | — | V |
| | | V _{CC} = 2.7V to 3.6V | | 2 | — | — | |
| V _{IL} | Input LOW Voltage Level | V _{CC} = 2.3V to 2.7V | | — | — | 0.7 | V |
| | | V _{CC} = 2.7V to 3.6V | | — | — | 0.8 | |
| I _{IH} | Input HIGH Current | V _{CC} = 3.6V | V _I = V _{CC} | — | — | ±5 | μA |
| I _{IL} | Input LOW Current | V _{CC} = 3.6V | V _I = GND | — | — | ±5 | μA |
| I _{OZH} I _{OZL} | High Impedance Output Current (3-State Output pins) | V _{CC} = 3.6V | V _O = V _{CC} | — | — | ±10 | μA |
| | | | V _O = GND | — | — | ±10 | |
| V _{IK} | Clamp Diode Voltage | V _{CC} = 2.3V, I _{IN} = -18mA | | — | -0.7 | -1.2 | V |
| V _H | Input Hysteresis | V _{CC} = 3.3V | | — | 100 | — | mV |
| I _{CC1} I _{CC2} I _{CC3} | Quiescent Power Supply Current | V _{CC} = 3.6V V _{IN} = GND or V _{CC} | | — | 0.1 | 40 | μA |
| ΔI _{CC} | Quiescent Power Supply Current Variation | One input at V _{CC} - 0.6V, other inputs at V _{CC} or GND | | — | — | 750 | μA |

NOTE:

1. Typical values are at V_{CC} = 3.3V, +25°C ambient.

BUS-HOLD CHARACTERISTICS

| Symbol | Parameter ⁽¹⁾ | Test Conditions | | Min. | Typ. ⁽²⁾ | Max. | Unit |
|--|----------------------------------|------------------------|----------------------------|------|---------------------|------|------|
| I _{BHH} I _{BHL} | Bus-Hold Input Sustain Current | V _{CC} = 3V | V _I = 2V | -75 | — | — | μA |
| | | | V _I = 0.8V | 75 | — | — | |
| I _{BHH} I _{BHL} | Bus-Hold Input Sustain Current | V _{CC} = 2.3V | V _I = 1.7V | -45 | — | — | μA |
| | | | V _I = 0.7V | 45 | — | — | |
| I _{BHHO} I _{BHLO} | Bus-Hold Input Overdrive Current | V _{CC} = 3.6V | V _I = 0 to 3.6V | — | — | ±500 | μA |

NOTES:

1. Pins with Bus-Hold are identified in the pin description.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.

OUTPUT DRIVE CHARACTERISTICS

| Symbol | Parameter | Test Conditions ⁽¹⁾ | | Min. | Max. | Unit |
|--------|---------------------|--------------------------------|---------------|-----------|------|------|
| VOH | Output HIGH Voltage | VCC = 2.3V to 3.6V | IOH = - 0.1mA | VCC - 0.2 | — | V |
| | | VCC = 2.3V | IOH = - 6mA | 2 | — | |
| | | VCC = 2.3V | IOH = - 12mA | 1.7 | — | |
| | | VCC = 2.7V | | 2.2 | — | |
| | | VCC = 3V | | 2.4 | — | |
| | | VCC = 3V | IOH = - 24mA | 2 | — | |
| VOL | Output LOW Voltage | VCC = 2.3V to 3.6V | IOL = 0.1mA | — | 0.2 | V |
| | | VCC = 2.3V | IOL = 6mA | — | 0.4 | |
| | | | IOL = 12mA | — | 0.7 | |
| | | VCC = 2.7V | IOL = 12mA | — | 0.4 | |
| | | VCC = 3V | IOL = 24mA | — | 0.55 | |

NOTE:
1. VIH and VIL must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate VCC range. TA = - 40°C to + 85°C.

OPERATING CHARACTERISTICS, TA = 25°C

| Symbol | Parameter | Test Conditions | VCC = 2.5V ± 0.2V | VCC = 3.3V ± 0.3V | Unit |
|--------|---|---------------------|-------------------|-------------------|------|
| | | | Typical | Typical | |
| CPD | Power Dissipation Capacitance per Driver Outputs enabled | CL = 0pF, f = 10Mhz | 44 | 58 | pF |
| CPD | Power Dissipation Capacitance per Driver Outputs disabled | | 8 | 10 | |

SWITCHING CHARACTERISTICS⁽¹⁾

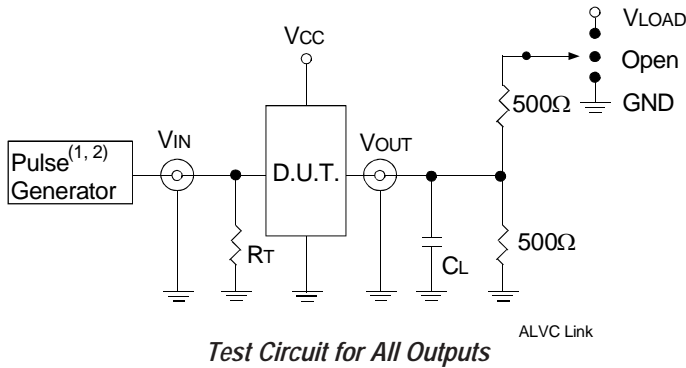
| Symbol | Parameter | VCC = 2.5V ± 0.2V | | VCC = 2.7V | | VCC = 3.3V ± 0.3V | | Unit |
|--------|--------------------------------|-------------------|------|------------|------|-------------------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| tPLH | Propagation Delay | 1 | 3.7 | — | 3.6 | 1 | 3 | ns |
| tPHL | xAx to xBx or xBx to xAx | | | | | | | |
| tPZH | Output Enable Time | 1 | 5.7 | — | 5.4 | 1 | 4.4 | ns |
| tPZL | \overline{xOE} to xAx to xBx | | | | | | | |
| tPHZ | Output Disable Time | 1 | 5.2 | — | 4.6 | 1 | 4.1 | ns |
| tPLZ | \overline{xOE} to xAx to xBx | | | | | | | |
| tSK(O) | Output Skew ⁽²⁾ | — | — | — | — | — | 500 | ps |

NOTES:
1. See TEST CIRCUITS AND WAVEFORMS. TA = - 40°C to + 85°C.
2. Skew between any two outputs of the same package and switching in the same direction.

TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

| Symbol | V _{CC} ⁽¹⁾ = 3.3V ± 0.3V | V _{CC} ⁽¹⁾ = 2.7V | V _{CC} ⁽²⁾ = 2.5V ± 0.2V | Unit |
|-------------------|--|---------------------------------------|--|------|
| V _{LOAD} | 6 | 6 | 2 x V _{CC} | V |
| V _{IH} | 2.7 | 2.7 | V _{CC} | V |
| V _T | 1.5 | 1.5 | V _{CC} / 2 | V |
| V _{LZ} | 300 | 300 | 150 | mV |
| V _{HZ} | 300 | 300 | 150 | mV |
| C _L | 50 | 50 | 30 | pF |



DEFINITIONS:

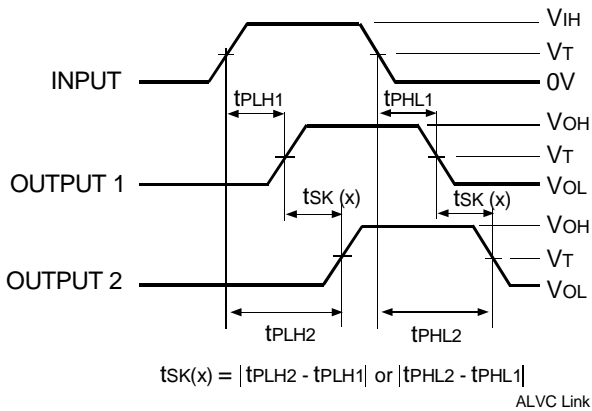
C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTES:

1. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_r ≤ 2.5ns; t_r ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_r ≤ 2ns; t_r ≤ 2ns.

SWITCH POSITION

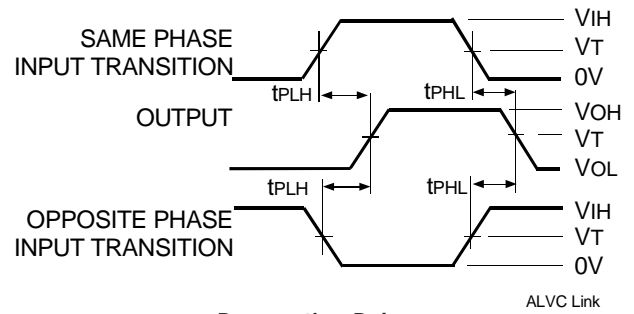
| Test | Switch |
|---|-------------------|
| Open Drain Disable Low Enable Low | V _{LOAD} |
| Disable High Enable High | GND |
| All Other Tests | Open |



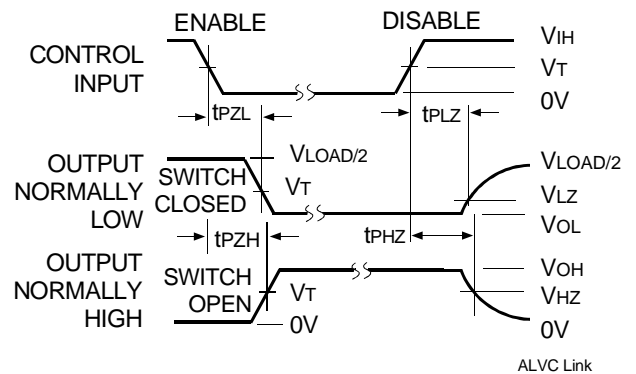
Output Skew - t_{SK}(x)

NOTES:

1. For t_{SK}(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For t_{SK}(b) OUTPUT1 and OUTPUT2 are in the same bank.



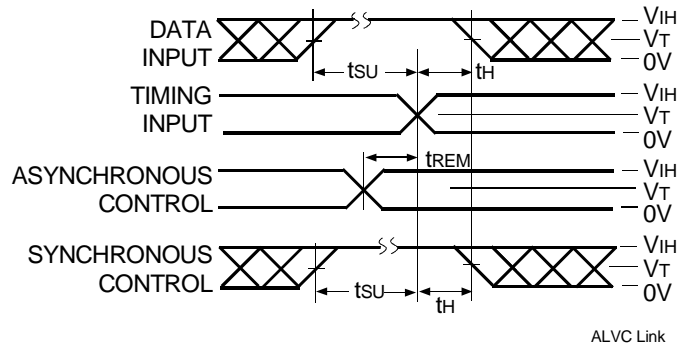
Propagation Delay



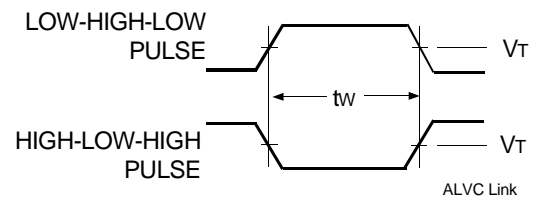
Enable and Disable Times

NOTE:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

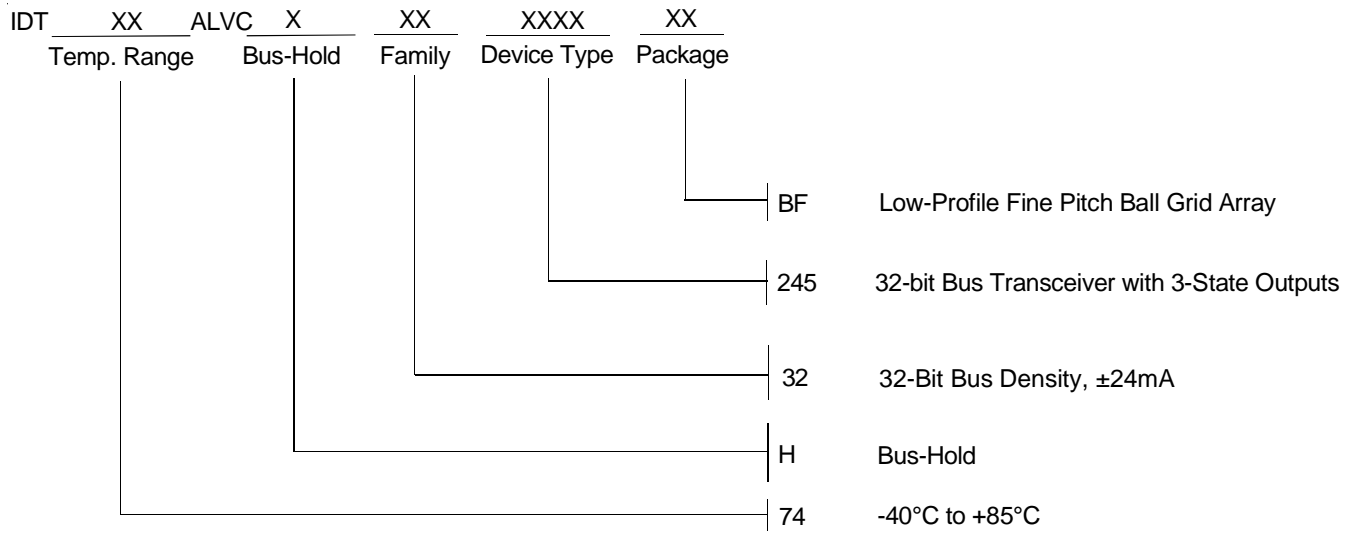


Set-up, Hold, and Release Times



Pulse Width

ORDERING INFORMATION



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