



# FAST CMOS SYNCHRONOUS PRESETTABLE BINARY COUNTER

**IDT74FCT161AT/CT**

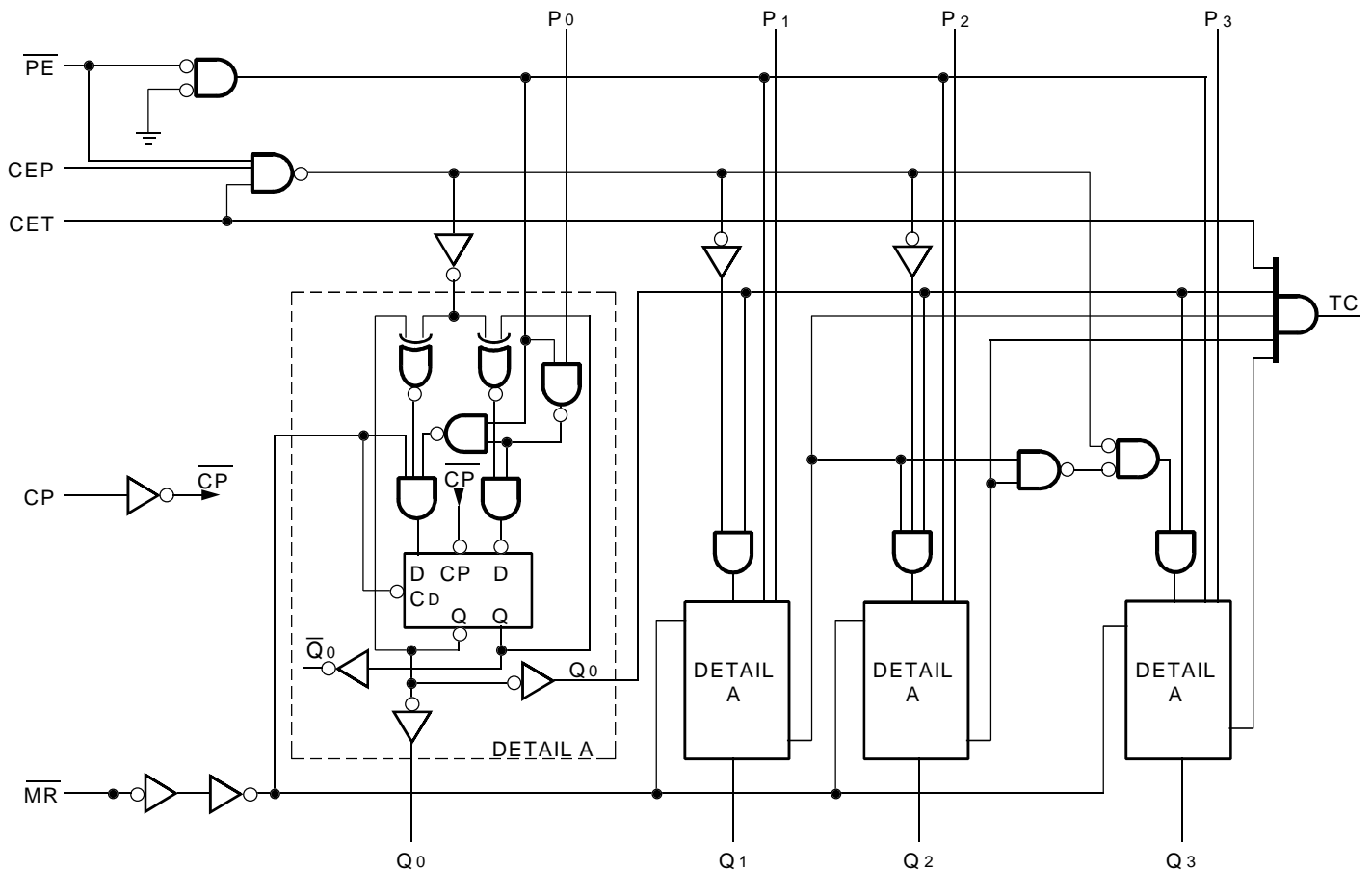
## FEATURES:

- A and C grades
- Low input and output  $\leq 1\mu\text{A}$  (max.)
- CMOS power levels
- True TTL input and output compatibility:
  - $V_{OH} = 3.3V$  (typ.)
  - $V_{OL} = 0.3V$  (typ.)
- High Drive outputs (-15mA  $I_{OH}$ , 48mA  $I_{OL}$ )
- Meets or exceeds JEDEC standard 18 specifications
- Power off disable outputs permit "live insertion"
- Available in SOIC and QSOP packages

## DESCRIPTION:

The IDT74FCT161T is a high-speed synchronous modulo-16 binary counter built using an advanced dual metal CMOS technology. It is synchronously presettable for application in programmable dividers and has two types of count enable inputs plus a terminal count output for versatility in forming synchronous multi-stage counters. The IDT74FCT161T has asynchronous Master Reset inputs that override all other inputs and force the outputs low.

## FUNCTIONAL BLOCK DIAGRAM

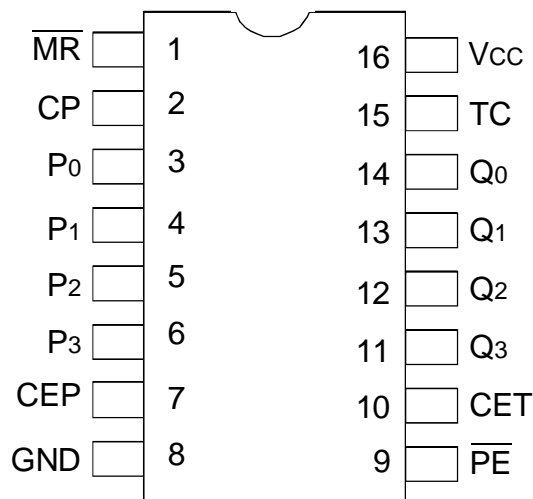


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**INDUSTRIAL TEMPERATURE RANGE**

**MARCH 2002**

## PIN CONFIGURATION



SOIC/ QSOP  
TOP VIEW

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Description	Max	Unit
V <sub>TERM</sub> <sup>(2)</sup>	Terminal Voltage with Respect to GND	-0.5 to +7	V
V <sub>TERM</sub> <sup>(3)</sup>	Terminal Voltage with Respect to GND	-0.5 to V <sub>CC</sub> +0.5	V
T <sub>STG</sub>	Storage Temperature	-65 to +150	°C
I <sub>OUT</sub>	DC Output Current	-60 to +120	mA

### NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V<sub>CC</sub> by +0.5V unless otherwise noted.
- Inputs and V<sub>CC</sub> terminals only.
- Output and I/O terminals only.

## CAPACITANCE (T<sub>A</sub> = +25°C, F = 1.0MHz)

Symbol	Parameter <sup>(1)</sup>	Conditions	Typ.	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	6	10	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0V	8	12	pF

### NOTE:

- This parameter is measured at characterization but not tested.

## PIN DESCRIPTION

Pin Names	Description
CEP	Count Enable Parallel Input
CET	Count Enable Trickle Input
CP	Clock Pulse Input (Active Rising Edge)
$\overline{MR}$	Asynchronous Master Reset Input (Active LOW)
P <sub>0-3</sub>	Parallel Data Inputs
$\overline{PE}$	Parallel Enable Input (Active LOW)
Q <sub>0-3</sub>	Flip-Flop Outputs
TC	Terminal Count Output

## FUNCTION TABLE<sup>(1)</sup>

$\overline{PE}$	CET	CEP	Action on the Rising Clock Edge(s)
X	X	X	Reset (Clear)
L	X	X	Load (P <sub>x</sub> →Q <sub>x</sub> )
H	H	H	Count (Increment)
H	L	X	No Change (Hold)
H	X	L	No Change (Hold)

### NOTE:

- H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Don't Care

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Industrial:  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 5\%$

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Typ. <sup>(2)</sup>	Max.	Unit
$V_{IH}$	Input HIGH Level	Guaranteed Logic HIGH Level <sup>(5)</sup>		2V	—	—	V
$V_{IL}$	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
$I_{IH}$	Input HIGH Current <sup>(4)</sup>	$V_{CC} = \text{Max.}$	$V_I = 2.7\text{V}$	—	—	$\pm 1$	$\mu\text{A}$
$I_{IL}$	Input LOW Current <sup>(4)</sup>	$V_{CC} = \text{Max.}$	$V_I = 0.5\text{V}$	—	—	$\pm 1$	$\mu\text{A}$
$I_I$	Input HIGH Current <sup>(4)</sup>	$V_{CC} = \text{Max.}, V_I = V_{CC} (\text{Max.})$		—	—	$\pm 1$	$\mu\text{A}$
$V_{IK}$	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_N = -18\text{mA}$		—	-0.7	-1.2	V
$I_{OS}$	Short Circuit Current	$V_{CC} = \text{Max.}^{(3)}, V_O = \text{GND}$		-60	-120	-225	mA
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -8\text{mA}$	2.4	3.3	—	V
			$I_{OH} = -15\text{mA}$	2	3	—	
$V_{OL}$	Output LOW Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 48\text{mA}$	—	0.3	0.5	V
$V_H$	Input Hysteresis	—		—	200	—	mV
$I_{CC}$	Quiescent Power	$V_{CC} = \text{Max.}$		—	0.01	1	mA
	Supply Current	$V_{IN} = \text{GND}$ or $V_{CC}$					

### NOTES:

1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at  $V_{CC} = 5.0\text{V}$ ,  $+25^{\circ}\text{C}$  ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. The test limit for this parameter is  $\pm 5\mu\text{A}$  at  $T_A = -55^{\circ}\text{C}$ .
5. Clock pin requires a minimum  $V_{IH}$  of 2.5V.

## POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions <sup>(1)</sup>	Min.	Typ. <sup>(2)</sup>	Max.	Unit	
$\Delta I_{CC}$	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(3)}$	—	0.5	2	mA	
$I_{CCD}$	Dynamic Power Supply Current <sup>(4)</sup>	$V_{CC} = \text{Max.}$ , Outputs Open Load Mode $CEP = CET = \overline{PE} = GND$ $\overline{MR} = V_{CC}$ One Input Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = GND$	—	0.15	0.25	mA/ MHz
$I_C$	Total Power Supply Current <sup>(6)</sup>	$V_{CC} = \text{Max.}$ , Outputs Open Load Mode $f_{CP} = 10\text{MHz}$ 50% Duty Cycle $CEP = CET = \overline{PE} = GND$ $\overline{MR} = V_{CC}$ One Bit Toggling at $f_i = 5\text{MHz}$ 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = GND$	—	1.5	3.5	mA
			$V_{IN} = 3.4V$ $V_{IN} = GND$	—	2	5.5	
		$V_{CC} = \text{Max.}$ , Outputs Open Load Mode $f_{CP} = 10\text{MHz}$ 50% Duty Cycle $CEP = CET = \overline{PE} = GND$ $\overline{MR} = V_{CC}$ Four Bits Toggling at $f_i = 5\text{MHz}$ 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = GND$	—	3.8	7.3 <sup>(5)</sup>	
			$V_{IN} = 3.4V$ $V_{IN} = GND$	—	5	12.3 <sup>(5)</sup>	

### NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at  $V_{CC} = 5.0V$ ,  $+25^\circ\text{C}$  ambient.
- Per TTL driven input ( $V_{IN} = 3.4V$ ). All other inputs at  $V_{CC}$  or  $GND$ .
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the  $I_{CC}$  formula. These limits are guaranteed but not tested.
- $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$   
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$   
 $I_{CC}$  = Quiescent Current  
 $\Delta I_{CC}$  = Power Supply Current for a TTL High Input ( $V_{IN} = 3.4V$ )  
 $D_H$  = Duty Cycle for TTL Inputs High  
 $N_T$  = Number of TTL Inputs at  $D_H$   
 $I_{CCD}$  = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)  
 $f_{CP}$  = Clock Frequency for Register Devices (Zero for Non-Register Devices)  
 $f_i$  = Input Frequency  
 $N_i$  = Number of Inputs at  $f_i$   
 All currents are in milliamps and all frequencies are in megahertz.

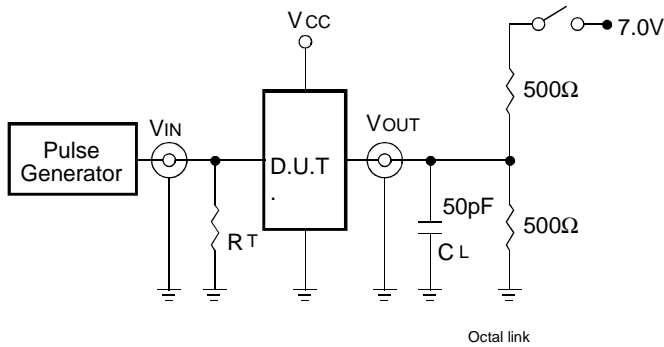
## SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition <sup>(1)</sup>	IDT74FCT161AT		IDT74FCT161CT		Unit
			Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay CP to Qx (P <sub>E</sub> Input HIGH)	C <sub>L</sub> = 50pF R <sub>L</sub> = 500Ω	2	7.2	2	5.8	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay CP to Qx (P <sub>E</sub> Input LOW)		2	6.2	2	5.8	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay CP to TC		2	9.8	2	7.4	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay CET to TC		1.5	5.5	1.5	5.2	ns
t <sub>PHL</sub>	Propagation Delay MR to Qx		2	8.5	2	6	ns
t <sub>PHL</sub>	Propagation Delay MR to TC		2	7.5	2	7	ns
t <sub>SU</sub>	Set-up Time, HIGH or LOW, P <sub>x</sub> to CP		4	—	4	—	ns
t <sub>H</sub>	Hold Time, HIGH or LOW, P <sub>x</sub> to CP		1.5	—	1.5	—	ns
t <sub>SU</sub>	Set-up Time, HIGH or LOW, P <sub>E</sub> or S <sub>R</sub> to CP		9.5	—	9.5	—	ns
t <sub>H</sub>	Hold Time, HIGH or LOW, P <sub>E</sub> or S <sub>R</sub> to CP		1.5	—	1.5	—	ns
t <sub>SU</sub>	Set-up Time, HIGH or LOW, CEP or CET to CP		9.5	—	9.5	—	ns
t <sub>H</sub>	Hold Time, HIGH or LOW, CEP or CET to CP		0	—	0	—	ns
t <sub>w</sub>	Clock Pulse, Width (Load) HIGH or LOW		4 <sup>(3)</sup>	—	4 <sup>(3)</sup>	—	ns
t <sub>w</sub>	Clock Pulse, Width (Count) HIGH or LOW		6	—	6	—	ns
t <sub>PHL</sub>	MR Pulse Width LOW		4 <sup>(3)</sup>	—	4 <sup>(3)</sup>	—	ns
t <sub>PHL</sub>	Recovery Time MR to CP		5	—	5	—	ns

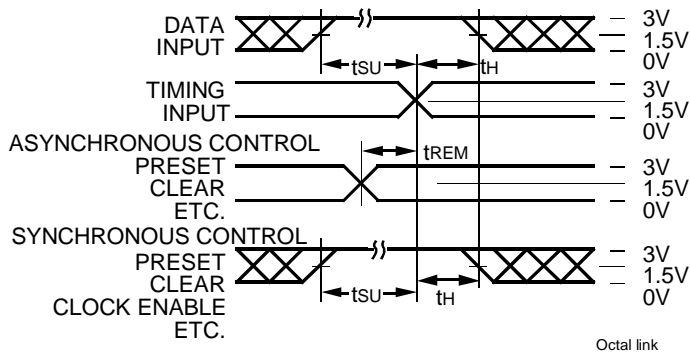
**NOTES:**

1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This limit is guaranteed but not tested.

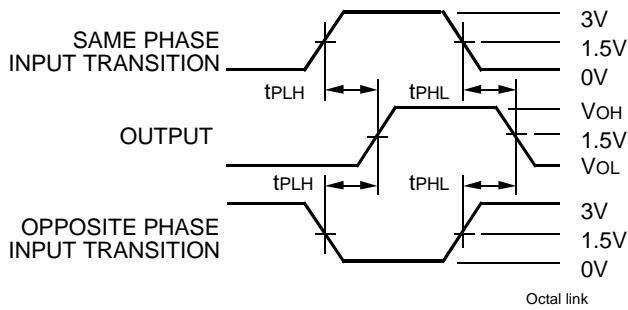
### TEST CIRCUITS AND WAVEFORMS



Test Circuits for All Outputs



Set-Up, Hold, and Release Times



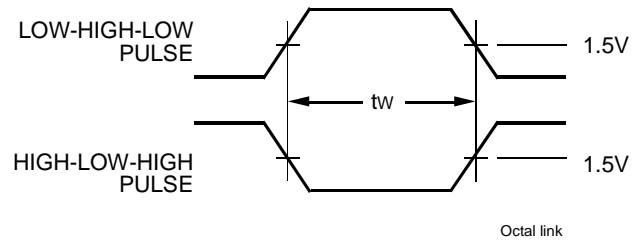
Propagation Delay

### SWITCH POSITION

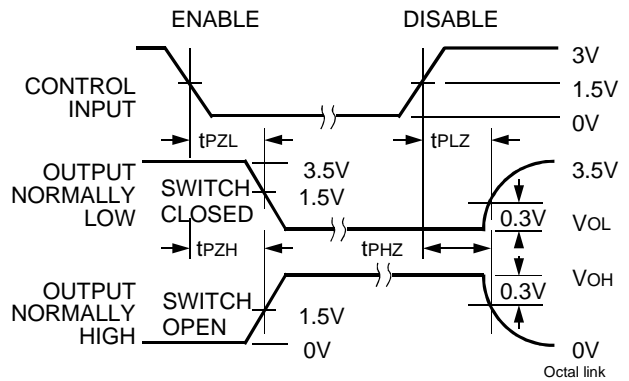
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

#### DEFINITIONS:

CL = Load capacitance: includes jig and probe capacitance.  
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.



Pulse Width

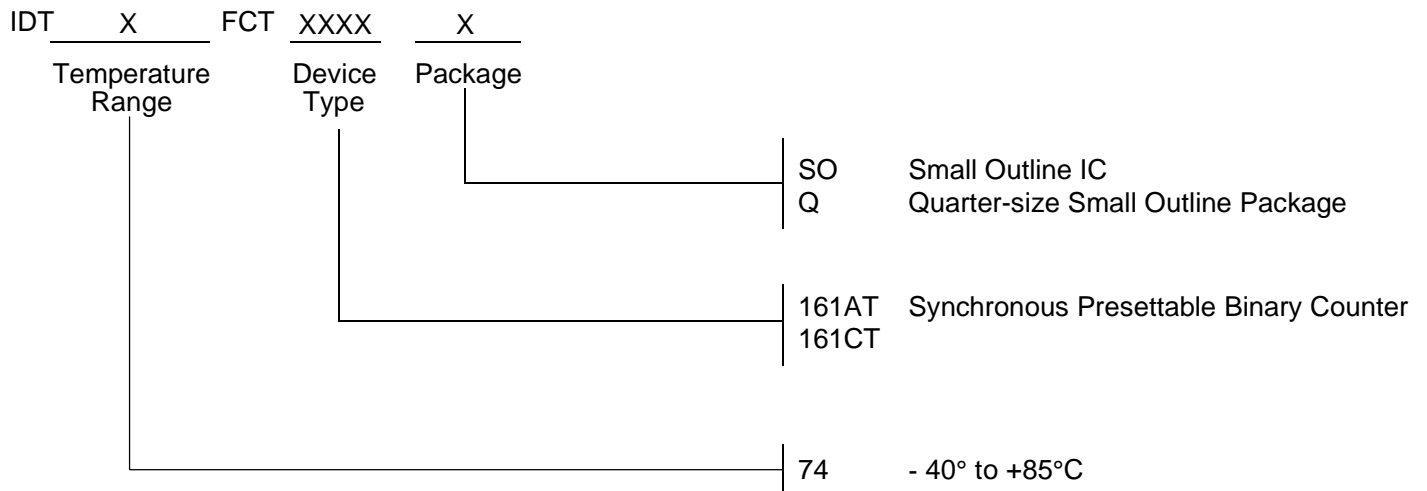


Enable and Disable Times

#### NOTES:

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
- Pulse Generator for All Pulses: Rate ≤ 1.0MHz; tr ≤ 2.5ns; tr ≤ 2.5ns.

## ORDERING INFORMATION



## DATA SHEET DOCUMENT HISTORY

3/25/2002 Removed standard speed grade



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