



FAST CMOS ADDRESS/CLOCK DRIVER

IDT74FCT162344AT/CT/ET

FEATURES:

- 0.5 MICRON CMOS Technology
- Ideal for address line driving and clock distribution
- 8 banks with 1:4 fanout and 3-state
- Typical $t_{sk(o)}$ (Output Skew) < 500ps
- Balanced Output Drivers ($\pm 24mA$)
- Reduced system switching noise
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- $V_{CC} = 5V \pm 10\%$
- Low input and output leakage $\leq 1\mu A$ (max.)
- Available in SSOP and TSSOP packages

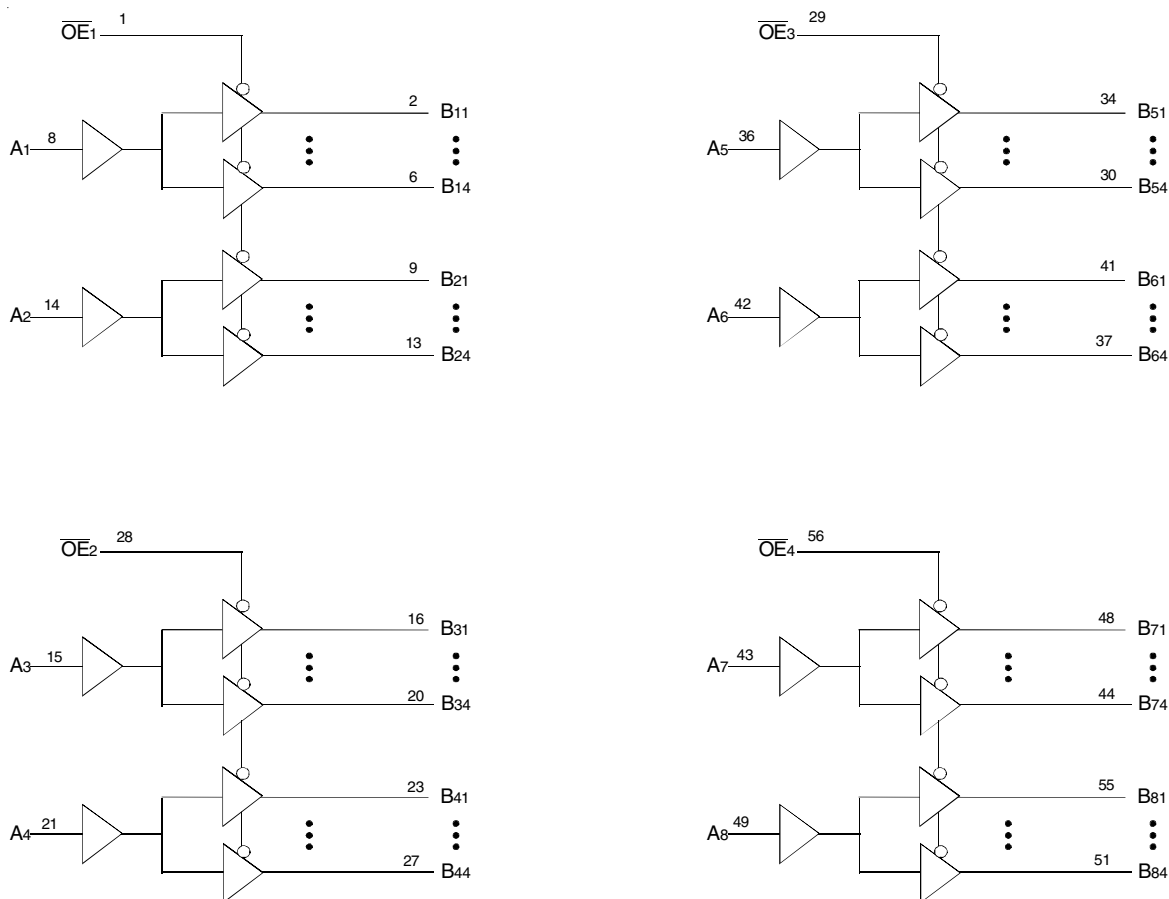
DESCRIPTION:

The FCT162344T is a 1:4 address/clock driver built using advanced dual metal CMOS technology. This high-speed, low power device provides the ability to fanout to memory arrays. Eight banks, each with a fanout of 4, and 3-state control provide efficient address distribution. One or more banks may be used for clock distribution.

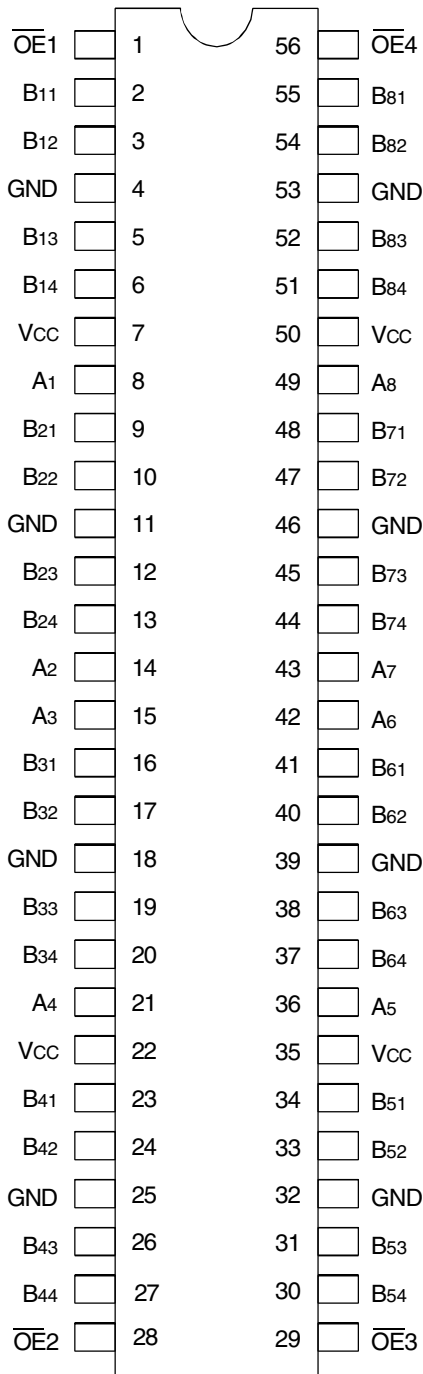
The FCT162344T has balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot and controlled output fall times reducing the need for external series terminating resistors.

A large number of power and ground pins and TTL output swings also ensure reduced noise levels. All inputs are designed with hysteresis for improved noise margins.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



SSOP/ TSSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Description	Max	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +7	V
VTERM ⁽³⁾	Terminal Voltage with Respect to GND	-0.5 to VCC+0.5	V
TSTG	Storage Temperature	-65 to +150	°C
IOUT	DC Output Current	-60 to +120	mA

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All device terminals except FCT162XXX Output and I/O terminals.
3. Output and I/O terminals terminals for FCT162XXX.

CAPACITANCE (TA = +25°C, F = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
CIN	Input Capacitance	VIN = 0V	3.5	6	pF
COU	Output Capacitance	VOUT = 0V	3.5	8	pF

NOTE:

1. This parameter is measured at characterization but not tested.

PIN DESCRIPTION

Pin Names	Description
OE _x	3-State Output Enable Inputs (Active LOW)
A _x	Inputs
B _{xx}	3-State Outputs

FUNCTION TABLE(1)

Inputs		Outputs
OE _x	A _x	B _{xx}
L	L	L
L	H	H
H	X	Z

NOTE:

1. H = HIGH Voltage Level
X = Don't Care
L = LOW Voltage Level
Z = High-Impedance

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Industrial: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Input pins) ⁽⁴⁾	$V_{CC} = \text{Max.}$	$V_i = V_{CC}$	—	—	± 1	μA
	Input HIGH Current (I/O pins) ⁽⁴⁾			—	—	± 1	
I_{IL}	Input LOW Current (Input pins) ⁽⁴⁾	$V_{CC} = \text{Max.}$	$V_i = \text{GND}$	—	—	± 1	μA
	Input LOW Current (I/O pins) ⁽⁴⁾			—	—	± 1	
I_{OZH}	High Impedance Output Current (3-State Output pins) ⁽⁴⁾	$V_{CC} = \text{Max.}$	$V_o = 2.7\text{V}$	—	—	± 1	μA
I_{OZL}				$V_o = 0.5\text{V}$	—	—	
V_{IK}	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18\text{mA}$		—	-0.7	-1.2	V
I_{OS}	Short Circuit Current	$V_{CC} = \text{Max.}, V_o = \text{GND}^{(3)}$		-80	-140	-250	mA
V_H	Input Hysteresis	—		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$ $V_{IN} = \text{GND or } V_{CC}$		—	5	500	μA

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
I_{ODL}	Output LOW Current	$V_{CC} = 5\text{V}, V_{IN} = V_{IH} \text{ or } V_{IL}, V_o = 1.5\text{V}^{(3)}$		60	115	200	mA
I_{ODH}	Output HIGH Current	$V_{CC} = 5\text{V}, V_{IN} = V_{IH} \text{ or } V_{IL}, V_o = 1.5\text{V}^{(3)}$		-60	-115	-200	mA
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -24\text{mA}$	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = 24\text{mA}$	—	0.3	0.55	V

NOTES:

1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at $V_{CC} = 5.0\text{V}$, $+25^{\circ}\text{C}$ ambient.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. This test limit for this parameter is $\pm 5\mu\text{A}$ at $T_A = -55^{\circ}\text{C}$.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(3)}$		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current ⁽⁴⁾	$V_{CC} = \text{Max.}$ Outputs Open $\overline{OE}_x = \text{GND}$ One Input Bit Toggling Four Output Bits Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	170	220	$\mu A/$ MHz
I_C	Total Power Supply Current ⁽⁶⁾	$V_{CC} = \text{Max.}$ Outputs Open $f_i = 10\text{MHz}$ 50% Duty Cycle $\overline{OE}_x = \text{GND}$ One Input Bit Toggling Four Output Bits Toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	1.7	2.7	mA
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	2	3.5	
		$V_{CC} = \text{Max.}$ Outputs Open $f_i = 2.5\text{MHz}$ 50% Duty Cycle $\overline{OE}_x = \text{GND}$ Eight Input Bits Toggling Thirty-Two Output Bits Toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	3.4	4.9 ⁽⁵⁾	
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	5.4	10.9 ⁽⁵⁾	

NOTES:

- For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0V$, $+25^\circ\text{C}$ ambient.
- Per TTL driven input ($V_{IN} = 3.4V$). All other inputs at V_{CC} or GND .
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
 $I_C = I_{CC} + \Delta I_{CC} \text{DH} + I_{CCD} (f_{CP} N_{CP} / 2 + f_i N_i)$
 $I_{CC} = \text{Quiescent Current (} I_{CCL}, I_{CCH} \text{ and } I_{CCZ} \text{)}$
 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input (} V_{IN} = 3.4V \text{)}$
 $\text{DH} = \text{Duty Cycle for TTL Inputs High}$
 $\text{NT} = \text{Number of TTL Inputs at DH}$
 $I_{CCD} = \text{Dynamic Current caused by an Input Transition Pair (HLH or LHL)}$
 $f_{CP} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$
 $N_{CP} = \text{Number of Clock Inputs at } f_{CP}$
 $f_i = \text{Input Frequency}$
 $N_i = \text{Number of Inputs at } f_i$

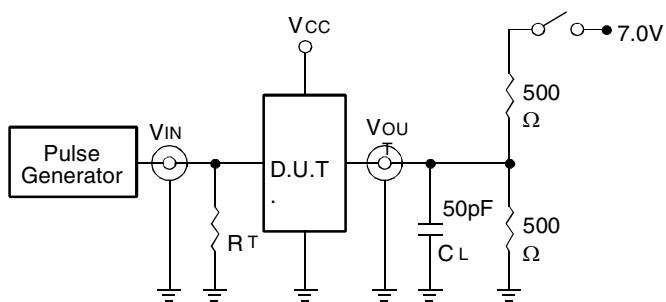
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition ⁽¹⁾	FCT1622344AT		FCT162344CT		FCT162344ET		Unit
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
t_{PLH}	Propagation Delay	$C_L = 50\text{pF}$ $R_L = 500\Omega$	1.5	4.8	1.5	4.3	1.5	3.8	ns
t_{PHL}	Ax to Bxx								
t_{PZH}	Output Enable Time		1.5	6.2	1.5	5.8	1.5	5	ns
t_{PZL}	\overline{OE}_x to Bx								
t_{PHZ}	Output Disable Time		1.5	5.6	1.5	5.2	1.5	4.6	ns
t_{PLZ}	\overline{OE}_x to Bx								
$t_{SK1}^{(3)}$	Skew between outputs of same bank and same package (same transition) ⁽³⁾	—	0.5	—	0.35	—	0.25	ns	
$t_{SK2}^{(3)}$	Skew between outputs of all banks of same package (A1 thru A8 tied together) ⁽³⁾	—	0.5	—	0.5	—	0.5	ns	

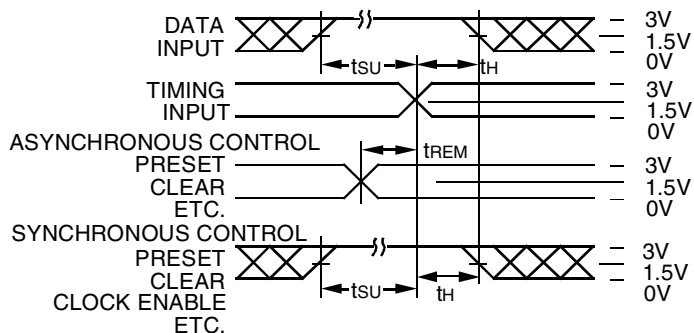
NOTES:

- See test circuit and waveforms.
- Minimum limits are guaranteed but not tested on Propagation Delays.
- This parameter is guaranteed but not production tested.

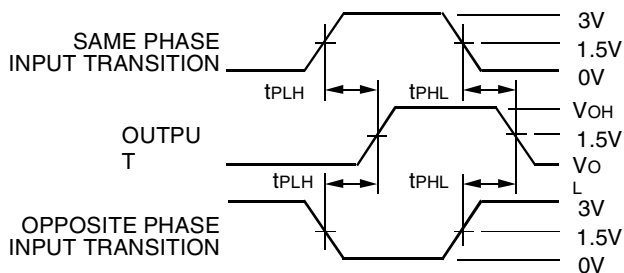
TEST CIRCUITS AND WAVEFORMS



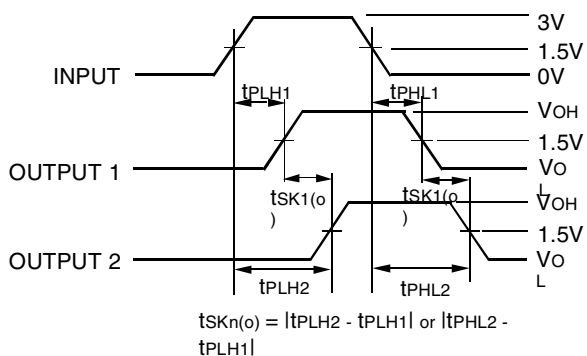
Test Circuits for All Outputs



Set-up, Hold, and Release Times



Propagation Delay



$$t_{SKn(o)} = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

Output Skew - $t_{SKn(o)}$

NOTES:

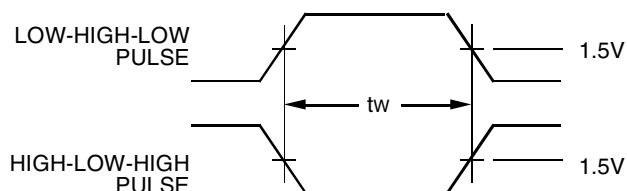
1. For $t_{SK1(o)}$ OUTPUT1 and OUTPUT2 are in the same bank.
2. For $t_{SK2(o)}$ OUTPUT1 and OUTPUT2 are in different banks on the same part.

SWITCH POSITION

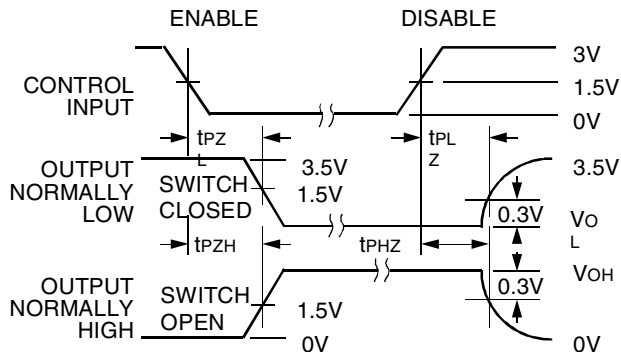
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.
 R_T = Termination resistance: should be equal to Z_{out} of the Pulse Generator.



Pulse Width

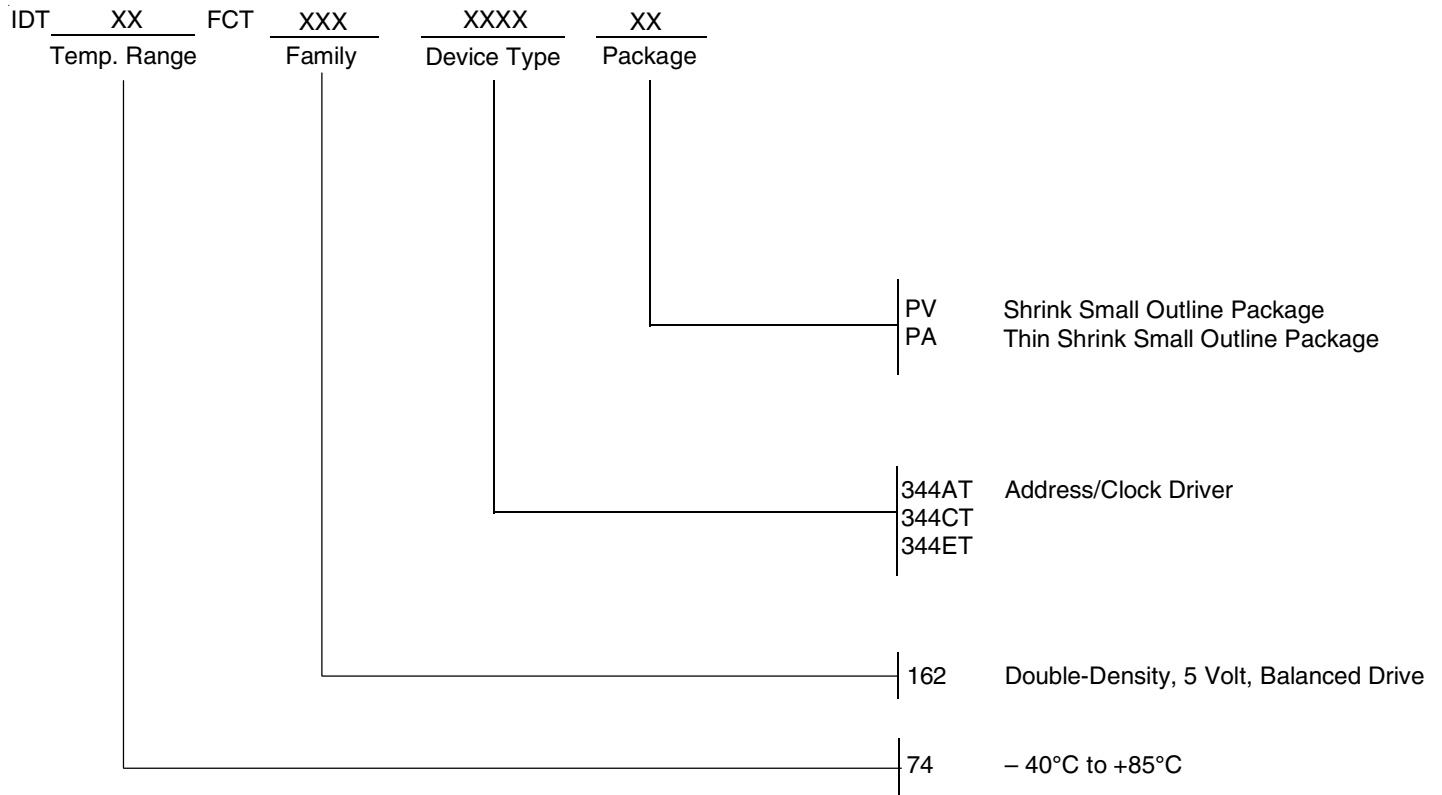


Enable and Disable Times

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; $t_r \leq 2.5\text{ns}$; $t_f \leq 2.5\text{ns}$.

ORDERING INFORMATION



DATA SHEET DOCUMENT HISTORY

1/21/2002 Removed Military temp grade
 5/21/2002 Removed TVSOP package



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