



FAST CMOS OCTAL BUFFER/LINE DRIVER

IDT54/74FCT244/A/C

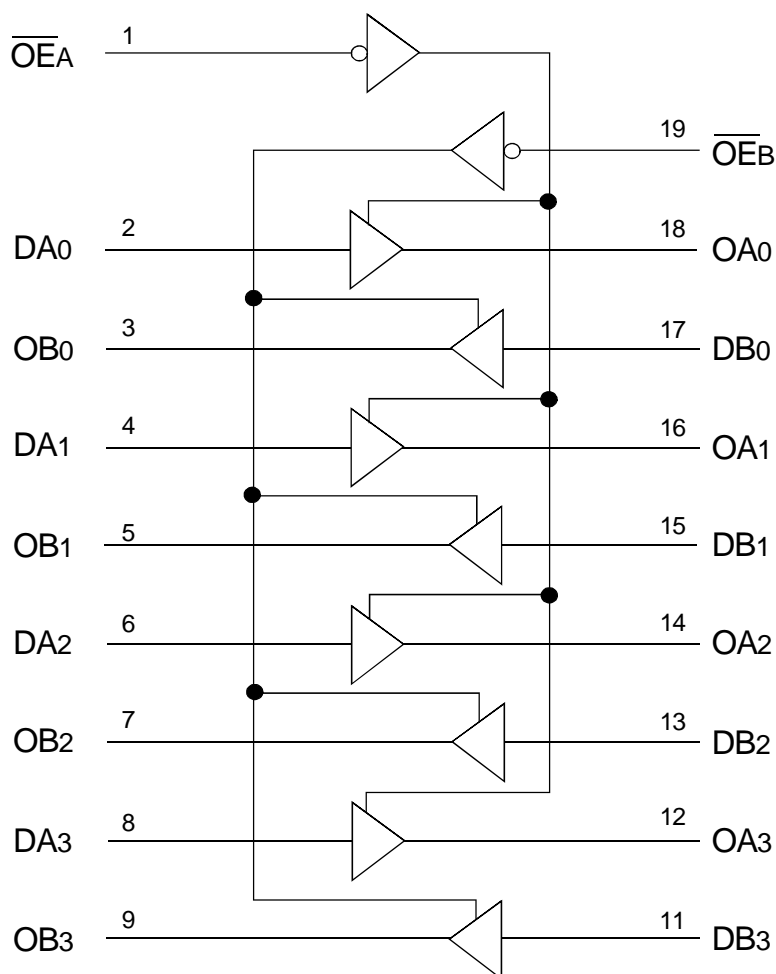
FEATURES:

- IDT54FCT244 equivalent to FAST™ speed and drive
- IDT54/74FCT244A 25% faster than FAST
- IDT74FCT244C up to 55% faster than FAST
- I_{OL} = 64mA (commercial) and 48mA (military)
- CMOS power levels (1mW typ. static)
- Military product compliant to MIL-STD-883, Class B
- Meets or exceeds JEDEC Standard 18 specifications
- Available in the following packages:
 - Commercial: SOIC
 - Military: CERDIP, LCC

DESCRIPTION:

The IDT octal buffer/line drivers are built using an advanced dual metal CMOS technology. The FCT244 is designed to be employed as a memory and address driver, clock driver, and bus-oriented transmitter/receiver which provides improved board density.

FUNCTIONAL BLOCK DIAGRAM

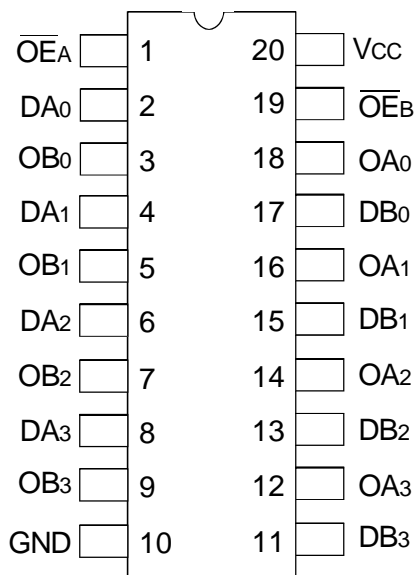


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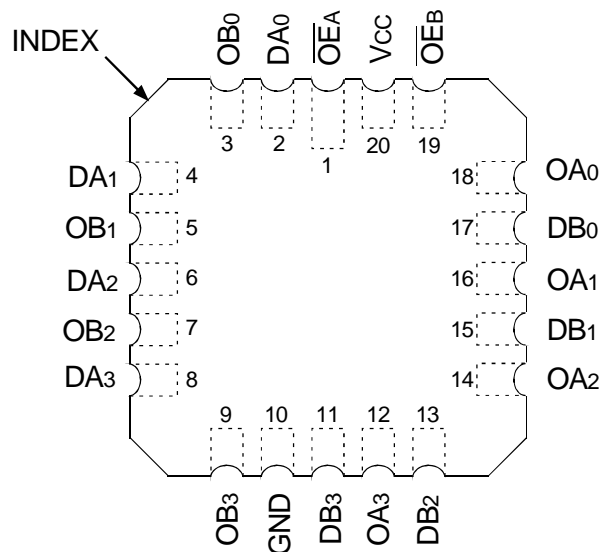
MILITARY AND COMMERCIAL TEMPERATURE RANGES

JUNE 2002

PIN CONFIGURATION



CERDIP/ SOIC
TOP VIEW



LCC
TOP VIEW

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Commercial	Military	Unit
V _{TERM} ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +7	-0.5 to +7	V
V _{TERM} ⁽³⁾	Terminal Voltage with Respect to GND	-0.5 to V _{CC}	-0.5 to V _{CC}	V
T _A	Operating Temperature	0 to +70	-55 to +125	°C
T _{BIAS}	Temperature under BIAS	-55 to +125	-65 to +135	°C
T _{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P _T	Power Dissipation	0.5	0.5	W
I _{OUT}	DC Output Current	120	120	mA

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
- Input and V_{CC} terminals only.
- Output and I/O terminals only.

CAPACITANCE (T_A = +25°C, F = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	6	10	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	8	12	pF

NOTE:

- This parameter is measured at characterization but not tested.

PIN DESCRIPTION

Pin Names	Description
\overline{OE}_A , \overline{OE}_B	3-State Output Enable Inputs (Active LOW)
D _{xx}	Inputs
O _{xx}	Outputs

FUNCTION TABLE⁽¹⁾

Inputs			Outputs
\overline{OE}_A	\overline{OE}_B	D	
L	L	L	L
L	L	H	H
H	H	X	Z

NOTE:

- H = HIGH Voltage Level
X = Don't Care
L = LOW Voltage Level
Z = High Impedance

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: $V_{LC} = 0.2V$; $V_{HC} = V_{CC} - 0.2V$

Commercial: $T_A = 0^\circ C$ to $+70^\circ C$, $V_{CC} = 5.0V \pm 5\%$, Military: $T_A = -55^\circ C$ to $+125^\circ C$, $V_{CC} = 5.0V \pm 10\%$

Symbol	Parameter	Test Conditions ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Unit	
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level	2	—	—	V	
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level	—	—	0.8	V	
I_{IH}	Input HIGH Current	$V_{CC} = \text{Max.}$	$V_I = V_{CC}$	—	—	5	μA
I_{IL}	Input LOW Current		$V_I = 2.7V$	—	—	5 ⁽⁴⁾	
			$V_I = 0.5V$	—	—	-5 ⁽⁴⁾	
			$V_I = GND$	—	—	-5	
I_{OZH}	Off State (High Impedance) Output Current	$V_{CC} = \text{Max.}$	$V_O = V_{CC}$	—	—	10	μA
I_{OZL}			$V_O = 2.7V$	—	—	10 ⁽⁴⁾	
			$V_O = 0.5V$	—	—	-10 ⁽⁴⁾	
			$V_O = GND$	—	—	-10	
V_{IK}	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18mA$	—	-0.7	-1.2	V	
I_{OS}	Short Circuit Current	$V_{CC} = \text{Max.}, V_O = GND$ ⁽³⁾	-60	-120	—	mA	
V_{OH}	Output HIGH Voltage	$V_{CC} = 3V, V_{IN} = V_{LC}$ or $V_{HC}, I_{OH} = -32\mu A$	V_{HC}	V_{CC}	—	V	
		$V_{CC} = \text{Min}$	$I_{OH} = -300\mu A$	V_{HC}	V_{CC}		—
		$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -12mA$ MIL	2.4	4.3		—
			$I_{OH} = -15mA$ COM'L	2.4	4.3		—
V_{OL}	Output LOW Voltage	$V_{CC} = 3V, V_{IN} = V_{LC}$ or $V_{HC}, I_{OL} = 300\mu A$	—	GND	V_{LC}	V	
		$V_{CC} = \text{Min}$	$I_{OL} = 300\mu A$	—	GND		V_{LC} ⁽⁴⁾
		$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 48mA$ MIL	—	0.3		0.55
			$I_{OL} = 64mA$ COM'L	—	0.3		0.55

NOTES:

1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at $V_{CC} = 5.0V$, $+25^\circ C$ ambient and maximum loading.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

$V_{LC} = 0.2V$; $V_{HC} = V_{CC} - 0.2V$

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
I _{CC}	Quiescent Power Supply Current	V _{CC} = Max. V _{IN} ≥ V _{HC} ; V _{IN} ≤ V _{LC}		—	0.2	1.5	mA
ΔI _{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V _{CC} = Max. V _{IN} = 3.4V ⁽³⁾		—	0.5	2	mA
I _{CCD}	Dynamic Power Supply Current ⁽⁴⁾	V _{CC} = Max. Outputs Open OE _A = OE _B = GND One Input Toggling 50% Duty Cycle	V _{IN} ≥ V _{HC} V _{IN} ≤ V _{LC}	—	0.15	0.25	mA/ MHz
I _C	Total Power Supply Current ⁽⁶⁾	V _{CC} = Max. Outputs Open f _i = 10MHz 50% Duty Cycle OE _A = OE _B = GND One Bit Toggling	V _{IN} ≥ V _{HC} V _{IN} ≤ V _{LC} (FCT)	—	1.7	4	mA
			V _{IN} = 3.4V V _{IN} = GND	—	2	5	
		V _{CC} = Max. Outputs Open f _i = 2.5MHz 50% Duty Cycle OE _A = OE _B = GND Eight Bits Toggling	V _{IN} ≥ V _{HC} V _{IN} ≤ V _{LC} (FCT)	—	3.2	6.5 ⁽⁵⁾	
			V _{IN} = 3.4V V _{IN} = GND	—	5.2	14.5 ⁽⁵⁾	

NOTES:

1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.

2. Typical values are at V_{CC} = 5.0V, +25°C ambient.

3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.

4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.

5. Values for these conditions are examples of ΔI_{CC} formula. These limits are guaranteed but not tested.

6. I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}

I_C = I_{CC} + ΔI_{CC} D_{HNT} + I_{CCD} (f_{CP}/2 + f_iN_i)

I_{CC} = Quiescent Current

ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)

D_H = Duty Cycle for TTL Inputs High

N_T = Number of TTL Inputs at D_H

I_{CCD} = Dynamic Current caused by an Input Transition Pair (HLH or LHL)

f_{CP} = Clock Frequency for register devices (zero for non-register devices)

f_i = Input Frequency

N_i = Number of Inputs at f_i

All currents are in milliamperes and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE^(1,2)

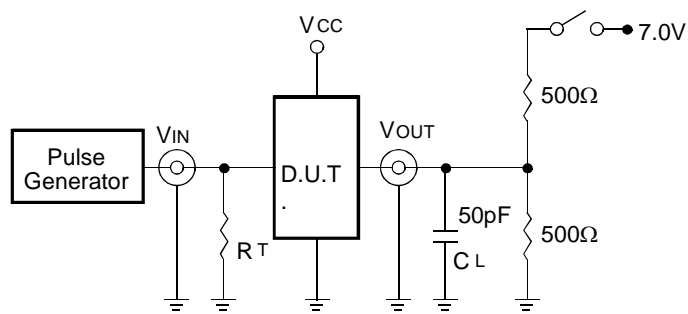
Symbol	Parameter	Condition	54FCT244		54/74FCT244A				74FCT244C		Unit
			Mil.		Com'l.		Mil.		Com'l.		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{PLH}	Propagation Delay	C _L = 50pF R _L = 500Ω	1.5	7	1.5	4.8	1.5	5.1	1.5	4.1	ns
t _{PHL}	Dx to Ox										
t _{PZH}	Output Enable Time		1.5	8.5	1.5	6.2	1.5	6.5	1.5	5.8	
t _{PZL}	Output Disable Time										
t _{PHZ}	Output Disable Time										
t _{PLZ}	Output Disable Time										

NOTES:

1. See test circuit and waveforms.

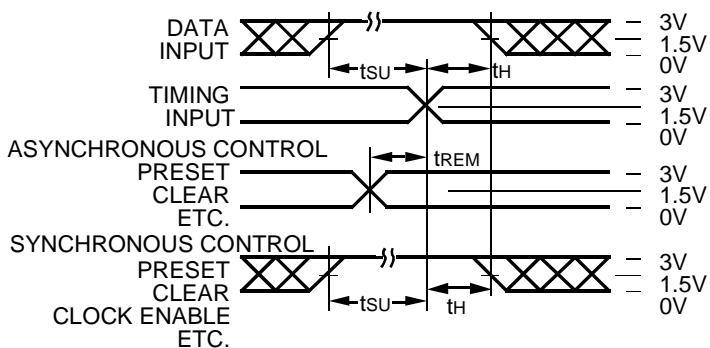
2. Minimum limits are guaranteed but not tested on Propagation Delays.

TEST CIRCUITS AND WAVEFORMS



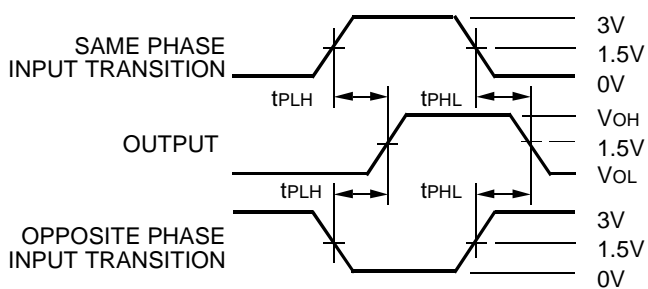
Octal Link

Test Circuits for All Outputs



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Set-Up, Hold, and Release Times



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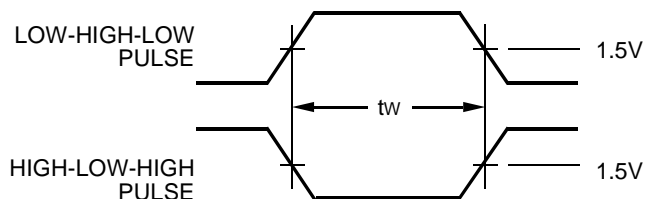
Propagation Delay

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

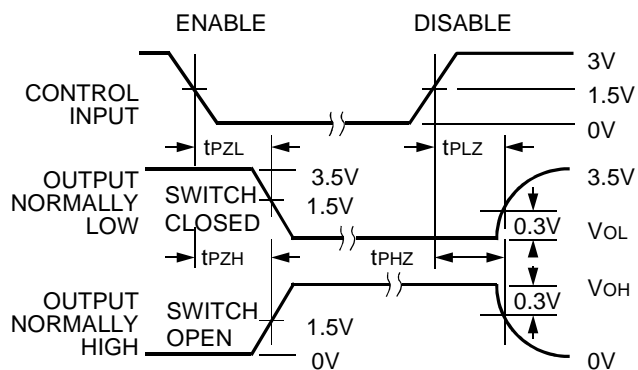
DEFINITIONS:

CL = Load capacitance: includes jig and probe capacitance.
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.



Pulse Width

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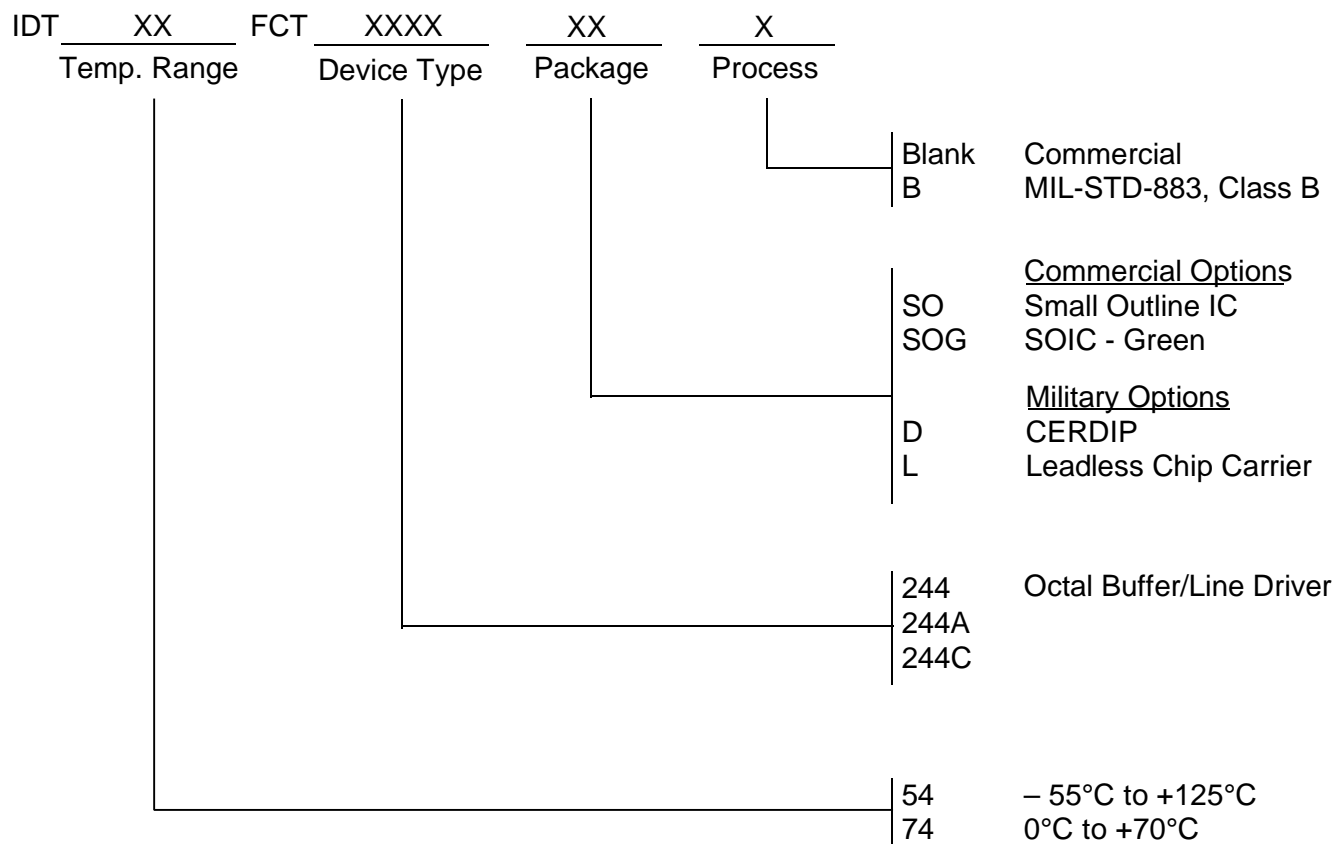
Enable and Disable Times

Octal Link

NOTES:

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
- Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Zo ≤ 50Ω; tr ≤ 2.5ns; tr ≤ 2.5ns.

ORDERING INFORMATION



DATA SHEET DOCUMENT HISTORY

6/21/2002 Updated according to PDNs Logic-00-07 and Logic-01-04



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