



Features

- ◆ **High-performance 64-bit embedded Microprocessor**
 - 250MHz operating frequency
 - >330 Dhrystone MIPS performance
 - 300MFLOPS/s floating-point performance
 - Up to 125 million multiply accumulate per second (MAC/s)
 - MIPS-IV Instruction Set Architecture (ISA), with integer DSP and 3-operand integer multiply extensions
 - Limited dual-issue microarchitecture
- ◆ **Compatible with RC4640 and RC32364 DSP extensions**
 - DSP Extensions, for consumer applications
 - 2-cycle repeat rate, on atomic Multiply-add
 - Multiply-subtract (MSUB) support, for complex number processing
 - Count-leading-zero/one support, for string searches and normalization
- ◆ **High-performance on-chip cache subsystem**
 - 32kB, two-set associative instruction cache (I-cache)
 - 32kB, two-set associative data cache (D-cache)
 - Write-through and write-back data cache operations
 - High-performance cache-ops, bandwidth management
- ◆ **I-cache and D-cache locking capability (per line), provides improved real-time support**
- ◆ **Joint TLB on-chip, for virtual-to-physical address mapping**
- ◆ **Big- or Little-endian capability**
- ◆ **RC5000 compatible memory management**
 - On-chip 48-entry, 96-page TLB, for advanced operating system support
 - Compatible with major operating systems: Windows® CE, VxWorks, and others
- ◆ **Bus compatible with IDT 64-bit microprocessor families**
 - Pipeline runs at 2 to 8 times the bus frequency
 - Bus speeds to 125MHz
 - 32-bit bus option, for lower cost systems
 - Enhanced timing protocol for SyncDRAM systems (compatible with IDT79RC64474/475)
- ◆ **RC64574:**
 - 32-bit SysAd bus, for low-cost systems
 - Pin compatible with RC4640 and RC64474
 - 128-pin QFP package
- ◆ **RC64575:**
 - 64-bit SysAd bus interface
 - Pin compatible with RC4650 and RC64475
 - 208-pin QFP package
- ◆ **Industrial temperature range support**
- ◆ **JTAG Boundary Scan Interface**
- ◆ **2.5V operation with 3.3V tolerant I/O**

Block Diagram

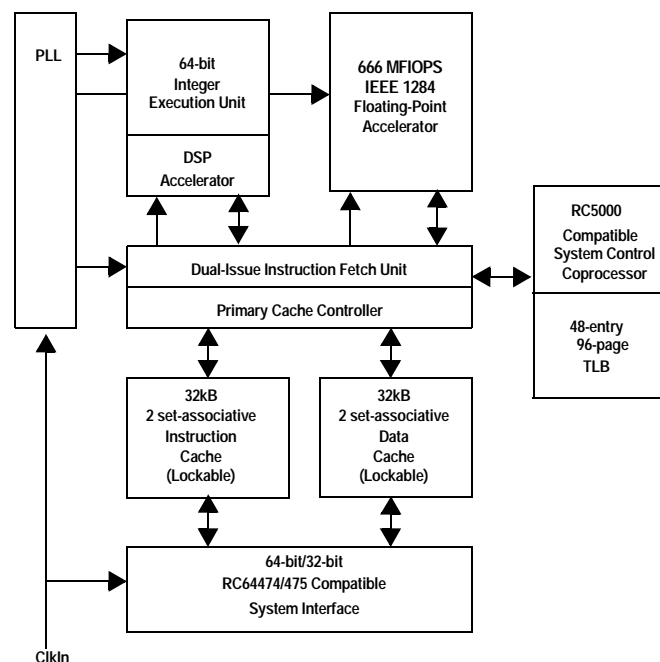


Figure 1 RC64574/RC64575 Block Diagram

Device Overview¹

IDT's 79RC64574/575 processors serve a wide range of performance-critical embedded applications that include high-end internet-working systems, digital set-top boxes, web browsers, color printers, and graphics terminals.

The RC64574/575 allow a socket compatible upgrade path for IDT's RC4640/50 and RC64474/475 processors. This unprecedented upgradability allows a 2:1 range of frequencies; 4:1 range of cache size; 15:1 range of floating-point; and 4:1 range of DSP performance in a single socket.

With special emphasis on system bandwidth, floating-point and DSP operations, the RC64574/575 have been optimized for high-performance applications through the integration of high-performance computational units and a high-performance memory hierarchy. The result is a low-cost CPU that is capable of more than 330 Dhrystone MIPS. Through the RC64574/64575 processors IDT offers:

- ◆ High-performance upgrade paths to existing embedded customers in the internetworking, office automation and visualization markets.
- ◆ Significant floating-point performance improvements over currently available, moderately priced MIPS CPUs.
- ◆ Performance improvements through the use of the MIPS-IV ISA.
- ◆ High-performance DSP acceleration

¹ Detailed system operation information is provided in the RC64574/RC64575 user's manual.

Instruction Issue Mechanism

The RC64574 and RC64575 are limited dual-issue super-scalar machines that use a traditional 5-stage integer pipeline, as shown in the pipeline diagram on Page 3. For multi-issue operations, these devices recognize the following two general classes of instructions:

- ◆ Floating-point ALU
- ◆ All others

Such a broad separation of instruction classes insure that there are no data dependencies to restrict multi-issue performance. As they are brought on-chip, these instruction classes are pre-decoded by the RC64574/575, and the class information is then stored in the instruction cache. Assuming there are no pending resource conflicts, the devices can issue one instruction per class per pipeline clock cycle.

However, longer latency resources—in either the floating-point ALU (for example, division or square root instructions) or integer unit (such as multiply)—can restrict the issue of instructions. Note that these processors do not perform out-of-order or speculative execution; instead, the pipeline slips until the required resource becomes available.

On dual-issue instruction pairs, there are no alignment restrictions, and the RC64574/575 fetch two instructions from the cache per cycle. Thus, for optimal performance, compilers should attempt to align branch targets to allow dual-issue on the first target cycle, because the instruction cache only performs aligned fetches.

RISCore4000/RISCore5000 Family of Socket Compatible Processors

| | 32-bit External Bus Processors | | | 64-bit External Bus Processors | | |
|---------------------|---|---|---|--|--|---|
| | RC4640 | RC64474 | RC64574 | RC4650 | RC64475 | RC64575 |
| CPU | 64-bit RISCore4000 w/ DSP extensions | 64-bit RISCore4000 | 64-bit RISCore5000 w/ DSP extensions | 64-bit RISCore4000 w/ DSP extensions | 64-bit RISCore4000 | 64-bit RISCore5000 w/ DSP extensions |
| Performance | >350MIPS | >330MIPS | >330MIPS | >350MIPS | >330MIPS | >330MIPS |
| FPA | 89 mflops, single precision only | 125 mflops, single and double precision | 666 mflops, single and double precision | 89 mflops, single precision only | 125 mflops, single and double precision | 666 mflops, single and double precision |
| Caches | 8kB/8kB, 2-way, lockable by set | 16kB/16kB, 2-way, lockable by set | 32kB/32kB, 2-way, lockable by line | 8kB/8kB, 2-way, lockable by set | 16kB/16kB, 2-way, lockable by set | 32kB/32kB, 2-way, lockable by line |
| External Bus | 32-bit | 32-bit, Superset pin compatible w/RC4640 | 32-bit, Superset pin compatible w/RC4640, RC64474 | 32- or 64-bit | 32- or 64-bit, Superset pin compatible w/ RC4650 | 32- or 64-bit, Superset pin compatible w/ RC4650, RC64475 |
| Voltage | 3.3V | 3.3V | 2.5V | 3.3V | 3.3V | 2.5V |
| Frequencies | 100-267 MHz | 180-250 MHz | 200-250 MHz | 100-267 MHz | 180-250 MHz | 250 MHz |
| Packages | 128 PQFP | 128 QFP | 128 QFP | 208 QFP | 208 QFP | 208 QFP |
| MMU | Base-Bounds | 96 page TLB | 96 page TLB | Base-Bounds | 96 page TLB | 96 page TLB |
| Key Features | Cache locking, on-chip MAC, 32-bit external bus | Cache locking, JTAG, syncDRAM mode, 32-bit external bus | Cache locking, JTAG, syncDRAM mode, 32-bit external bus | Cache locking, on-chip MAC, 32-bit & 64 bit bus option | Cache locking, JTAG, syncDRAM mode, 32-64-bit bus option | Cache locking, JTAG, syncDRAM mode, 32-64-bit bus option |

Table 1 RISCore4000/RISCore5000 Processor Family

Instruction Set Architecture

The RC64574/575 implement a superset of the MIPS-IV 64-bit ISA, including CP1 and CP1X functional units and their instruction set. Both 32- and 64-bit data operations are performed by utilizing thirty-two general purpose 64-bit registers (GPR) that are used for integer operations and address calculation. The complete on-chip floating-point coprocessor (CP1)—which includes a floating-point register file and execution units—forms a “seamless” interface, decoding and executing instructions in parallel with the integer unit.

CP1’s **floating-point execution units** support both single and double precision arithmetic—as specified in the IEEE Standard 754—and are separated into a multiply unit and a combined add/convert/divide/square root unit. Overlap of multiplies and add/subtract is supported, and the multiplier is partially pipelined, allowing the initiation of a new multiply instruction every fourth pipeline cycle. The **floating-point register file** is made up of thirty-two 64-bit registers. The floating-point unit can take advantage of the 64-bit wide data cache and issue a co-processor load or store doubleword instruction in every cycle.

The **system control coprocessor (CP0) registers** are also incorporated on-chip and provide the path through which the virtual memory system’s page mapping is examined and changed, exceptions are handled, and any operating mode selections are controlled. A secure user processing environment is provided through the **user, supervisor, and kernel operating modes** of virtual addressing to system software. Bits in a status register determine which of these modes is used.

Integer Pipeline

The integer instruction execution speed is tabulated—in number of pipeline clocks—as follows:

| Operation | Latency | Repeat |
|-------------------|---------|--------|
| Load | 2 | 1 |
| Store | 2 | 1 |
| MULT/MULTU | 4 | 3 |
| DMULT/DMULTU | 6 | 5 |
| DIV/DIVU | 36 | 36 |
| DDIV/DDIVU | 68 | 68 |
| MAD/MADU | 3 | 2 |
| MSUB/MSUBU | 4 | 3 |
| Other Integer ALU | 1 | 1 |
| Branch | 2 | 2 |
| Jump | 2 | 2 |

Table 2 Integer Instruction Execution Speed

To insure that the maximum frequency of operation is not limited by the speed of the multiplier unit, a “**fast multiply**” disable reset mode bit (see Table 2) is featured. When this bit is asserted, each multiply operation shown in Table 1 has its latency and repeat rate increased by one cycle.

Load and branch latencies are minimized by the short pipeline of the RC64574/575, and the caches contain special logic that will allow any combination of loads and stores to execute in back-to-back cycles without requiring pipeline slips or stalls, assuming the operation does not miss in the cache.

Computational Units

The RC64574/575 implement a full, single-cycle 64-bit arithmetic logic unit (ALU), for **Integer ALU** functions other than multiply and divide. Bypassing is used to support back-to-back ALU operations at the full pipeline rate, without requiring stalls for data dependencies.

To allow the longer latency operations to run in parallel with other operations, the **Integer Multiply/Divide** unit of the RC64574/575 is separated from the primary ALU. The pipeline stalls only if an attempt to access the HI or LO registers is made before an operation completes.

The **Floating-point ALU** unit is responsible for all of the CP1/CP1X ALU operations—other than DIV/SQRT operations—and is pipelined to allow a single-cycle repeat rate for single-precision operations.

The **Floating-point DIV/SQRT** unit is separated from the floating-point ALU, to ensure that these longer latency operations do not prevent the issue of other floating-point operations. Separate logical units are also provided on the RC64574/575 to implement load, store, and branch operations.

Intended to enhance the performance of DSP algorithms such as fast fused multiply-adds, multiply-subtracts and three operand multiply operations, **new instructions** have been added over and above the MIPS-IV ISA.

System Interfaces

The **RC64575 supports a 64-bit system interface** that is pin and bus compatible with the RC4650 and RC64475 system interface. The system interface consists of a 64-bit Address/Data bus with eight parity-check bits and a 9-bit command bus.

During 64-bit operation, RC64575 system address/data (SysAD) transfers are protected with an 8-bit parity check bus, SysADC. When initialized for 32-bit operation, the RC64575’s SysAD can be viewed as a 32-bit multiplexed bus that is protected by four parity-check bits.

The **RC64574 supports a 32-bit system interface** that is pin and bus compatible with the RC4640 and RC64474. During 32-bit operation, SysAD transfers are performed on a 32-bit multiplexed bus (SysAD 31:0) that is protected by 4 parity check bits (SysADC 6:0).

Writes to external memory—whether they are cache miss write-backs, stores to uncached or write-through addresses—use the on-chip **write buffer**. The write buffer holds a maximum of four 64-bit addresses and 64-bit data pairs. The entire buffer is used for a data cache write-back and allows the processor to proceed in parallel with memory updates.

Included in the system interface are **six handshake signals**: RdRdy*, WrRdy*, ExtRqst*, Release*, ValidOut*, and ValidIn*; **six interrupt inputs**, and a **simple timing** specification that is capable of trans-

ferring data between the processor and memory at a peak rate of 1000MB/sec. A boot-time selectable option to run the system interface as 32-bits wide—using basically the same protocols as the 64-bit system—is also supported.

A **boot-time mode control interface** initializes fundamental processor modes and is a serial interface that operates at a very low frequency (SysClk divided by 256). This low-frequency operation allows the initialization information to be kept in a low-cost EPROM; alternatively, the twenty-or-so bits could be generated by the system interface ASIC or a simple PAL. The boot-time serial stream is shown in Table 3.

| Serial Bit | Description | Value & Mode Setting |
|------------|--------------------------------------|---|
| 0 | Reserved | Must be set to 0. |
| 1:4 | Transmit-data-pattern. Bit 4 is MSB | 64-bit bus width: 0: DDDD 1: DDxDDx 2: DDxxDDxx 3: Dx Dx Dx Dx 4: DDxxxDDxxx 5: DDxxxxDDxxxx 6: DxxDxxDxxDxx 7: DDxxxxxxDDxxxxxx 8: DxxxDxxxDxxxDxxx 9-15: Reserved. Must not be selected. 32-bit bus width: 0: WWWWWWWW 1: WWxWWxWWxWWx 2: WWxxWWxxWWxxWWxx 3: WxWxWxWxWxWxWxWx 4: WWxxxWWxxxWWxxxWWxxx 5: WWxxxxWWxxxxWWxxxxWWxxxx 6: WxxWxxWxxWxxWxxWxxWxxWxx 7: WxxxxxxWxxxxxxWxxxxxxWxxxxxx 8: WxxxWxxxWxxxWxxxWxxxWxxxWxxx 9-15: Reserved. Must not be selected. |
| 5:7 | PClock-to-SysClk-Ratio. Bit 7 is MSB | 0: 2 1: 3 2: 4 3: 5 4: 6 5: 7 6: 8 7: Reserved |
| 8 | Endianness | 0: Little endian 1: Big endian |
| 9:10 | Non-block write Mode. Bit 10 is MSB | 00: R4400 compatible 01: Reserved 10: Pipelined-Write-Mode 11: Write-Reissue-Mode |

Table 3 Boot-time Mode Stream (Page 1 of 2)

| Serial Bit | Description | Value & Mode Setting |
|------------|------------------------------------|--|
| 11 | TimerIntEn | Timer interrupt settings: 0: Enable Timer Interrupt on Int(5) 1: Disable Timer Interrupt on Int(5) |
| 12 | System Interface Bus Width. | Interface bus width control settings: 0: 64-bit system interface 1: 32-bit system interface |
| 13:14 | Drv_Out Bit 14 is MSB | Slew rate control of the output drivers: 10: 100% strength (fastest) 11: 83% strength 00: 67% strength 01: 50% strength (slowest) |
| 15:17 | Write address to write data delay. | From 0 to 7 SysClk cycles: 0: AD... 1: AxD... 2: AxxD... 3: AxxxD... 4: AxxxxD... 5: AxxxxxD... 6: AxxxxxD... 7: AxxxxxD... |
| 18 | Reserved | User must select '0' |
| 19 | Extend Multiplication Repeat Rate. | Initial setting of the "Fast Multiply" bit. 0: Enable Fast Multiply 1: Do not Enable Fast Multiply Note: For pipeline speeds >250MHz, this bit must be set to '1'. |
| 20:24 | Reserved | User must select '0' |
| 25:26 | System configuration identifier. | Software visible in processorConfig[21:20] 0: Config[21:20] = Mode Bit [25:26] Must be set to 0. |
| 27:256 | Reserved | User must select '0' |

Table 3 Boot-time Mode Stream (Page 2 of 2)

The **clocking interface** allows the CPU to be easily mated with external reference clocks. The CPU input clock is the bus reference clock and can be between 33 and 125MHz. An on-chip **phase-locked-loop (PLL)** generates the pipeline clock (PClock) through multiplication of the system interface clock by values of 2,3,4,5,6,7 or 8, as defined at system reset. This allows the pipeline clock to be implemented at a significantly higher frequency than the system interface clock. The RC64574/575 support both single data (one byte through full CPU bus width) and 8-word block transfers on the SysAD bus.

The RC64574/575 implement additional **write protocols** that **double the effective write bandwidth**. The write re-issue has a repeat rate of 2 cycles per write. Pipelined writes have the same 2-cycle per write repeat rate, but can issue an additional write after WrRdy* de-asserts.

Choosing a 32- or 64-bit wide system interface dictates whether a cache line block transaction requires 4 double word data cycles or 8 single word cycles as well as whether a single data transfer—larger than 4 bytes—must be divided into two smaller transfers.

As shown in Table 3, the bus delay can be defined as 0 to 7 SysClock cycles and is activated and controlled through mode bit (17:15) settings selected during the reset initialization sequence. The '000' setting provides the same write operations timing protocol as the RC4640, RC4650, and RC5000 processors.

To facilitate discrete **interface to SyncDRAM**, the RC64574/575 bus interface is enhanced during write cycles with a programmable delay that is inserted between the write address and the write data (for both block and non-block writes).

Board-level testing during Run-Time mode is facilitated through the full JTAG boundary scan facility. Five pins—TDI, TDO, TMS, TCK, TRST*—have been incorporated to support the standard JTAG interface.

The RC64574/575 devices offer a direct migration path for designs that are based on IDT's RC4640/RC4650 and RC64474/RC64475 processors², through full pin and socket compatibility. Full 64-bit-family software and bus protocol compatibility ensures the RC64574/575 processors access to an existing market and development infrastructure, allowing quicker time to market.

Development Tools

An array of hardware and software tools is available to assist system designers in the rapid development of RC64574/575 based systems. This accessibility allows a wide variety of customers to take full advantage of the device's high-performance features while addressing today's aggressive time-to-market demands.

Cache Memory

To keep the high-performance pipeline of the RC64574/575 full and operating efficiently, on-chip instruction and data caches have been incorporated. Each cache has its own data path and can be accessed in the same single pipeline clock cycle.

The 32kB two-way set associative **instruction cache** is virtually indexed, physically tagged, and word parity protected. Because this cache is virtually indexed, the virtual-to-physical address translation occurs in parallel with the cache access, further increasing performance by allowing both operations to occur simultaneously. The instruction cache provides a peak instruction bandwidth of 2GB/sec at 250MHz.

The 32kB two-way set associative **data cache** is byte parity protected and has a fixed 32-byte (eight words) line size. Its tag is protected with a single parity bit. To allow simultaneous address translation and data cache access, the D-cache is virtually indexed and physically tagged. The data cache can provide 8 bytes each clock cycle, for a peak bandwidth of 2GB/s.

² To ensure socket compatibility, refer to Table 8 and Table 9.

To lock critical sections of code and/or data into the caches for quick access, a per line "**cache locking**" feature has been implemented. Once enabled, a cache is said to be locked when a particular piece of code or data is loaded into the cache and that cache location will not be selected later for refill by other data.

Power Management

Executing the WAIT instruction enables the processor to enter Standby mode. The internal clocks will shut down, thus freezing the pipeline. The PLL, internal timer, and some of the input pins (Int[5:0]*, NMI*, ExtReq*, Reset*, and ColdReset*) will continue to run. Once in Standby Mode, any interrupt, including the internally generated timer interrupt, will cause the CPU to exit Standby Mode.

Thermal Considerations

The RC64574 is packaged in a 128-pin QFP footprint package and uses a 32-bit external bus, offering the ideal combination of 64-bit processing power and 32-bit low-cost memory systems. The RC64575 is packaged in a 208-pin QFP footprint package and uses the full 64-bit external bus. The RC64575 is ideal for applications requiring 64-bit performance and 64-bit external bandwidth.

Both devices are guaranteed in a case temperature range of 0° to +85° C for commercial temperature devices and -40° to +85° C for Industrial temperature devices. Package type, speed (power) of the device, and air flow conditions affect the equivalent ambient temperature conditions that will meet these specifications.

Using the thermal resistance from case to ambient (Θ_{CA}) of the given package, the equivalent allowable ambient temperature, T_A , can be calculated. The following equation relates ambient and case temperatures:

$$T_A = T_C - P * \Theta_{CA}$$

where P is the maximum power consumption at hot temperature, calculated by using the maximum ICC specification for the device. Typical values for Θ_{CA} at various air flow are shown in Table 4. Note that the RC64574/575 processor implements advanced power management, which substantially reduces the typical power dissipation of the device.

| Airflow (ft/min) | Θ_{CA} | | | | | |
|------------------|---------------|-----|-----|-----|-----|------|
| | 0 | 200 | 400 | 600 | 800 | 1000 |
| 128 QFP | 16 | 10 | 9 | 7 | 6 | 5 |
| 208 QFP | 20 | 13 | 10 | 9 | 8 | 7 |

Table 4 Thermal Resistance (Θ_{CA}) at Various Airflows

Revision History

July 22, 1999: Original data sheet.

September 9, 1999: Made several changes in JTAG Interface section of Table 5. Added information on Pin 63 in Table 5.

October 14, 1999: Revised data in the Power Consumption tables for RC64574 and RC64575.

November 16, 1999: Added Power Curve graphs, revised data in System Interface Parameters table, added System Clock Jitter row to Clock Parameter table.

December 20, 1999: Table 7 "RC64574 128-Pin Package" on page 12, Changed pin #75 function from Vcc to N.C.

March 7, 2000: In Table 1, added "with DSP extensions" in the CPU row under RC64574 and RC64575 columns and changed "by set" to "by line" in the Caches row for RC64574 and RC64575 columns. Added rows in the Data Output and Data Output Hold rows in the System Interface Parameters table. Removed references to 300 MHz, and changed bandwidth speed to 2GB/second in Cache Memory section. Revised Power Curves.

March 28, 2000: Replaced existing figure in Mode Configuration Interface Reset Sequence section with 3 reset figures. Revised values for 250MHz in System Interface Parameters table. Changed Data Sheet from Preliminary to final.

April 3, 2000: Deleted signal t_{DZ} from Figure 6.

April 25, 2001: In the Absolute Maximum Ratings table, changed upper voltage limit from 3.8 to 4.0V and removed "Vin should not exceed Vcc +0.5 volts" from footnote #1. In DC Electrical Characteristics table, changed maximum value for Vih from 3.3 to 3.8V for all speeds.

May 1, 2001: In the Data Output Hold category of the System Interface Parameters table, changed values in the Min column for all speeds from 1.0 to 0. In the Electrical Characteristics table, values were added to the System Clock Jitter row. Added Industrial temperature range of -40° C to +85° C.

December 14, 2001: In Absolute Maximum Ratings Table, changed the Industrial low-end temperature for symbol Tc to read -40 degrees instead of 0 degrees.

Pin Description Table

The following is a list of system interface pins available on the RC64574/575. Pin names ending with an asterisk (*) are active when low.

| Pin Name | Type | Description |
|--------------------------------|------|--|
| System Interface | | |
| ExtRqst* | I | External request An external agent asserts ExtRqst* to request use of the System interface. The processor grants the request by asserting Release*. |
| Release* | O | Release interface In response to the assertion of ExtRqst* or a CPU read request, the processor asserts Release* and signals to the requesting device that the system interface is available. |
| RdRdy* | I | Read Ready The external agent asserts RdRdy* to indicate that it can accept a processor read request. |
| WrRdy* | I | Write Ready An external agent asserts WrRdy* when it can now accept a processor write request. |
| ValidIn* | I | Valid Input Signals that an external agent is now driving a valid address or data on the SysAD bus and a valid command or data identifier on the SysCmd bus. |
| ValidOut* | O | Valid Output Signals that the processor is now driving a valid address or data on the SysAD bus and a valid command or data identifier on the SysCmd bus. |
| SysAD(63:0) | I/O | System address/data bus A 64-bit address and data bus for communication between the processor and an external agent. In 64 bit interface mode, during address phases only, SysAd(35:0) contains invalid address information. The remaining SysAD(63:36) pins are not used. The whole 64-bit SysAD(63:0) may be used during the data transfer phase. For all double-word accesses (read or write), the low-order 3 bits (SysAD[2:0]) will always be output as zero during the address phase. In 32-bit interface mode and in the RC64574, SysAD(63:32) is not used, regardless of Endianness. A 32-bit address and data communication between processor and external agent is performed via SysAD(31:0). |
| SysADC(7:0) | I/O | System address/data check bus An 8-bit bus containing parity check bits for the SysAD bus during data bus cycles. In 32-bit mode and in the RC64574, SysADC(7:4) is not used. The SysADC(3:0) contains check bits for SysAD(31:0). |
| SysCmd(8:0) | I/O | System command/data identifier bus A 9-bit bus for command and data identifier transmission between the processor and an external agent. |
| SysCmdP | I/O | System Command Parity A single, even-parity bit for the Syscmd bus. This signal is always driven low. |
| Clock/Control Interface | | |
| SysClock | I | SystemClock The system clock input establishes the processor and bus operating frequency. It is multiplied internally by 2,3,4,5,6,7, or 8 to generate the pipeline clock (PClock). |
| V _{cc} P | I | Quiet VCC for PLL Quiet Vcc for the internal phase locked loop. |
| V _{ss} P | I | Quiet V_{ss} for PLL Quiet Vss for the internal phase locked loop. |

Table 5 Pin Descriptions (Page 1 of 2)

| Pin Name | Type | Description |
|---------------------------------|------|--|
| Interrupt Interface | | |
| Int*(5:0) | I | Interrupt Six general processor interrupts, bit-wise ORed with bits 5:0 of the interrupt register. |
| NMI* | I | Non-maskable interrupt Non-maskable interrupt, ORed with bit 6 of the interrupt register. |
| Initialization Interface | | |
| V _{ccOk} | I | V_{cc} is OK When asserted, this signal indicates to the processor that the power supply has been above the V _{cc} minimum for more than 100 milliseconds and will remain stable. The assertion of V _{ccOk} initiates the initialization sequence. |
| ColdReset* | I | Cold reset This signal must be asserted for a power on reset or a cold reset. ColdReset must be de-asserted synchronously with SysClock. |
| Reset* | I | Reset This signal must be asserted for any reset sequence. It can be asserted synchronously or asynchronously for a cold reset, or synchronously to initiate a warm reset. Reset must be de-asserted synchronously with SysClock. |
| ModeClock | O | Boot-mode clock Serial boot-mode data clock output at the system clock frequency divided by two hundred fifty-six. |
| ModeIn | I | Boot-mode data in Serial boot-mode data input. |
| JTAG Interface | | |
| TDI | I | JTAG Data In On the rising edge of TCK, serial input data are shifted into either the Instruction register or Data register, depending on the TAP controller state. An external pull-up resistor is required. |
| TDO | O | JTAG Data Out On the falling edge of TCK, the TDO is serial data shifted out from either the instruction or data register. When no data is shifted out, the TDO is tri-stated (high impedance). |
| TCK | I | JTAG Clock Input An input test clock used to shift into or out of the boundary-scan register cells. TCK is independent of the system and processor clock with nominal 40-60% duty cycle. |
| TMS | I | JTAG Command Select The logic signal received at the TMS input is decoded by the TAP controller to control test operation. TMS is sampled on the rising edge of TCK. An external pull-up resistor is required. |
| TRST* | I | JTAG Reset The TRST* pin is an active-low signal used for asynchronous reset of the debug unit, independent of the processor logic. During normal CPU operation, the JTAG controller will be held in the reset mode, asserting this active low pin. When asserted low, this pin will also tristate the TDO pin. An external pull-down resistor is required. |
| JTAG32* | I | JTAG 32-bit scan This pin is used to control length of the scan chain for SysAD (32-bit or 64-bit) for the JTAG mode. When set to V _{ss} , 32-bit bus mode is selected. In this mode, only SysAD(31:0) are part of the scan chain. When set to V _{cc} , 64-bit bus mode is selected. In this mode, SysAD(63:0) are part of the scan chain. This pin has a built-in pull-down device to guarantee 32-bit scan, if it is left unconnected. |
| JR_V _{cc} | I | JTAG VCC This pin has an internal pull-down to continuously reset the JTAG controller (if left unconnected) bypassing the TRst* pin. When supplied with V _{cc} , the TRst* pin will be the primary control for the JTAG reset. |

Table 5 Pin Descriptions (Page 2 of 2)

Logic Diagram — RC64574/RC64575

Figure 1 illustrates the direction and functional groupings for the processor signals.

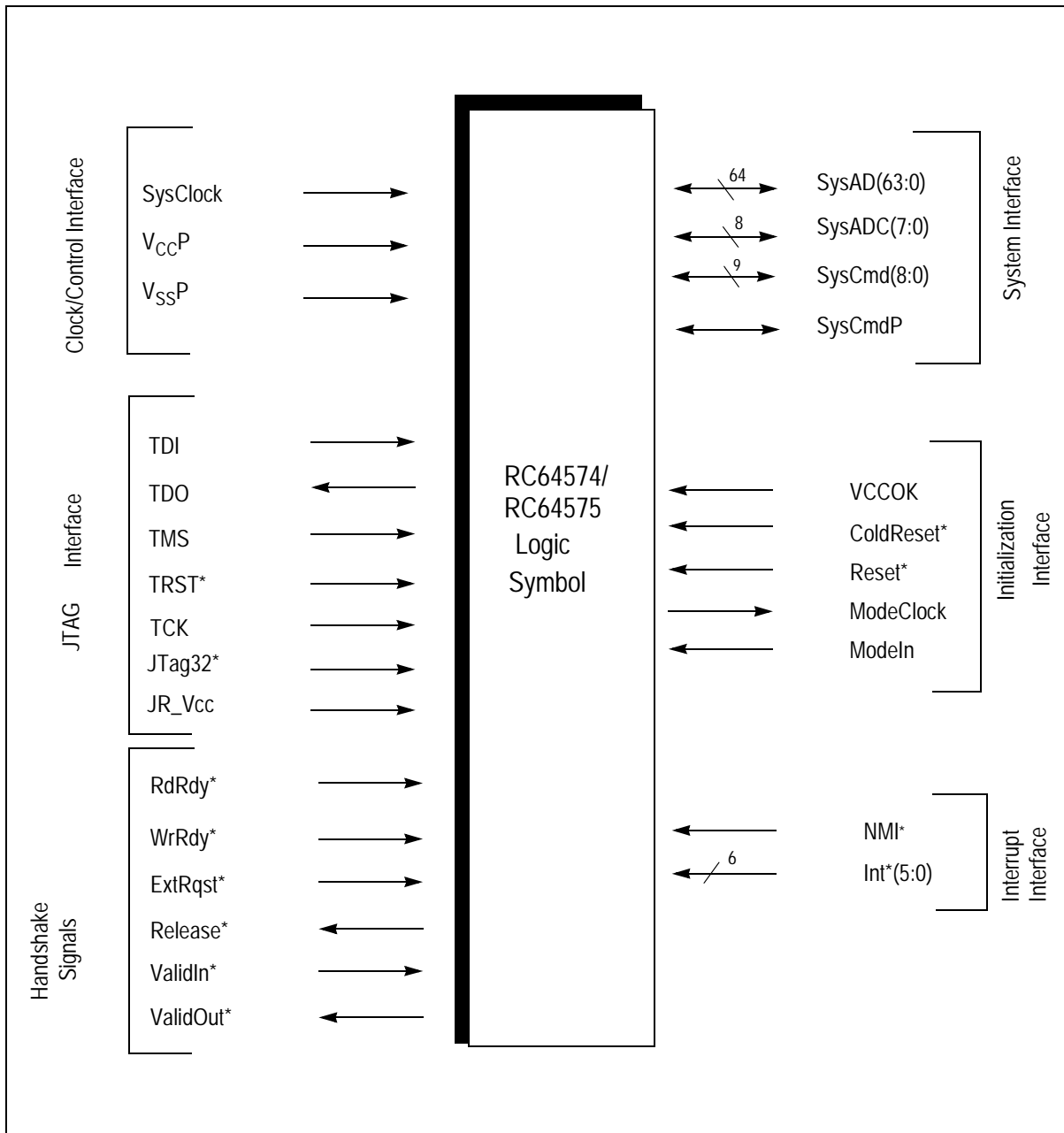


Figure 1 Logic Symbol for RC64574/RC64575

RC64575 208-pin QFP Package Pin-out

Pin names followed by an asterisk (*) are active when low. For maximum flexibility and compatibility with future designs, N.C. pins should be left floating.

| Pin | Function | Pin | Function | Pin | Function | Pin | Function |
|-----|-----------------|-----|-----------------|-----|-----------------|-----|--------------------|
| 1 | N.C. | 53 | JTAG32* | 105 | N.C. | 157 | N.C. |
| 2 | N.C. | 54 | N.C. | 106 | N.C. | 158 | N.C. |
| 3 | N.C. | 55 | N.C. | 107 | N.C. | 159 | SysAD59 |
| 4 | N.C. | 56 | N.C. | 108 | N.C. | 160 | ColdReset* |
| 5 | N.C. | 57 | SysCmd2 | 109 | N.C. | 161 | SysAD28 |
| 6 | N.C. | 58 | SysAD36 | 110 | N.C. | 162 | V _{cc} |
| 7 | N.C. | 59 | SysAD4 | 111 | N.C. | 163 | V _{ss} |
| 8 | N.C. | 60 | SysCmd1 | 112 | N.C. | 164 | SysAD60 |
| 9 | N.C. | 61 | V _{ss} | 113 | N.C. | 165 | Reset* |
| 10 | SysAD11 | 62 | V _{cc} | 114 | SysAD52 | 166 | SysAD29 |
| 11 | V _{ss} | 63 | SysAD35 | 115 | ExtRqst* | 167 | SysAD61 |
| 12 | V _{cc} | 64 | SysAD3 | 116 | V _{cc} | 168 | SysAD30 |
| 13 | SysCmd8 | 65 | SysCmd0 | 117 | V _{ss} | 169 | V _{cc} |
| 14 | SysAD42 | 66 | SysAD34 | 118 | SysAD21 | 170 | V _{ss} |
| 15 | SysAD10 | 67 | V _{ss} | 119 | SysAD53 | 171 | SysAD62 |
| 16 | SysCmd7 | 68 | V _{cc} | 120 | RdRdy* | 172 | SysAD31 |
| 17 | V _{ss} | 69 | SysAD2 | 121 | Modein | 173 | SysAD63 |
| 18 | V _{cc} | 70 | Int5* | 122 | SysAD22 | 174 | V _{cc} |
| 19 | SysAD41 | 71 | SysAD33 | 123 | SysAD54 | 175 | V _{ss} |
| 20 | SysAD9 | 72 | SysAD1 | 124 | V _{cc} | 176 | V _{cc} OK |
| 21 | SysCmd6 | 73 | V _{ss} | 125 | V _{ss} | 177 | SysADC3 |
| 22 | SysAD40 | 74 | V _{cc} | 126 | Release* | 178 | SysADC7 |
| 23 | V _{ss} | 75 | Int4* | 127 | SysAD23 | 179 | N.C. |
| 24 | V _{cc} | 76 | SysAD32 | 128 | SysAD55 | 180 | TDI |
| 25 | SysAD8 | 77 | SysAD0 | 129 | NMI* | 181 | TRst* |
| 26 | SysCmd5 | 78 | Int3* | 130 | V _{cc} | 182 | TCK |
| 27 | SysADC4 | 79 | V _{ss} | 131 | V _{ss} | 183 | TMS |
| 28 | SysADC0 | 80 | V _{cc} | 132 | SysADC2 | 184 | TDO |
| 29 | V _{ss} | 81 | Int2* | 133 | SysADC6 | 185 | V _{cc} P |
| 30 | V _{cc} | 82 | SysAD16 | 134 | SysAD24 | 186 | V _{ss} P |
| 31 | SysCmd4 | 83 | SysAD48 | 135 | V _{cc} | 187 | SysClock |
| 32 | SysAD39 | 84 | Int1* | 136 | V _{ss} | 188 | V _{cc} |
| 33 | SysAD7 | 85 | V _{ss} | 137 | SysAD56 | 189 | V _{ss} |

Table 6 RC64575 208-pin QFP Package Pin-Out (Page 1 of 2)

| Pin | Function | Pin | Function | Pin | Function | Pin | Function |
|-----|-----------------|-----|-----------------|-----|--------------------|-----|-----------------|
| 34 | SysCmd3 | 86 | V _{CC} | 138 | SysAD25 | 190 | SysADC5 |
| 35 | V _{SS} | 87 | SysAD17 | 139 | SysAD57 | 191 | SysADC1 |
| 36 | V _{CC} | 88 | SysAD49 | 140 | V _{CC} | 192 | V _{CC} |
| 37 | SysAD38 | 89 | Int0* | 141 | V _{SS} | 193 | V _{SS} |
| 38 | SysAD6 | 90 | SysAD18 | 142 | N.C. | 194 | SysAD47 |
| 39 | ModeClock | 91 | V _{SS} | 143 | SysAD26 | 195 | SysAD15 |
| 40 | WrRdy* | 92 | V _{CC} | 144 | SysAD58 | 196 | SysAD46 |
| 41 | SysAD37 | 93 | SysAD50 | 145 | N.C. | 197 | V _{CC} |
| 42 | SysAD5 | 94 | ValidIn* | 146 | V _{CC} | 198 | V _{SS} |
| 43 | V _{SS} | 95 | SysAD19 | 147 | V _{SS} | 199 | SysAD14 |
| 44 | V _{CC} | 96 | SysAD51 | 148 | SysAD27 | 200 | SysAD45 |
| 45 | N.C. | 97 | V _{SS} | 149 | N.C. | 201 | SysAD13 |
| 46 | N.C. | 98 | V _{CC} | 150 | JR_V _{CC} | 202 | SysAD44 |
| 47 | N.C. | 99 | ValidOut* | 151 | N.C. | 203 | V _{SS} |
| 48 | N.C. | 100 | SysAD20 | 152 | N.C. | 204 | V _{CC} |
| 49 | N.C. | 101 | N.C. | 153 | N.C. | 205 | SysAD12 |
| 50 | N.C. | 102 | N.C. | 154 | N.C. | 206 | SysCmdP |
| 51 | N.C. | 103 | N.C. | 155 | N.C. | 207 | SysAD43 |
| 52 | N.C. | 104 | N.C. | 156 | N.C. | 208 | N.C. |

Table 6 RC64575 208-pin QFP Package Pin-Out (Page 2 of 2)

RC64574 128-pin Package Pin-out

N.C. pins should be left floating for maximum flexibility as well as for compatibility with future designs. An asterisk (*) identifies a pin that is active when low.

| Pin | Function | Pin | Function | Pin | Function | Pin | Function |
|-----|-----------------|-----|--------------------|-----|--------------------|-----|-----------------|
| 1 | JTAG32* | 33 | V _{CC} | 65 | V _{CC} | 97 | V _{CC} |
| 2 | SysCmd2 | 34 | V _{SS} | 66 | SysAD28 | 98 | V _{SS} |
| 3 | V _{CC} | 35 | SysAD13 | 67 | ColdReset* | 99 | SysAD19 |
| 4 | V _{SS} | 36 | SysAD14 | 68 | SysAD27 | 100 | ValidIn* |
| 5 | SysAD5 | 37 | V _{SS} | 69 | V _{SS} | 101 | V _{CC} |
| 6 | WrRdy* | 38 | V _{CC} | 70 | V _{CC} | 102 | V _{SS} |
| 7 | ModeClock | 39 | SysAD15 | 71 | JR_V _{CC} | 103 | SysAD18 |
| 8 | SysAD6 | 40 | V _{SS} | 72 | SysAD26 | 104 | Int0* |
| 9 | V _{CC} | 41 | V _{CC} | 73 | N.C. | 105 | SysAD17 |
| 10 | V _{SS} | 42 | SysADC1 | 74 | V _{SS} | 106 | V _{CC} |
| 11 | SysCmd3 | 43 | V _{SS} | 75 | N.C. | 107 | V _{SS} |
| 12 | SysAD7 | 44 | V _{CC} | 76 | SysAD25 | 108 | Int1* |
| 13 | SysCmd4 | 45 | SysClock | 77 | V _{SS} | 109 | SysAD16 |
| 14 | V _{CC} | 46 | V _{SS} P | 78 | V _{CC} | 110 | Int2* |
| 15 | V _{SS} | 47 | V _{CC} P | 79 | SysAD24 | 111 | V _{CC} |
| 16 | SysADC0 | 48 | TDO | 80 | SysADC2 | 112 | V _{SS} |
| 17 | SysCmd5 | 49 | TMS | 81 | V _{SS} | 113 | Int3* |
| 18 | SysAD8 | 50 | TCK | 82 | V _{CC} | 114 | SysAD0 |
| 19 | V _{CC} | 51 | TRst* | 83 | NMI* | 115 | Int4* |
| 20 | V _{SS} | 52 | TDI | 84 | SysAD23 | 116 | V _{CC} |
| 21 | SysCmd6 | 53 | V _{SS} | 85 | Release* | 117 | V _{SS} |
| 22 | SysAD9 | 54 | SysADC3 | 86 | V _{SS} | 118 | SysAD1 |
| 23 | V _{CC} | 55 | V _{CC} OK | 87 | V _{CC} | 119 | Int5* |
| 24 | V _{SS} | 56 | V _{SS} | 88 | SysAD22 | 120 | SysAD2 |
| 25 | SysCmd7 | 57 | V _{CC} | 89 | ModeIn | 121 | V _{CC} |
| 26 | SysAD10 | 58 | SysAD31 | 90 | RdRdy* | 122 | V _{SS} |
| 27 | SysCmd8 | 59 | V _{SS} | 91 | SysAD21 | 123 | SysCmd0 |
| 28 | V _{CC} | 60 | V _{CC} | 92 | V _{SS} | 124 | SysAD3 |
| 29 | V _{SS} | 61 | SysAD30 | 93 | V _{CC} | 125 | V _{CC} |
| 30 | SysAD11 | 62 | SysAD29 | 94 | ExtRqst* | 126 | V _{SS} |
| 31 | SysCmdP | 63 | Reset* | 95 | SysAD20 | 127 | SysCmd1 |
| 32 | SysAD12 | 64 | V _{SS} | 96 | ValidOut* | 128 | SysAD4 |

Table 7 RC64574 128-Pin Package

RC64574 Socket Compatibility to RC64474 & RC4640

The RC64574/575 is 100% pin compatible with the RC64474/475 with the supply voltage being the only difference. RC64474/475 requires a 3.3V supply, while RC64574/575 requires a 2.5V supply.

To ensure socket compatibility between the RC64574/RC64474 and the RC4640 devices, several pin changes are required, as shown in the tables below. **Note:** The RC64574/575 are 2.5V parts and as such all V_{cc} must be at the correct voltage for a given part.

| Pin | RC4640 | RC64574/ RC64474 | Compatible to RV4640? | Comments |
|-----|-----------------|---------------------|--------------------------|---|
| 1 | N.C | JTAG32* | Yes | Pin has an internal pull-down, to enable 32-bit scan. Can also be left a N.C. |
| 48 | V _{SS} | TDO | Yes | Can be driven with V _{SS} , if JTAG is not needed. Is tristated when TRst* is low. |
| 49 | V _{SS} | TMS | Yes | Can be driven with V _{SS} if JTAG is not needed. |
| 50 | V _{SS} | TCK | Yes | Can be driven with V _{SS} if JTAG is not needed. |
| 51 | V _{SS} | TRst* | Yes | Can be driven with V _{SS} if JTAG is not needed. |
| 52 | V _{SS} | TDI | Yes | Can be driven with V _{SS} if JTAG is not needed. |
| 71 | N.C. | JR_V _{CC} | Yes | Can be left N.C. in RC64574, if JTAG is not need. If JTAG is needed, it must be driven to V _{CC} . |

Table 8 RC64574 Socket Compatibility to RC64474 and R4640

RC64575 Socket Compatibility to RC64475 & RC4650

| Pin | RV4650 32-bit | RC64575 32-bit RC64475 32-bit | RV4650 64-bit | RC64575 64-bit RC64475 64-bit | Compatible to RV4650? | Comments |
|-----|------------------|--|------------------|--|--------------------------|---|
| 53 | N.C. | JTAG32* | No Connect | JTAG32* | Yes | In 32-bit, this pin can be left unconnected because of internal pull-down. In 64-bit, this assumes that JTAG will not be used. If using JTAG, this pin must be at V _{CC} . |
| 150 | N.C. | JR_V _{CC} | No Connect | JR_V _{CC} | Yes | In RC64475, can be left a N.C, if JTAG is not need. If JTAG is needed, it must be driven to V _{CC} . |
| 180 | N.C. | TDI | No Connect | TDO | Yes | If JTAG is not needed, can be left a N.C. |
| 181 | N.C. | TRsT* | No Connect | TRsT* | Yes | If JTAG is not needed, can be left a N.C. |
| 182 | N.C. | TCK | No Connect | TCK | Yes | If JTAG is not needed, can be left a N.C. |
| 183 | N.C. | TMS | No Connect | TMS | Yes | If JTAG is not needed, can be left a N.C. |
| 184 | N.C. | TDO | No Connect | TDIO | Yes | If JTAG is not needed, can be left a N.C. |

Table 9 RC64575 Socket Compatibility to RC64475 & RC4650

Absolute Maximum Ratings

Note: Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

| Symbol | Rating | Commercial (2.5V±5%) | Industrial (2.5V±5%) | Unit |
|--------------|--------------------------------------|---------------------------|---------------------------|------|
| V_{TERM} | Terminal Voltage with respect to GND | -0.5 ¹ to +4.0 | -0.5 ¹ to +4.0 | V |
| T_C | Operating Temperature (case) | 0 to +85 | -40 to +85 | °C |
| T_{BIAS}^2 | Case Temperature Under Bias | -55 to +125 | -55 to +125 | °C |
| T_{STG} | Storage Temperature | -55 to +125 | -55 to +125 | °C |
| I_{IN} | DC Input Current | 20 ³ | 20 ³ | mA |
| I_{OUT} | DC Output Current | 50 ⁴ | 50 ⁴ | mA |

¹. V_{IN} minimum = -2.0V for pulse width less than 15ns. For 3.3V tolerant input, V_{IN} maximum is 3.8V.

². Case temperature when device is powered up but not operating.

³. When $V_{IN} < 0V$ or $V_{IN} > V_{CC}$.

⁴. Not more than one output should be shorted at a time. Duration of the short should not exceed 30 seconds.

Recommended Operation Temperature and Supply Voltage

| Grade | Temperature | GND | RC64574/575 |
|------------|-----------------------|-----|-----------------|
| | | | V _{CC} |
| Commercial | 0°C to +85°C (Case) | 0V | 2.5V±5% |
| Industrial | -40°C to +85°C (Case) | 0V | 2.5V±5% |

DC Electrical Characteristics

Commercial Temperature Range—RC64574/575

($T_{case} = 0^\circ\text{C}$ to $+85^\circ\text{C}$ Commercial, $T_{case} = -40^\circ\text{C}$ to $+85^\circ\text{C}$ Industrial, $V_{CC} = 2.5V \pm 5\%$)

| Parameter | RC64574/RC64575 200MHz | | RC64574/RC64575 250MHz | | Conditions |
|-----------|---------------------------|---------------------|---------------------------|---------------------|-----------------------------|
| | Min | Max | Min | Max | |
| V_{OL} | — | 0.1V | — | 0.1V | $ I_{OUT} = 20\mu\text{A}$ |
| V_{OH} | $V_{CC} - 0.1V$ | — | $V_{CC} - 0.1V$ | — | |
| V_{OL} | — | 0.4V | — | 0.4V | $ I_{OUT} = 4\text{mA}$ |
| V_{OH} | 2.0V | — | 2.0V | — | |
| V_{IL} | -0.5V | $0.2V_{CC}$ | -0.5V | $0.2V_{CC}$ | — |
| V_{IH} | $0.7V_{CC}$ | 3.8V | $0.7V_{CC}$ | 3.8V | — |
| I_{IN} | — | $\pm 10\mu\text{A}$ | — | $\pm 10\mu\text{A}$ | $0 \leq V_{IN} \leq V_{CC}$ |
| C_{IN} | — | 10pF | — | 10pF | — |

| Parameter | RC64574/RC64575 200MHz | | RC64574/RC64575 250MHz | | Conditions |
|---------------------|---------------------------|------|---------------------------|------|----------------------|
| | Min | Max | Min | Max | |
| C _{IO} | — | 10pF | — | 10pF | — |
| C _{clk} | — | 10pF | — | 10pF | |
| I/O _{LEAK} | — | 20uA | — | 20uA | Input/Output Leakage |

Power Consumption—RC64574

Note: The following table assumes as 4:1 pipeline to bus clock ratio.

| Parameter | | RC64574 200MHz | | RC64574 250MHz | | Conditions |
|-----------------|----------|----------------------|---------------------|----------------------|---------------------|--|
| | | Typical ¹ | Max | Typical ¹ | Max | |
| I _{CC} | stand-by | — | 60 mA ² | — | 60 mA ² | C _L = 0pF ³ |
| | | — | 120 mA ² | — | 120 mA ² | C _L = 50pF |
| | active | 470 mA ² | 550 mA ² | 550 mA ² | 680 mA ² | C _L = 0pF No SysAd activity ³ V _{CC} = 2.63V |
| | | 550 mA ² | 650 mA ² | 650 mA ² | 800 mA ² | C _L = 50pF R4x00 compatible writes, T _C = 25°C V _{CC} = 2.63V |
| | | 600 mA ² | 715 mA ⁴ | 715 mA ² | 880 mA ⁴ | C _L = 50pF Pipelined writes or write re-issue, T _C = 25°C ³ V _{CC} = 2.63V |

¹ Typical integer instruction mix and cache miss rates.

² These are not tested. They are the results of engineering analysis and are provided for reference only.

³ Guaranteed by design.

⁴ These are the specifications IDT tests to insure compliance.

RC64574 Power Curves

The following two graphs contain power curves that show power consumption at various bus frequencies. Power consumption is based on the values for R4x00 compatible write mode, shown in the table above.

Note: Only pipeline frequencies that are integer multiples (2x, 3x, etc.) of bus frequencies are supported.

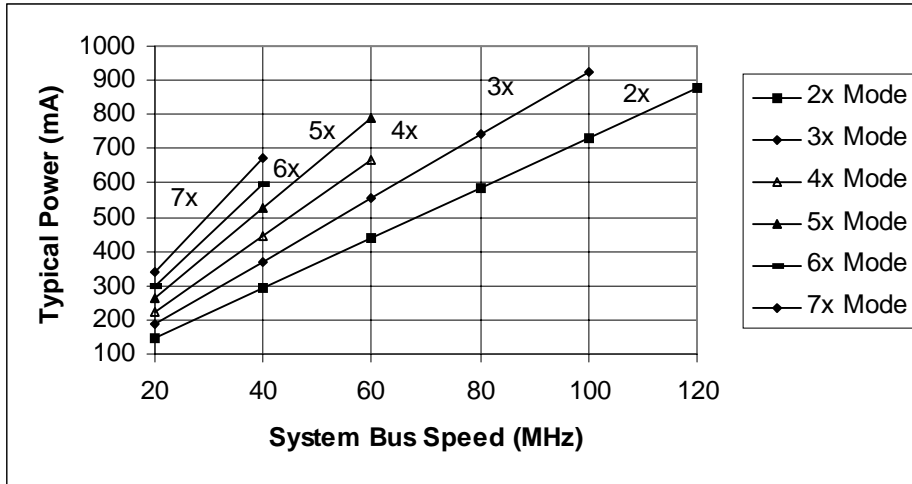


Figure 2 Typical Power Usage - RC64574

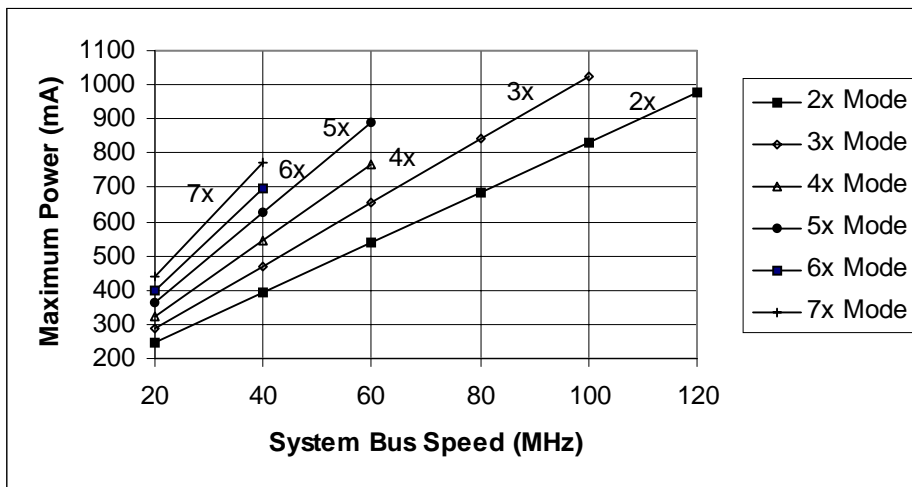


Figure 3 Maximum Power Usage - RC64574

Power Consumption—RC64575

Note: The following table assumes a 4:1 pipeline to bus clock ratio.

| Parameter | | RC64575 200MHz | | RC64575 250MHz | | Conditions |
|-----------------|--|----------------------|---------------------|----------------------|----------------------|---|
| | | Typical ¹ | Max | Typical ¹ | Max | |
| I _{CC} | stand-by | — | 60 mA ² | — | 60 mA ² | C _L = 0pF ³ |
| | | — | 120 mA ² | — | 120 mA ² | C _L = 50pF |
| | active, 64-bit bus option ⁴ | 510 mA ² | 680 mA ² | 600 mA ² | 810 mA ² | C _L = 0pF No SysAd activity ³ V _{CC} = 2.63V |
| | | 600 mA ² | 800 mA ² | 700 mA ² | 950 mA ² | C _L = 50pF R4x00 compatible writes, T _C = 25°C V _{CC} = 2.63V |
| | | 660 mA ² | 880 mA ⁵ | 770 mA ² | 1050 mA ⁵ | C _L = 50pF Pipelined writes or write re-issue, T _C = 25°C ³ V _{CC} = 2.63V |

- ¹ Typical integer instruction mix and cache miss rates.
- ² These are not tested. They are the results of engineering analysis and are provided for reference only.
- ³ Guaranteed by design.
- ⁴ In 32-bit bus option, use RC64574 power consumption values.
- ⁵ These are the specifications IDT tests to insure compliance.

RC64575 Power Curves

The following two graphs contain power curves that show power consumption at various bus frequencies. Power consumption is based on the values for R4x00 compatible write mode, shown in the table above.

Note: Only pipeline frequencies that are integer multiples (2x, 3x, etc.) of bus frequencies are supported.

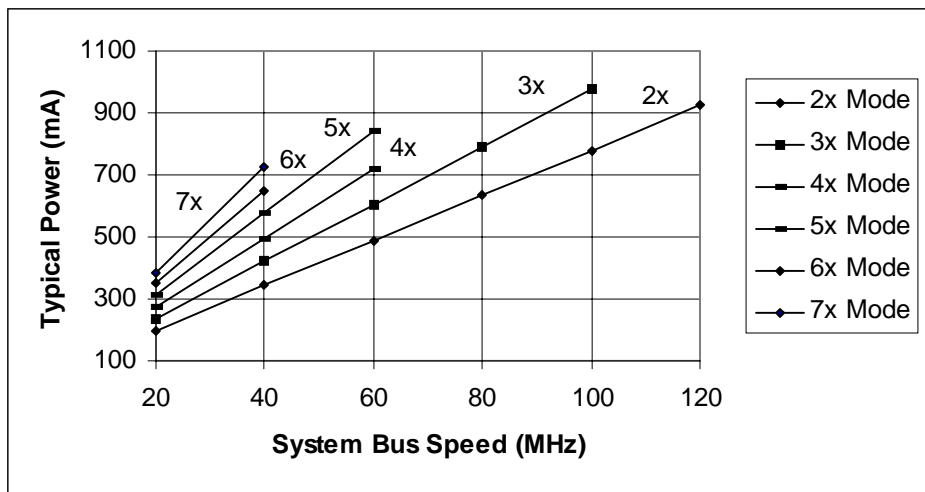


Figure 4 Typical Power Usage - RC64575

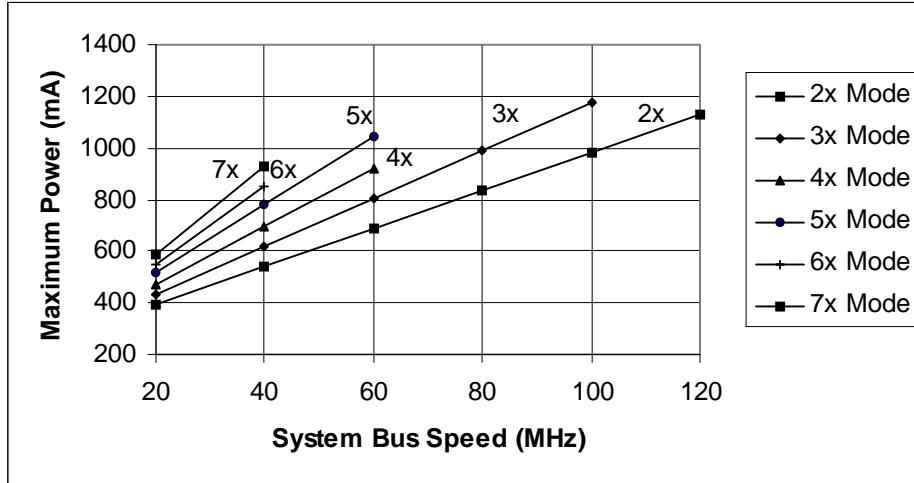


Figure 5 Maximum Power Usage - RC64575

Timing Characteristics—RC64574/RC64575

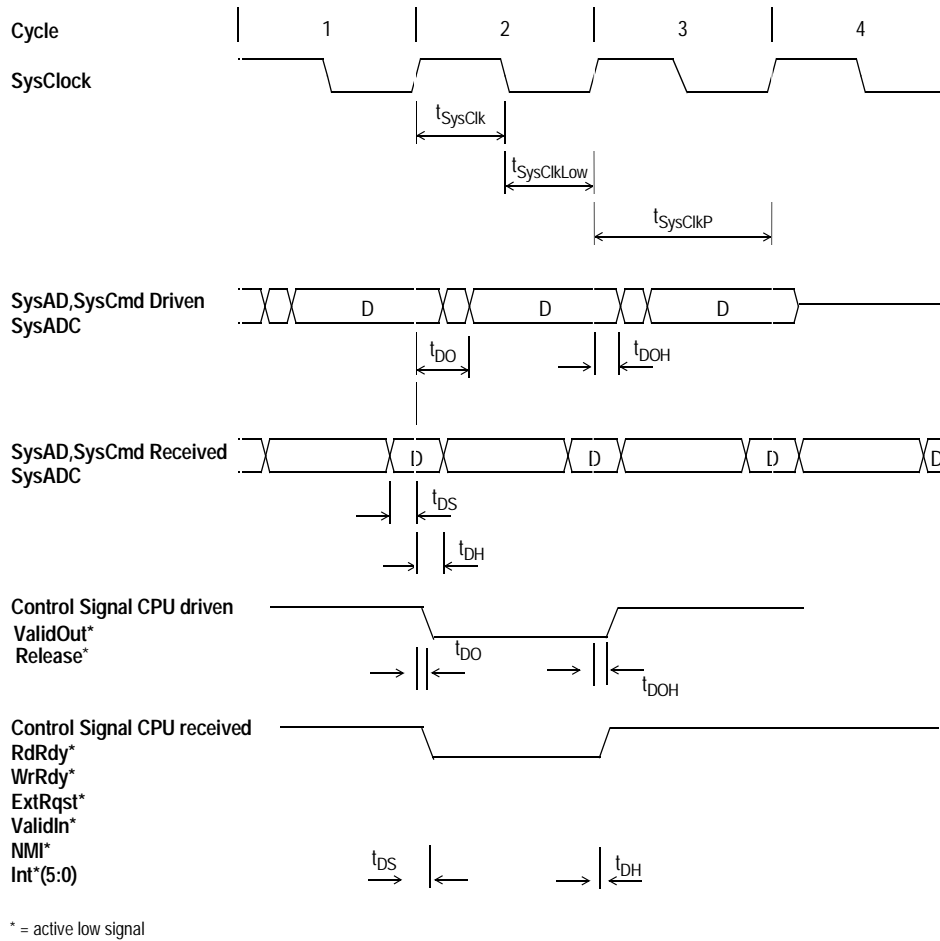


Figure 6 System Clocks Data Setup, Output, and Hold Timing

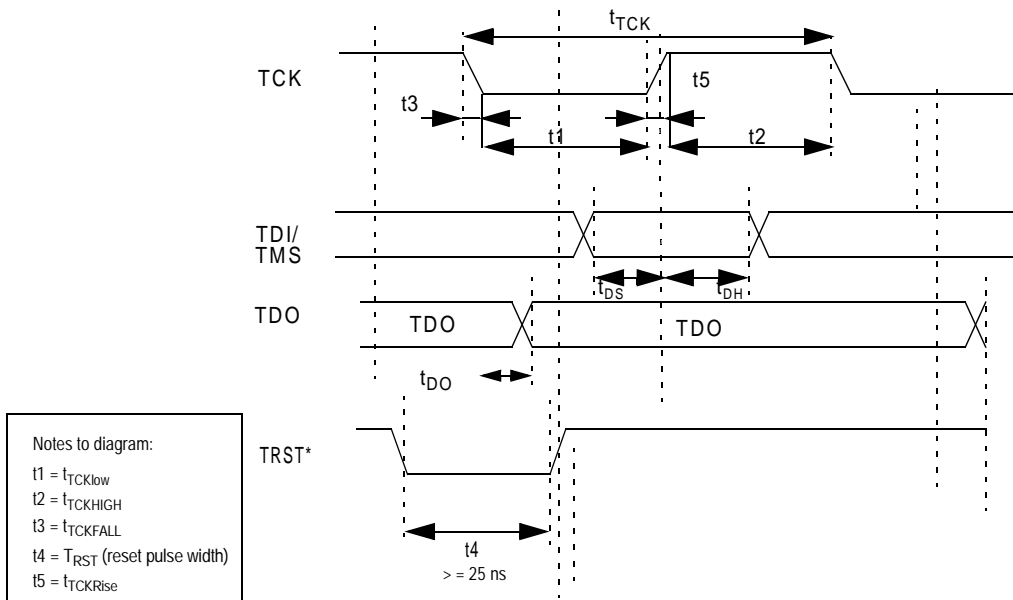


Figure 7 Standard JTAG Timing

System Interface Parameters

| Parameter | Symbol | Test Conditions | RC64574/ RC64575 | | RC64574/ RC64575 | | Units |
|------------------|-----------------------|--|---------------------|-----|---------------------|-----|-------|
| | | | 200MHz | | 250MHz | | |
| | | | Min | Max | Min | Max | |
| Data Output | $t_{DO} = \text{Max}$ | mode _{14..13} = 10 (Fastest) | — | 5 | — | 4.3 | ns |
| | | mode _{14..13} = 11 (85%) | — | 6 | — | 4.5 | ns |
| | | mode _{14..13} = 00 (66%) | — | 7 | — | 5 | ns |
| | | mode _{14..13} = 01 (Slowest) | — | 8 | — | 5 | ns |
| Data Output Hold | t_{DOH}^1 | mode _{14..13} = 10 | 0 | — | 0 | — | ns |
| | | mode _{14..13} = 11 | 0 | — | 0 | — | ns |
| | | mode _{14..13} = 00 | 0 | — | 0 | — | ns |
| | | mode _{14..13} = 01 | 0 | — | 0 | — | ns |
| Data Input | t_{DS} | $t_{rise} = 3\text{ns}$ | 2 | — | 2 | — | ns |
| | t_{DH} | $t_{fall} = 3\text{ns}$ | 1.0 | — | 1.0 | — | ns |

¹. 50 pf loading on external output signals

Boot-time Interface Parameters

| Parameter | Symbol | Test Conditions | RC64574/ RC64575 | | RC64574/ RC64575 | | Conditions |
|-----------------|----------|-----------------|---------------------|-----|---------------------|-----|----------------|
| | | | 200MHz | | 250MHz | | |
| | | | Min | Max | Min | Max | |
| Mode Data Setup | t_{DS} | — | 4 | — | 4 | — | SysClock Cycle |
| Mode Data Hold | t_{DH} | — | 0 | — | 0 | — | SysClock Cycle |

Mode Configuration Interface Reset Sequence

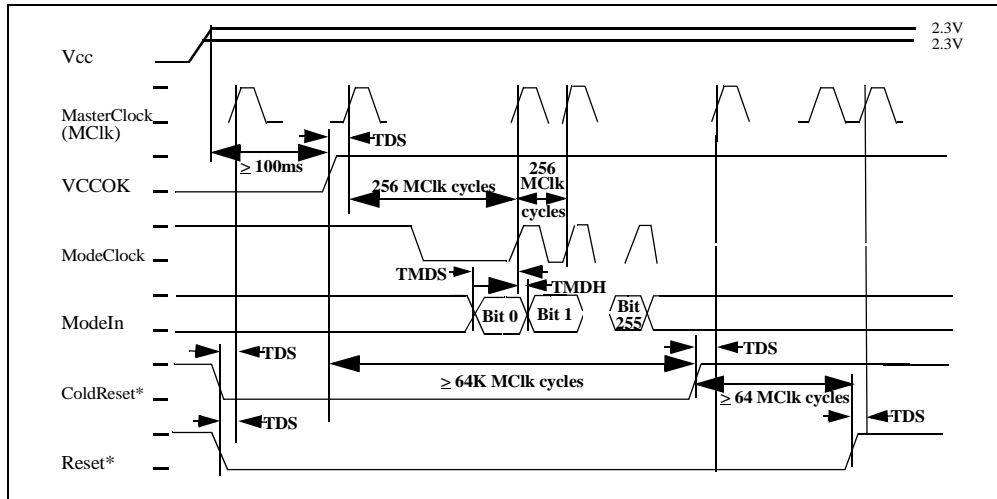


Figure 8 Power-on Reset

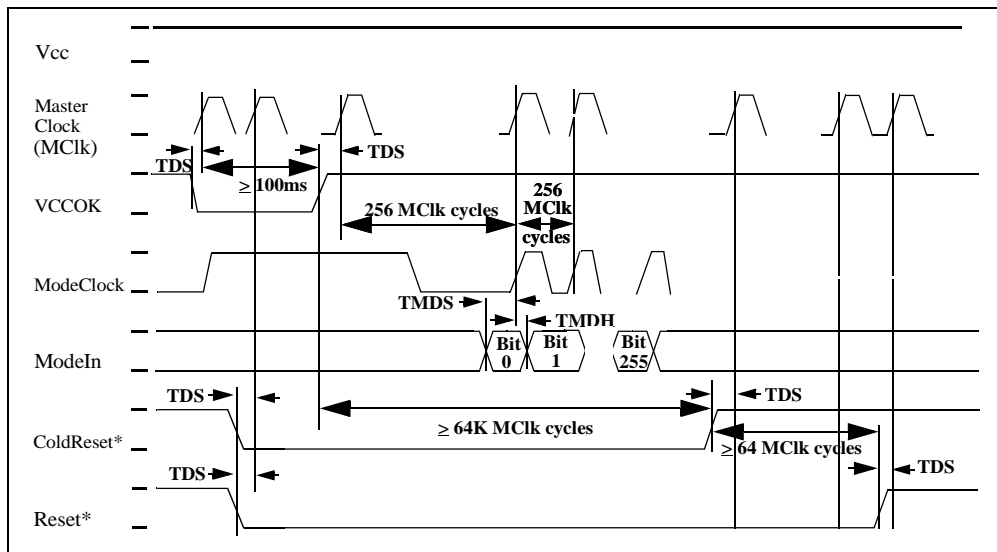


Figure 9 Cold Reset

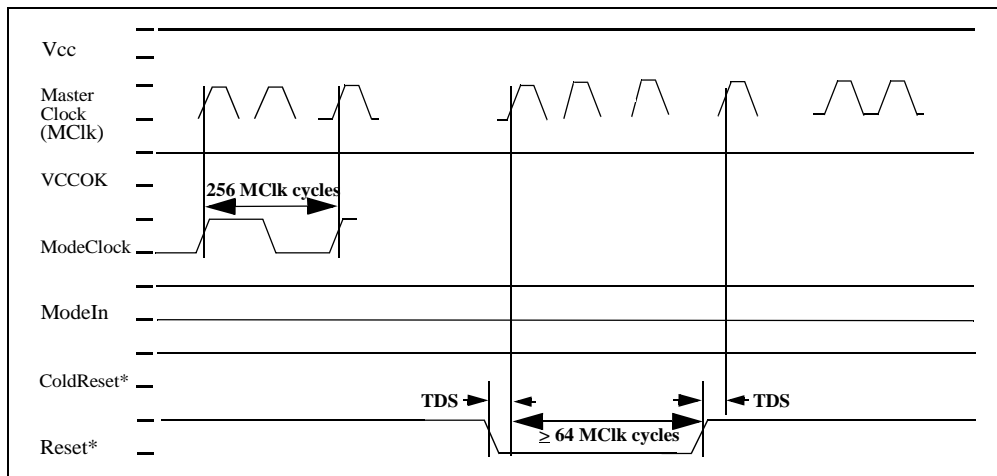


Figure 10 Warm Reset

AC Electrical Characteristics

($T_{\text{case}} = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ Commercial, $T_{\text{case}} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ Industrial, $V_{\text{CC}} = 2.5\text{V} \pm 5\%$)

Clock Parameters—RC64574/575

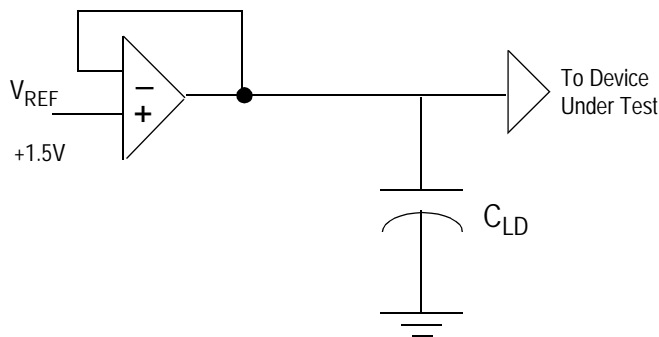
| Parameter | Symbol | Test Conditions | RC64574/RC64575 200MHz | | RC64574/RC64575 250MHz | | Units |
|-------------------------------------|----------------------|------------------------------|---------------------------|----------------------|---------------------------|----------------------|-------|
| | | | Min | Max | Min | Max | |
| Pipeline Clock Frequency | PCLk | — | 100 | 200 | 100 | 250 | MHz |
| System Clock HIGH | t_{SCHIGH} | Transition $\leq 3\text{ns}$ | 3 | — | 3 | — | ns |
| System Clock LOW | t_{SCLow} | Transition $\leq 3\text{ns}$ | 3 | — | 3 | — | ns |
| System Clock Frequency | — | — | 33 | 100 | 33 | 125 | MHz |
| System Clock Period | t_{SCP} | — | 10 | 30 | 8 | 30 | ns |
| System Clock Jitter | t_{JITTER} | — | — | ± 250 | — | ± 250 | ps |
| System Clock Rise Time ¹ | t_{SCRise} | — | — | 2 | — | 2 | ns |
| System Clock Fall Time ¹ | t_{SCFall} | — | — | 2 | — | 2 | ns |
| ModeClock Period | t_{ModeCKP} | — | — | $256 t_{\text{SCP}}$ | — | $256 t_{\text{SCP}}$ | ns |
| JTAG Clock Input Period | t_{TCK} | — | — | 100 | — | 100 | ns |
| JTAG Clock HIGH | t_{TCKHIGH} | — | — | 40 | — | 40 | ns |
| JTAG Clock Low | t_{TCKLOW} | — | — | 40 | — | 40 | ns |
| JTAG Clock Rise Time | t_{TCKRise} | — | — | 5 | — | 5 | ns |
| JTAG Clock Fall Time | t_{TCKFall} | — | — | 5 | — | 5 | ns |

¹ Rise and Fall times are measured between 10% and 90%

Capacitive Load Deration—RC64574/575

| Parameter | Symbol | Test Conditions | 200MHz | | 250MHz | | Units |
|-------------|-----------------|-----------------|--------|-----|--------|-----|---------|
| | | | Min | Max | Min | Max | |
| Load Derate | C_{LD} | — | — | 2 | — | 2 | ns/25pF |

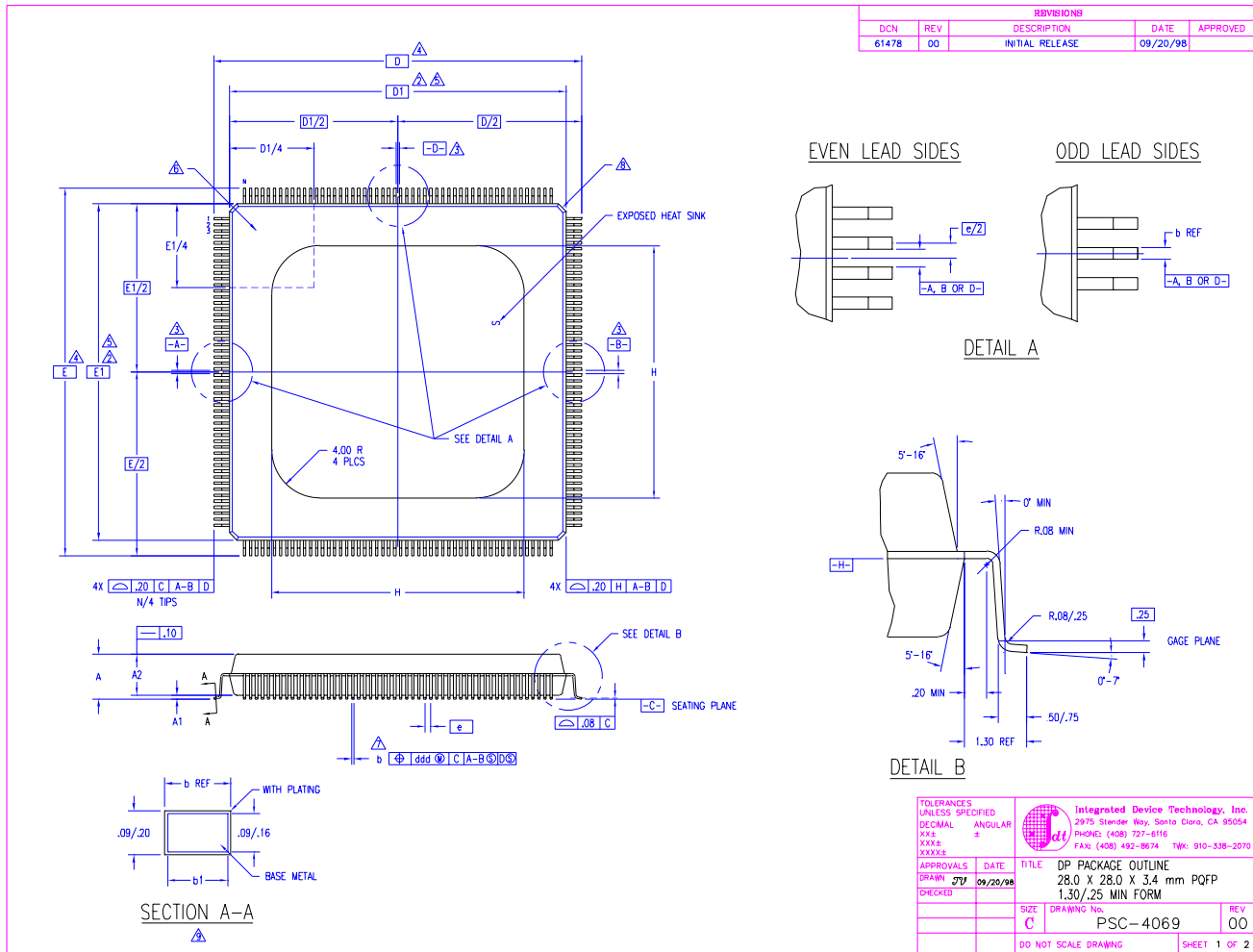
Output Loading for AC Testing



| Signal | Cld |
|-------------|-------|
| All Signals | 50 pF |

RC64575 208-pin Package Diagram

The RC64575 is available in a 208-pin QFP package.

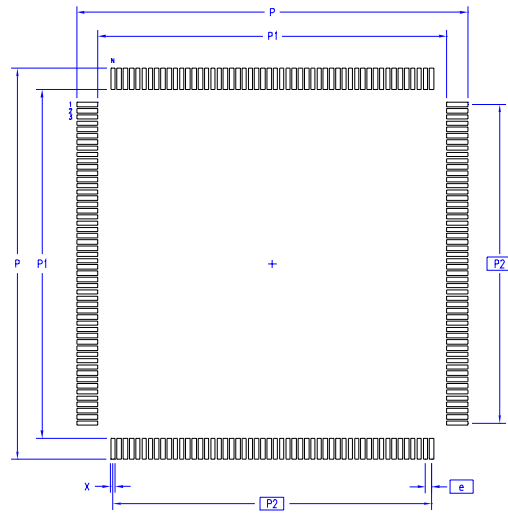


RC64575 208-pin Package Diagram (page2)

| REVISIONS | | | | |
|-----------|-----|-----------------|----------|----------|
| DCN | REV | DESCRIPTION | DATE | APPROVED |
| 61478 | 00 | INITIAL RELEASE | 09/20/98 | |

| SYMBOL | JEDEC VARIATION | | | NOTE |
|--------|-----------------|------|------|------|
| | FA-1 | | | |
| | MIN | NOM | MAX | |
| A | - | - | 4.10 | |
| A1 | .25 | - | - | |
| A2 | 3.20 | 3.40 | 3.60 | |
| D | 30.60 BSC | | 4 | |
| D1 | 28.00 BSC | | 5,2 | |
| E | 30.60 BSC | | 4 | |
| E1 | 28.00 BSC | | 5,2 | |
| H | 21.00 REF | | | |
| N | 208 | | | |
| e | .50 BSC | | | |
| b | .17 | - | .27 | 7 |
| b1 | .17 | .20 | .23 | |
| ddd | - | - | .08 | |


LAND PATTERN DIMENSIONS



| | MIN | MAX |
|----|-----------|-------|
| P | 31.20 | 31.40 |
| P1 | 27.80 | 28.00 |
| P2 | 25.50 BSC | |
| X | .30 | .40 |
| e | .50 BSC | |
| N | 208 | |

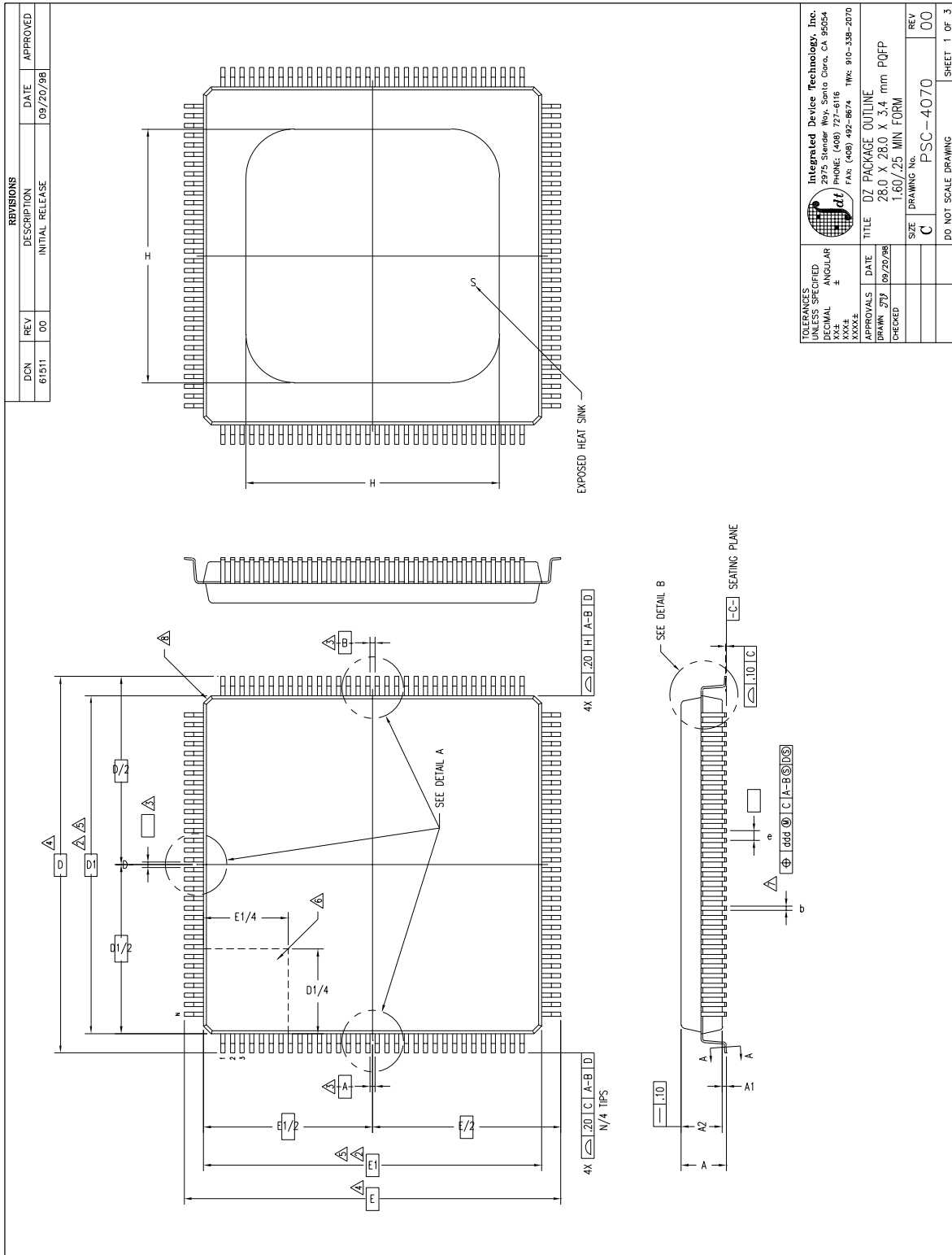
NOTES:

- 1 ALL DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M-1994
- ⚠ TOP PACKAGE MAY BE SMALLER THAN BOTTOM PACKAGE BY .15 mm
- ⚠ DATUMS [A-B] AND [-D-] TO BE DETERMINED AT DATUM PLANE [-H-]
- ⚠ DIMENSIONS D AND E ARE TO BE DETERMINED AT SEATING PLANE [-C-]
- ⚠ DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS .25 mm PER SIDE. D1 AND E1 ARE BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH
- ⚠ DETAIL OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED
- ⚠ DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .08 mm IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.
- ⚠ EXACT SHAPE OF EACH CORNER IS OPTIONAL
- ⚠ THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .10 AND .25 mm FROM THE LEAD TIP
- 10 ALL DIMENSIONS ARE IN MILLIMETERS
- 11 THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-143, VARIATION FA-1

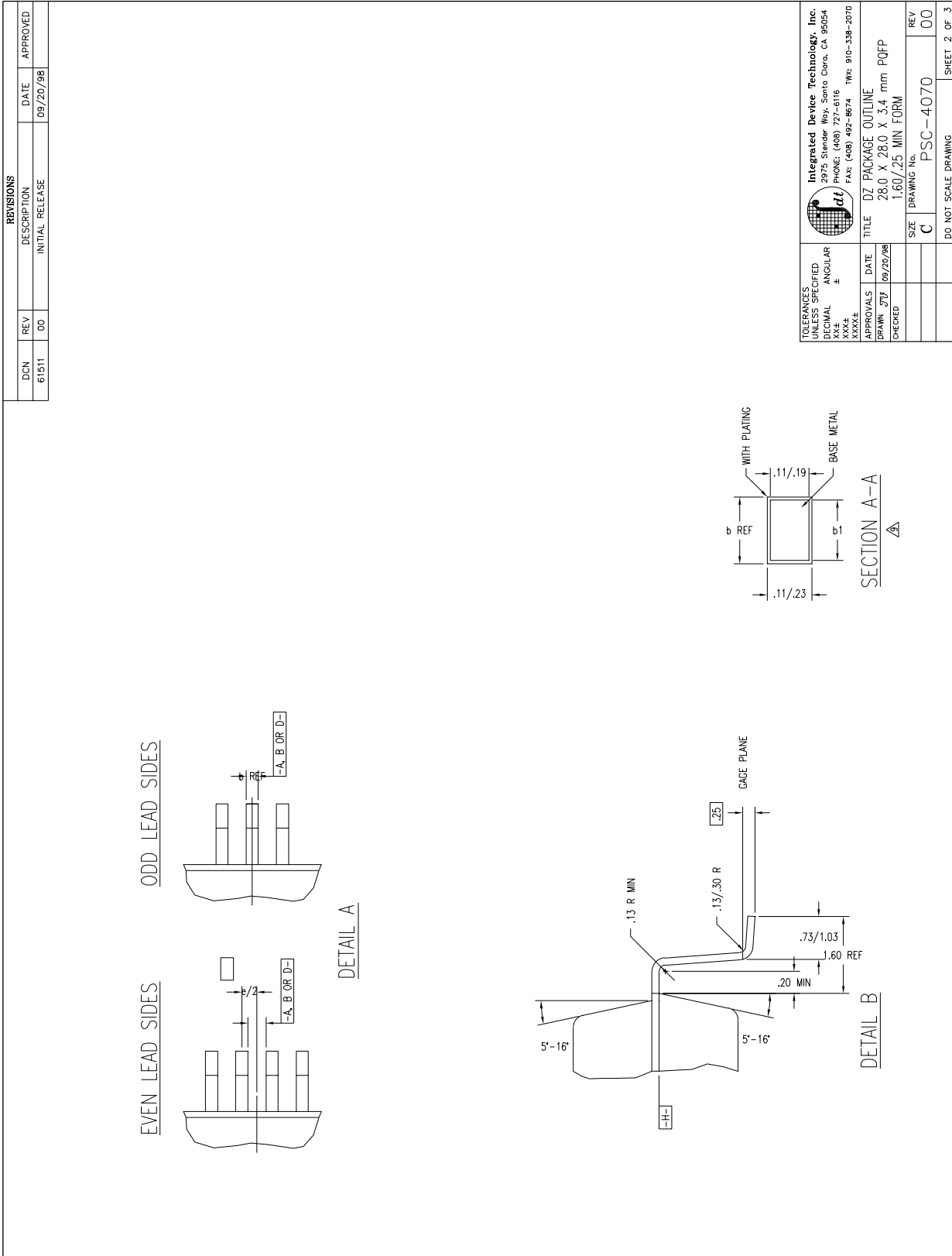
| | | |
|-----------------------------|----------|---|
| TOLERANCES UNLESS SPECIFIED | |  Integrated Device Technology, Inc. 2975 Slender Way, Santa Clara, CA 95054 PHONE: (408) 727-6116 FAX: (408) 492-8674 TRN: 910-338-2070 |
| DECIMAL | ANGULAR | |
| xxx± | ± | |
| xxxx | | |
| xxxxx | | |
| APPROVALS | DATE | TITLE |
| DRAWN <i>DT</i> | 09/20/98 | DP PACKAGE OUTLINE |
| CHECKED | | 28.0 X 28.0 X 3.4 mm PQFP |
| | | 1.30/.25 MIN FORM |
| | SIZE | DRAWING No. |
| | C | PSC-4069 |
| | | REV |
| | | 00 |
| DO NOT SCALE DRAWING | | SHEET 2 OF 2 |

RC64574 128-pin Package Diagram (page 1 of 3)

The RC64574 is available in a 128-pin QFP package.



RC64574 128-pin Package Diagram (page 2 of 3)





CORPORATE HEADQUARTERS

2975 Stender Way
Santa Clara, CA 95054

for SALES:

800-345-7015 or 408-727-6116
fax: 408-330-1748
www.idt.com

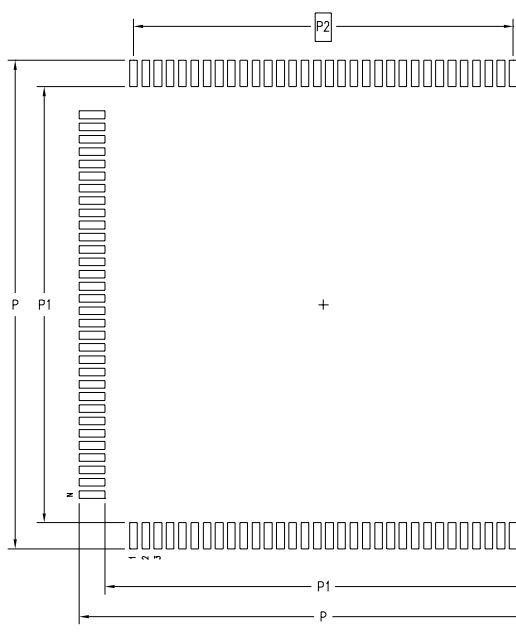
for Tech Support:

email: rischelp@idt.com
phone: 408-492-8208

Ordering Information

| REVISIONS | | |
|-----------|-----|-----------------|
| DCN | REV | DATE |
| 61511 | 00 | 09/20/98 |
| | | INITIAL RELEASE |
| | | APPROVED |

LAND PATTERN DIMENSIONS



IDT79RCXX YY

Product Type

Operating Voltage

| | MIN | MAX |
|----|-------|-------|
| P | 31.80 | 32.00 |
| P1 | 28.40 | 28.60 |
| P2 | 24.80 | BSC |
| X | .40 | .60 |
| e | .80 | BSC |
| N | | 128 |

| | |
|---|---------------------------|
| Integrated Device Technology, Inc. 2975 Steiner Way, San Jose, CA 95054 PHONE: (408) 729-2100 FAX: (408) 729-2101 | |
| TOLERANCES UNLESS SPECIFIED | DECIMAL |
| ANGULAR | ± |
| APPROVALS | DATE |
| DRAWN | JYJ 09/20/98 |
| CHECKED | |
| TITLE | DZ PACKAGE OUTLINE |
| SIZE | 28.0 X 28.0 X 3.4 mm PQFP |
| REV | 00 |
| DRAWING NO. | PSC-4070 |
| DO NOT SCALE DRAWING | |
| SHEET | 3 OF 3 |

999 Speed
A Package

| SYMBOL | JEDEC VARIATION | | N |
|--------|-----------------|------|-------|
| | DB-1 | MAX | |
| D | MIN | MAX | |
| A | -.25 | - | 4, 10 |
| A2 | 3.20 | 3.40 | 3.60 |
| D | 31.20 BSC | | 4 |
| D1 | 28.00 BSC | | 5.2 |
| E | 31.20 BSC | | 4 |
| E1 | 28.00 BSC | | 5.2 |
| H | 21.00 REF | | |
| N | | | 128 |
| e | .80 BSC | | |
| b | .29 | - | .45 |
| b1 | .29 | .35 | .41 |
| ddd | - | - | .20 |

NOTES:

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- DIMENSIONS D AND E ARE TO BE DETERMINED AT SEATING PLANE [-C-]
- DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS .08 mm PER SIDE. DIMENSIONS D AND E1 ARE BODY SIZE DIMENSIONS INCLUDING MOLD PROTRUSION.
- DETAIL OF PIN IDENTIFICATION IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED
- DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .08 mm PER SIDE. DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.
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- THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .10 AND .25 mm FROM THE LEAD TIP
- ALL DIMENSIONS ARE IN MILLIMETERS
- THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MS-022, VARIATION DB-1

Valid Combinations

- DT-79RC64574 250, DP
- DT-79RC64575 250, DP
- DT-79RC64574 250, DZ
- DT-79RC64575 250, DZ
- DT-79RC64574 250, DZ
- DT-79RC64575 250, DZ

- 128-pin QFP package, Commercial
- 208-pin QFP package, Commercial
- 128-pin QFP package, Industrial T
- 08-pin QFP package, Industrial Te



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