# 5V µP Power Supply Monitor and Reset Circuit

## – Selectable Trip-Point Tolerance and Watchdog Period

## – Push-Button Reset

The IMP1232LP/LPS microprocessor supervisor can halt and restart a "hung-up" or "stalled" microprocessor, restart a microprocessor after a power failure, and debounce and interface a manual push-button microprocessor reset switch. The low-power supervisors feature 40% lower supply current than the pin compatible Dallas Semiconductor DS1232LP/LPS.

Precision temperature compensated reference and comparator circuits monitor the 5V, $V_{CC}$ input voltage. During power-up or when the $V_{CC}$ power supply falls outside selectable tolerance limits, both the RESET and $\overline{\text{RESET}}$ become active. When $V_{CC}$ rises above the threshold voltage, the reset signals remain active for an additional 250ms minimum, allowing the power supply and system microprocessor to stabilize. The trip point tolerance signal, TOL, selects the trip level tolerance to be either 5- or 10-percent.

Each device has both a push-pull, active HIGH reset output and an open drain, active LOW reset output.

A debounced manual reset input activates the reset outputs for a minimum period of 250ms.

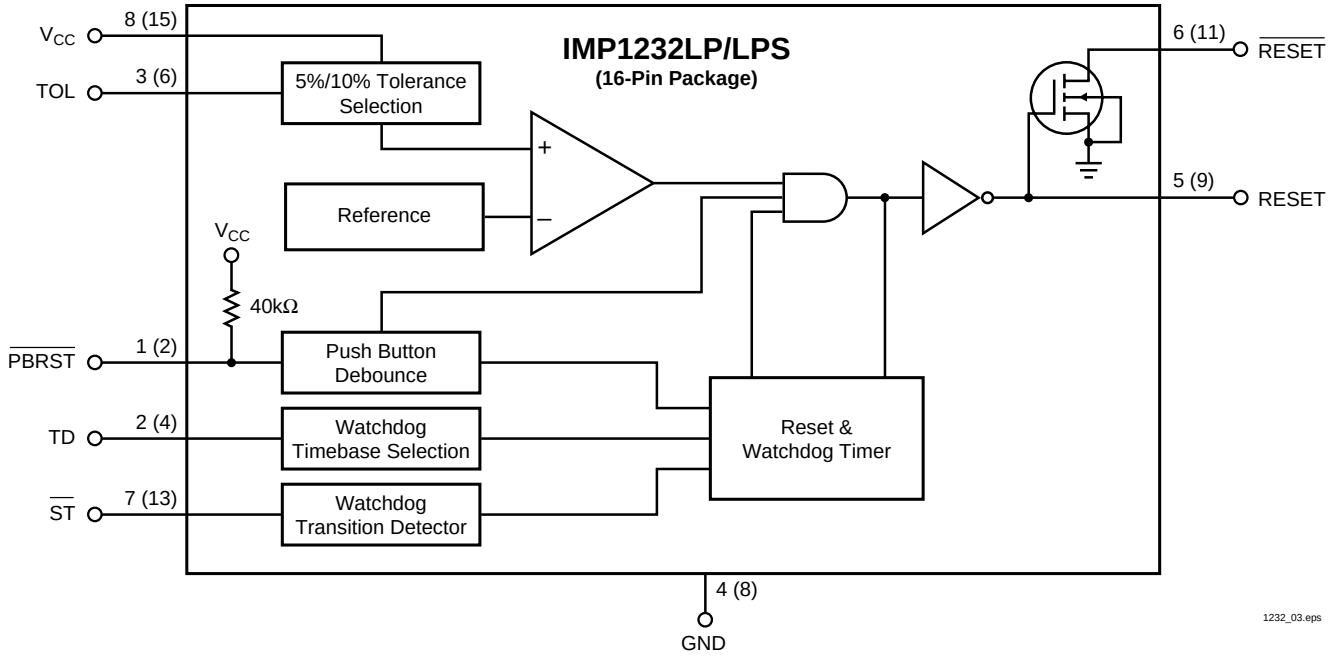
Also included is a watchdog timer to stop and restart a microprocessor that is "hung-up". Three watchdog time-out periods are selectable: 150ms, 610ms and 1,200ms. If the $\overline{\text{ST}}$ input is not strobed LOW before the time-out period expires, a reset is issued.

Devices are available in 8-pin DIP, 8/16-pin SO and compact 8-pin MicroSO packages.

## Key Features

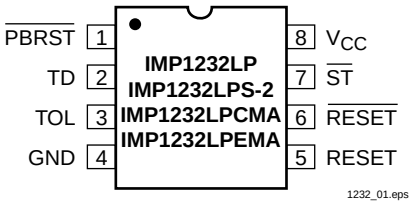
- Pin compatible with the Dallas Semiconductor DS1232LP/1232LPS
  — 40% lower supply current
- 5V supply monitor
- Selectable watchdog period
- Debounce manual push-button reset input
- Precision temperature-compensated voltage reference and comparator
- Power-up, power-down and brownout detection
- 250ms reset time
- Active LOW open-drain reset and active HIGH push-pull output
- Selectable trip point tolerance: 5% or 10%
- Low-cost, surface mount packages: 8/16-pin SO, 8-pin DIP and 8-pin MicroSO
- Wide operating temperature –40°C to +85°C (N/EPA suffixed devices)

## Block Diagram

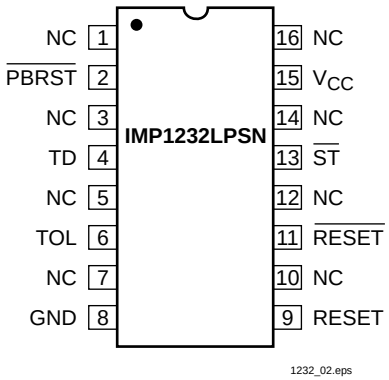


## Pin Configuration

### DIP/SO/MicroSO




### SO




## Pin Descriptions

| Pin Number 8-Pin Package | Pin Number 16-Pin Package | Name | Function |
|---|---|---|---|
| 1 | 2 | $\overline{\text{PBRST}}$ | Debounced manual pushbutton RESET input |
| 2 | 4 | TD | Watchdog time delay selection. ($t_{TD}$ = 150ms for TD = GND, $t_{TD}$ = 610ms for TD = Open, and $t_{TD}$ =1200ms for TD = $V_{CC}$) |
| 3 | 6 | TOL | Selects 5% (TOL connected to GND) or 10% (TOL connected to $V_{CC}$) trip point tolerance |
| 4 | 8 | GND | Ground |
| 5 | 9 | RESET | Active HIGH reset output. RESET is active:<br>1. If $V_{CC}$ falls below the reset voltage trip point.<br>2. If $\overline{\text{PBRST}}$ is LOW.<br>3. If $\overline{\text{ST}}$ is not strobed LOW before the timeout period set by TD expires.<br>4. During power-up. |
| 6 | 11 | $\overline{\text{RESET}}$ | Active LOW reset output. (See RESET) |
| 7 | 13 | $\overline{\text{ST}}$ | Strobe Input |
| 8 | 15 | $V_{CC}$ | 5V power |
| — | 1, 3, 5, 7, 10, 12, 14, 16 | NC | No internal connection |

## Ordering Information

| Part Number | Package | Operating Temperature Range | Maximum Supply Current (µA) | Voltage Monitoring Application |
|---|---|---|---|---|
| IMP1232LP | 8-DIP | 0°C to 70°C | 30 | 5V |
| IMP1232LPS | 16-SO | 0°C to 70°C | 30 | 5V |
| IMP1232LPS-2 | 8-SO | 0°C to 70°C | 30 | 5V |
| IMP1232LPCMA | 8-MicroSO | 0°C to 70°C | 30 | 5V |
| IMP1232LPEMA | 8-MicroSO | –40°C to 85°C | 30 | 5V |
| IMP1232LPN | 8-DIP | –40°C to 85°C | 30 | 5V |
| IMP1232LPSN-2 | 8-SO | –40°C to 85°C | 30 | 5V |
| IMP1232LPSN | 16-SO | –40°C to 85°C | 30 | 5V |

1232_t01.eps

## Absolute Maximum Ratings

Voltage on $V_{CC}$ . . . . . –0.5V to 7V
Voltage on $\overline{ST}$, TD . . . . . –0.5V to $V_{CC}$ + 0.5V
Voltage on $\overline{PBRST}$, RESET, $\overline{RESET}$ . . . . . –0.5V to $V_{CC}$ + 0.5V
Operating Temperature Range . . . . . –40°C to 85°C
(N / EMA version)
0°C to 70°C

Soldering Temperature . . . . . 260°C for 10 seconds
Storage Temperature . . . . . –55°C to 125°C

*Voltages measured with respect to ground.*
*These are stress ratings only and functional operation is not implied.*

## Electrical Characteristics

Unless otherwise stated, 4.5V ≤ $V_{CC}$ ≤ 5.5V and over the operating temperature range of 0°C to +70°C (–40°C to +85°C for N / EMA devices). All voltages are referenced to ground.

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Supply Voltage ($V_{CC}$) | $V_{CC}$ | | 4.5 | | 5.5 | V |
| $\overline{ST}$ and $\overline{PBRST}$ Input High Level | $V_{IH}$ | | 2 | | $V_{CC}$ + 0.3V | V |
| $\overline{ST}$ and $\overline{PBRST}$ Input Low Level | $V_{IL}$ | | –0.3 | | 0.8 | V |
| $V_{CC}$ Trip Point (TOL = GND) | $V_{CCTP}$ | | 4.50 | 4.62 | 4.74 | V |
| $V_{CC}$ Trip Point (TOL = $V_{CC}$) | $V_{CCTP}$ | | 4.25 | 4.37 | 4.49 | V |
| Watchdog Time-Out Period | $t_{TD}$ | TD = GND | 62.5 | 150 | 250 | ms |
| Watchdog Time-Out Period | $t_{TD}$ | TD = $V_{CC}$ | 500 | 1200 | 2000 | ms |
| Watchdog Time-Out Period | $t_{TD}$ | TD floating | 250 | 610 | 1000 | ms |
| Output Voltage | $V_{OH}$ | I = –500µA, Note 3 | $V_{CC}$ - 0.5V | $V_{CC}$ - 0.1V | | V |
| Output Current | $I_{OH}$ | Output = 2.4V , Note 2 | –8 | –10 | | mA |
| Output Current | $I_{OL}$ | Output = 0.4V, | 10 | | | mA |
| Input Leakage | $I_{IL}$ | Note 1 | –1.0 | | 1.0 | µA |
| RESET Low Level | $V_{OL}$ | | | | 0.4 | V |
| Internal Pull-Up Resistor | | Note 1 | | 40 | | kΩ |
| Operating Current (CMOS) | $I_{CC1}$ | | | | 30 | µA |
| Input Capacitance | $C_{IN}$ | | | | 5 | pF |
| Output Capacitance | $C_{OUT}$ | | | | 10 | pF |
| $\overline{PBRST}$ Manual Reset Minimum Low Time | $t_{PB}$ | $\overline{PBRST}$ = $V_{IL}$ | 20 | | | ms |
| Reset Active Time | $t_{RST}$ | | 250 | 610 | 1000 | ms |
| $\overline{ST}$ Pulse Width | $t_{ST}$ | Note 4 | 20 | | | ns |
| $V_{CC}$ Fail Detect to $\overline{RESET}$ or RESET | $t_{RPD}$ | | | 5 | 8 | µs |
| $V_{CC}$ Slew Rate | $t_F$ | 4.75V to 4.25V | 300 | | | µs |
| $\overline{PBRST}$ Stable LOW to RESET and $\overline{RESET}$ Active | $t_{PDLY}$ | | | | 20 | ms |
| $V_{CC}$ Detect to $\overline{RESET}$ or RESET Inactive | $t_{RPU}$ | $t_{RISE}$ = 5µs | 250 | 610 | 1000 | ms |
| $V_{CC}$ Slew Rate | $t_R$ | 4.25V to 4.75V | 0 | | | ns |

*Notes:* 1. *$\overline{PBRST}$ is internally pulled HIGH to $V_{CC}$ through a nominal 40kΩ resistor.*
2. *$\overline{RESET}$ is an open drain output.*
3. *RESET remains within 0.5V of $V_{CC}$ on power-down until $V_{CC}$ falls below 2V. $\overline{RESET}$ remains within 0.5V of ground on power-down until $V_{CC}$ falls below 2.0V.*
4. *Must not exceed the minimum watchdog time-out period ($t_{TD}$). The watchdog circuit cannot be disabled. To avoid a reset, $\overline{ST}$ must be strobed.*

## Application Information

### Supply Voltage Monitor

**Reset Signal Polarity and Output Stage Structure**

$\overline{\text{RESET}}$ is an active LOW signal. It is developed with an open drain driver. If a pullup resistor is required, typical values are 10kΩ to 50kΩ.

RESET is an active High signal developed by a CMOS push-pull output stage and is the logical opposite to $\overline{\text{RESET}}$.

**Trip Point Tolerance Selection**

With TOL connected to $V_{CC}$, RESET and $\overline{\text{RESET}}$ become active whenever $V_{CC}$ falls below 4.5V. RESET and $\overline{\text{RESET}}$ become active when $V_{CC}$ falls below 4.75V if TOL is connected to ground.

After $V_{CC}$ has risen above the trip point set by TOL, RESET and $\overline{\text{RESET}}$ remain active for a minimum time period of 250ms.

On power-down, once $V_{CC}$ falls below the reset threshold $\overline{\text{RESET}}$ stays LOW and is guaranteed to be 0.4V or less until $V_{CC}$ drops below 1.2V. The active HIGH reset signal is valid down to a $V_{CC}$ level of 1.2V also.

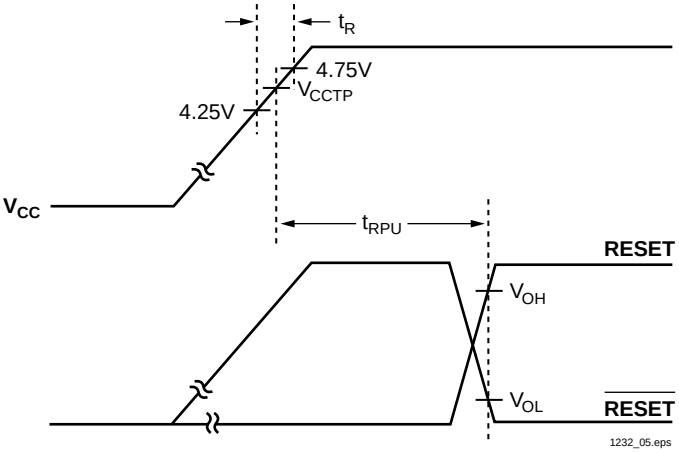



*Figure 1. Timing Diagram: Power Up*

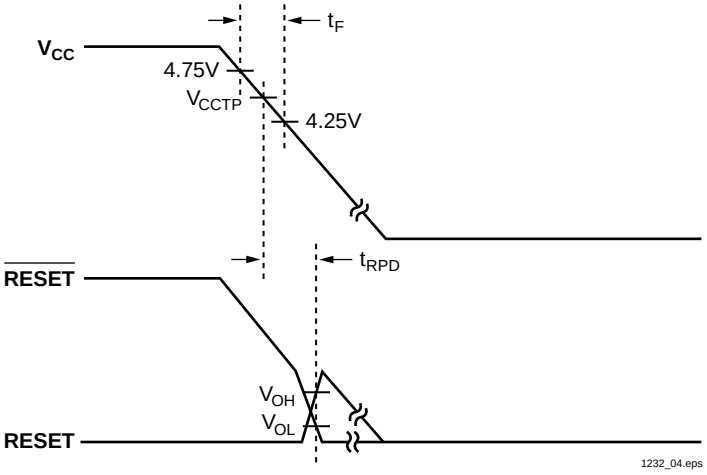



*Figure 2. Timing Diagram: Power Down*

| Tolerance Select | Tolerance | TRIP Point Voltage (V) | | |
|---|---|---|---|---|
| | | Min | Nominal | Max |
| TOL = $V_{CC}$ | 10% | 4.25 | 4.37 | 4.49 |
| TOL = GND | 5% | 4.5 | 4.62 | 4.74 |

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### Manual Reset Operation

Push-button switch input, $\overline{\text{PBRST}}$, allows the user to override the internal trip point detection circuits and issue reset signals. The pushbutton input is debounced and is normally pulled HIGH through an internal 40kΩ resistor.

When $\overline{\text{PBRST}}$ is held LOW for the minimum time $t_{PB}$ , both resets become active and remain active for approximately a minimum time period of 250ms after $\overline{\text{PBRST}}$ returns HIGH.

The debounced input is guaranteed to recognize pulses greater than 20ms. No external pull-up resistor is required, since $\overline{\text{PBRST}}$ is pulled HIGH by an internal 40kΩ resistor.

The $\overline{\text{PBRST}}$ can be driven from a TTL or CMOS logic line or shorted to ground with a mechanical switch.

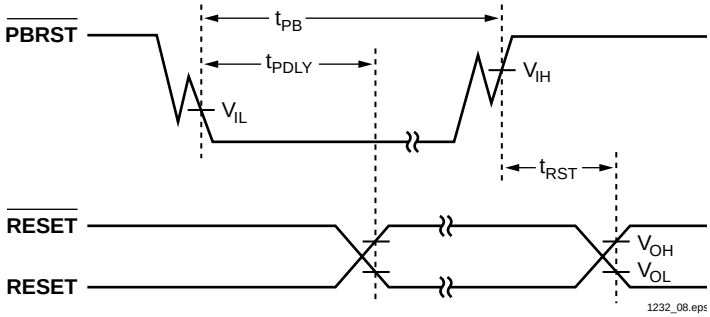



*Figure 3. Timing Diagram: Pushbutton Reset*

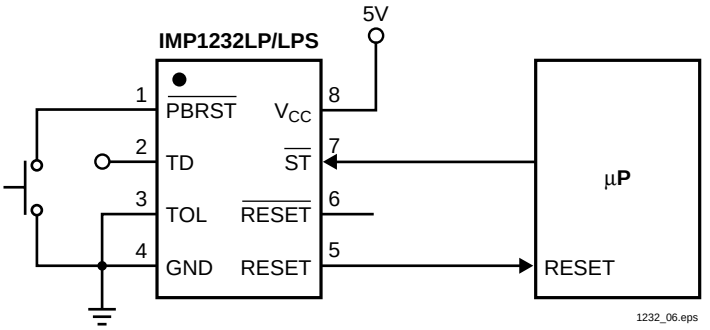
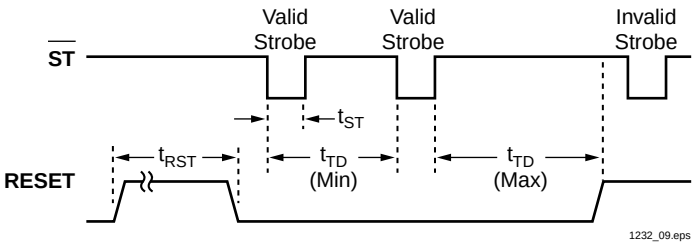



*Figure 4. Application Circuit: Pushbutton Reset*

## Watchdog Timer and $\overline{ST}$ Input

A watchdog timer stops and restarts a microprocessor that is "hung-up". Through the time delay input, TD, three watchdog time-out periods are selectable: 150ms, 610ms and 1,200ms. If the strobe input, $\overline{ST}$, is not strobed LOW prior to timeout, reset signals become active. On power-up or after the supply voltage returns to an in-tolerance condition, the reset signal remains active for 250ms minimum, allowing the power supply and system micro-processor to stabilize.

$\overline{ST}$ Pulses as short as 20ns can be detected.




*Note: $\overline{ST}$ is ignored whenever a reset is active.*

***Figure 5. Timing Diagram: Strobe Input***

A HIGH-to-LOW $\overline{ST}$ signal transition must be regularly issued no later than the minimum time-out period defined by the state of the TD signal. This guarantees the watchdog timer does not time-out.

Timeouts periods of approximately 150ms, 610ms or 1,200ms are selected through the TD pin.

| TD Voltage Level | Watchdog Time-Out Period (ms) | | |
|---|---|---|---|
| | Min | Nominal | Max |
| GND | 62.5 | 150 | 250 |
| Floating | 250 | 610 | 1000 |
| $V_{CC}$ | 500 | 1200 | 2000 |

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The watchdog timer cannot be disabled. It must be strobed with a high-to-low transition to avoid a watchdog timeout.

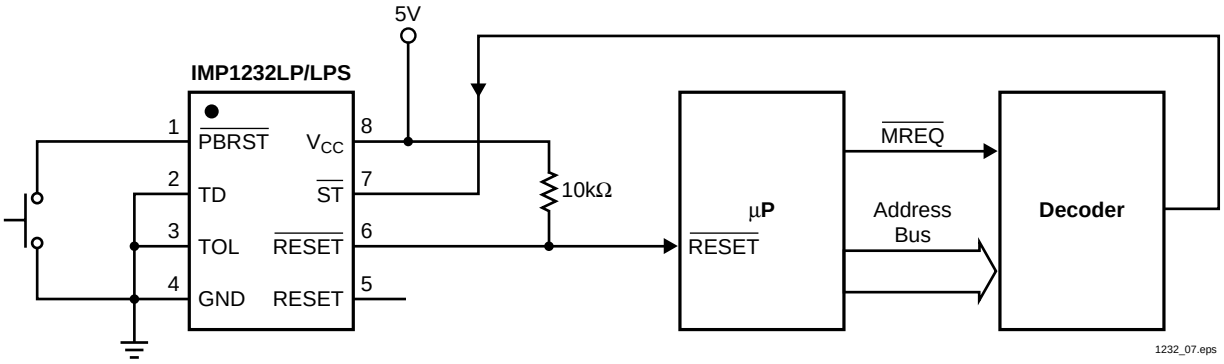
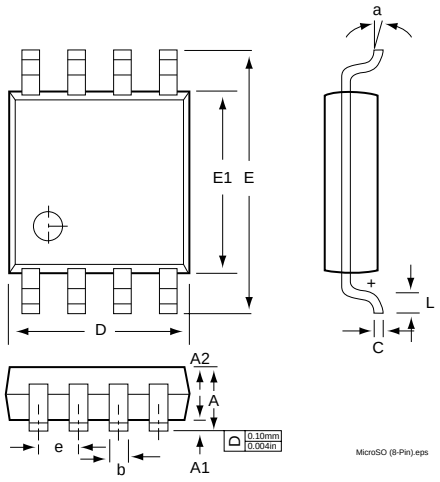


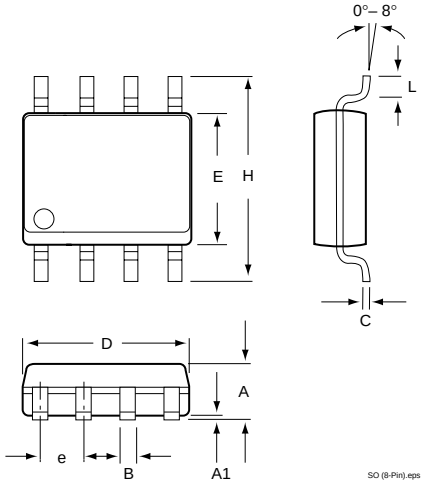

***Figure 6. Application Circuit: Watchdog Timer***

## Package Dimensions

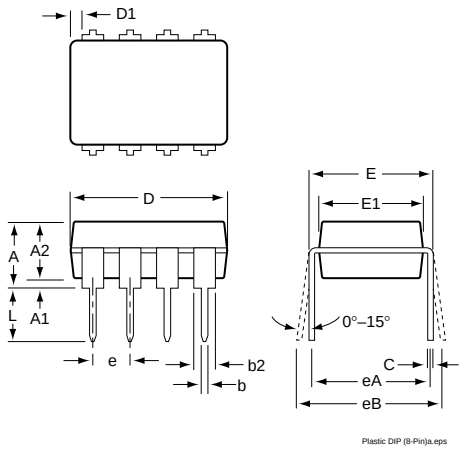
### MicroSO (8-Pin)




### SO (8-Pin)




### Plastic DIP (8-Pin)



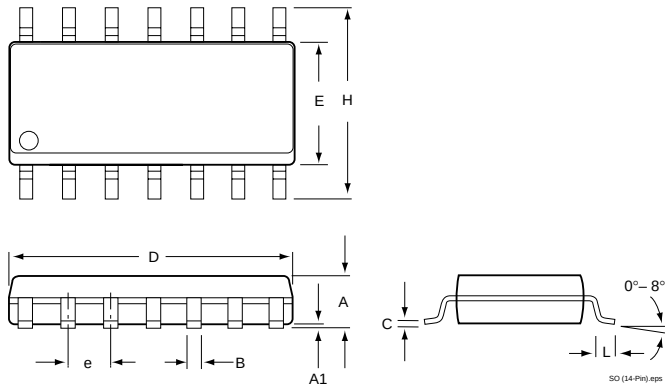

| | Inches | | Millimeters | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| **MicroSO (8-Pin)*** | | | | |
| A | ——— | 0.0433 | —— | 1.10 |
| A1 | 0.0020 | 0.0059 | 0.050 | 0.15 |
| A2 | 0.0295 | 0.0374 | 0.75 | 0.95 |
| b | 0.0098 | 0.0157 | 0.25 | 0.40 |
| C | 0.0051 | 0.0091 | 0.13 | 0.23 |
| D | 0.1142 | 0.1220 | 2.90 | 3.10 |
| e | 0.0256 BSC | | 0.65 BSC | |
| E | 0.193 BSC | | 4.90 BSC | |
| E1 | 0.1142 | 0.1220 | 2.90 | 3.10 |
| L | 0.0157 | 0.0276 | 0.40 | 0.70 |
| a | 0° | 6° | 0° | 6° |
| **SO (8-Pin)**** | | | | |
| A | 0.053 | 0.069 | 1.35 | 1.75 |
| A1 | 0.004 | 0.010 | 0.10 | 0.25 |
| B | 0.013 | 0.020 | 0.33 | 0.51 |
| C | 0.007 | 0.010 | 0.19 | 0.25 |
| e | 0.050 | | 1.27 | |
| E | 0.150 | 0.157 | 3.80 | 4.00 |
| H | 0.228 | 0.244 | 5.80 | 6.20 |
| L | 0.016 | 0.050 | 0.40 | 1.27 |
| D | 0.189 | 0.197 | 4.80 | 2.00 |
| **Plastic DIP (8-Pin)***** | | | | |
| A | ——— | 0.210 | —— | 5.33 |
| A1 | 0.015 | ——— | 0.38 | ——— |
| A2 | 0.115 | 0.195 | 2.92 | 4.95 |
| b | 0.014 | 0.022 | 0.36 | 0.56 |
| b2 | 0.045 | 0.070 | 1.14 | 1.78 |
| b3 | 0.030 | 0.045 | 0.80 | 1.14 |
| D | 0.355 | 0.400 | 9.02 | 10.16 |
| D1 | 0.005 | ——— | 0.13 | ——— |
| E | 0.300 | 0.325 | 7.62 | 8.26 |
| E1 | 0.240 | 0.280 | 6.10 | 7.11 |
| e | 0.100 | ——— | 2.54 | |
| eA | 0.300 | ——— | 7.62 | |
| eB | ——— | 0.430 | ——— | 10.92 |
| eC | ——— | 0.060 | | |
| L | 0.115 | 0.150 | 2.92 | 3.81 |

1232_t04.at3

** JEDEC Drawing MO-187AA*
*** JEDEC Drawing MS-112AA*
**** JEDEC Drawing MS-001BA*

## Package Dimensions

### SO (16-Pin)




| | Inches | | Millimeters | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| SO (16-Pin)* | | | | |
| A | 0.926 | 0.1043 | 2.35 | 2.65 |
| A1 | 0.0040 | 0.0118 | 0.10 | 0.30 |
| B | 0.013 | 0.020 | 0.33 | 0.51 |
| C | 0.0091 | 0.0125 | 0.23 | 0.32 |
| D | 0.3977 | 0.4133 | 10.10 | 10.50 |
| E | 0.2914 | 0.2662 | 7.40 | 7.60 |
| e | 0.050 BSC | | 1.27 BSC | |
| H | 0.394 | 0.419 | 10.00 | 10.65 |
| L | 0.016 | 0.050 | 0.40 | 1.27 |

** JEDEC Drawing MS-013AA*

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