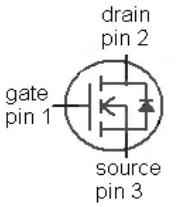
OptiMOS®2 Power-Transistor

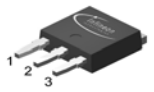
Product Summary

V_{DS}	25	V
$R_{DS(on),max}$ (SMD Version)	4.2	mΩ
I_D	90	A

Features

- Ideal for high-frequency dc/dc converters
- Qualified according to JEDEC[1] for target applications
- N-channel, logic level
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- Superior thermal resistance
- 175 °C operating temperature
- Pb-free lead plating; RoHS compliant



Type	IPDH4N03LA G	IPSH4N03LA G
		
Package	P-TO252-3-11	P-TO251-3-11
Ordering Code	Q67042-S4250	Q67042-S4254
Marking	H4N03LA	H4N03LA

Maximum ratings, at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	T_C=25 °C[2]	90	A
		T_C=100 °C	77	
Pulsed drain current	$I_{D,pulse}$	T_C=25 °C[3]	360	
Avalanche energy, single pulse	E_{AS}	I_D=90 A, R_{GS}=25 Ω	150	mJ
Reverse diode dv/dt	dv/dt	I_D=90 A, V_{DS}=20 V, di/dt=200 A/µs, $T_{j,max}$=175 °C	6	kV/µs
Gate source voltage[4]	V_{GS}		±20	V
Power dissipation	P_{tot}	T_C=25 °C	94	W
Operating and storage temperature	T_j, T_{stg}		-55 ... 175	°C
IEC climatic category; DIN IEC 68-1			55/175/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal characteristics						
Thermal resistance, junction - case	R_{thJC}		-	-	1.6	K/W
SMD version, device on PCB	R_{thJA}	minimal footprint	-	-	75	
		6 cm^2 cooling area[5]	-	-	50	
Electrical characteristics, at T_j=25 °C, unless otherwise specified						
Static characteristics						
Drain-source breakdown voltage	$V_{\mathrm{(BR)DSS}}$	V_{GS}=0 V, I_{D}=1 mA	25	-	-	V
Gate threshold voltage	$V_{\mathrm{GS(th)}}$	V_{DS}=V_{GS}, I_{D}=40 µA	1.2	1.6	2	
Zero gate voltage drain current	I_{DSS}	V_{DS}=25 V, V_{GS}=0 V, T_j=25 °C	-	0.1	1	µA
		V_{DS}=25 V, V_{GS}=0 V, T_j=125 °C	-	10	100	
Gate-source leakage current	I_{GSS}	V_{GS}=20 V, V_{DS}=0 V	-	10	100	nA
Drain-source on-state resistance	$R_{\mathrm{DS(on)}}$	V_{GS}=4.5 V, I_{D}=50 A	-	6.1	7.6	mΩ
		V_{GS}=4.5 V, I_{D}=50 A, SMD version	-	5.9	7.4	
		V_{GS}=10 V, I_{D}=60 A	-	3.7	4.4	
		V_{GS}=10 V, I_{D}=60 A, SMD version	-	3.5	4.2	
Gate resistance	R_{G}		-	1.3	-	Ω
Transconductance	g_{fs}	$\|V_{\mathrm{DS}}\|>2\|I_{\mathrm{D}}\|R_{\mathrm{DS(on)max}}$, I_{D}=60 A	45	90	-	S

[1] J-STD20 and JESD22

[1] Current is limited by bondwire; with an R_{thJC}=1.6 K/W the chip is able to carry 109 A.

[3] See figure 3

[4] $T_{\mathrm{j,max}}$=150 °C and duty cycle D <0.25 for V_{GS}<-5 V

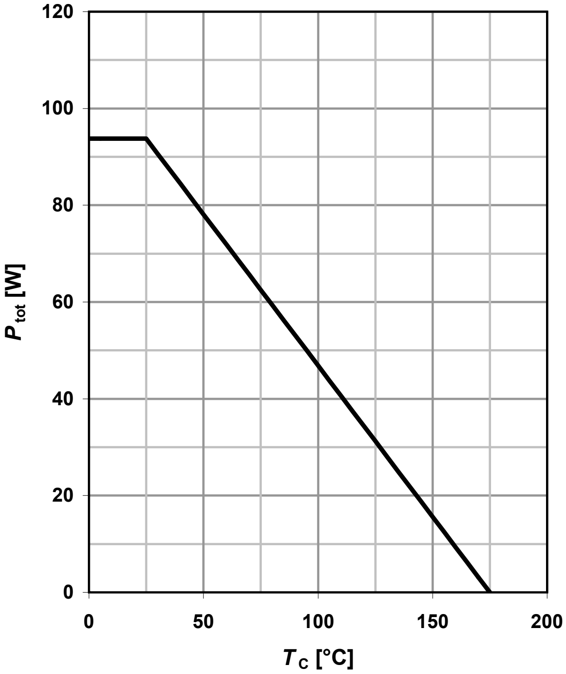
[5] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Dynamic characteristics						
Input capacitance	C_{iss}	V_{GS}=0 V, V_{DS}=15 V, f=1 MHz	-	2400	3200	pF
Output capacitance	C_{oss}		-	920	1200	
Reverse transfer capacitance	C_{rss}		-	110	160	
Turn-on delay time	$t_{\text{d(on)}}$	V_{DD}=15 V, V_{GS}=10 V, I_{D}=25 A, R_{G}=2.7 Ω	-	9	14	ns
Rise time	t_{r}		-	7	11	
Turn-off delay time	$t_{\text{d(off)}}$		-	29	44	
Fall time	t_{f}		-	4.6	7	
Gate Charge Characteristics[6]						
Gate to source charge	Q_{gs}	V_{DD}=15 V, I_{D}=45 A, V_{GS}=0 to 5 V	-	8	11	nC
Gate charge at threshold	$Q_{\text{g(th)}}$		-	3.9	5.1	
Gate to drain charge	Q_{gd}		-	5.6	8	
Switching charge	Q_{sw}		-	10	14	
Gate charge total	Q_{g}		-	19	26	
Gate plateau voltage	V_{plateau}		-	3.4	-	V
Gate charge total, sync. FET	$Q_{\text{g(sync)}}$	V_{DS}=0.1 V, V_{GS}=0 to 5 V	-	17	23	nC
Output charge	Q_{oss}	V_{DD}=15 V, V_{GS}=0 V	-	20	27	
Reverse Diode						
Diode continous forward current	I_{S}	T_{C}=25 °C	-	-	78	A
Diode pulse current	$I_{\text{S,pulse}}$		-	-	360	
Diode forward voltage	V_{SD}	V_{GS}=0 V, I_{F}=78 A, T_{j}=25 °C	-	0.93	1.2	V
Reverse recovery charge	Q_{rr}	V_{R}=15 V, I_{F}=I_{S}, di_{F}/dt=400 A/µs	-	-	15	nC

[6] See figure 16 for gate charge parameter definition

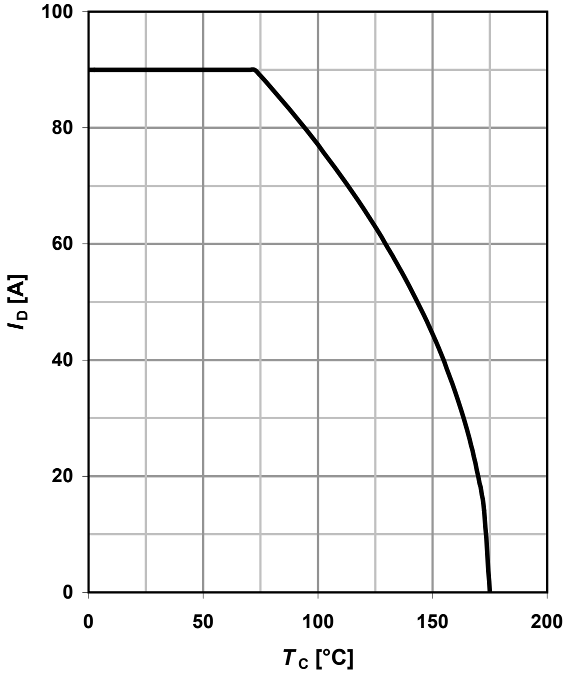
1 Power dissipation

P_{tot}=f(T_C)



2 Drain current

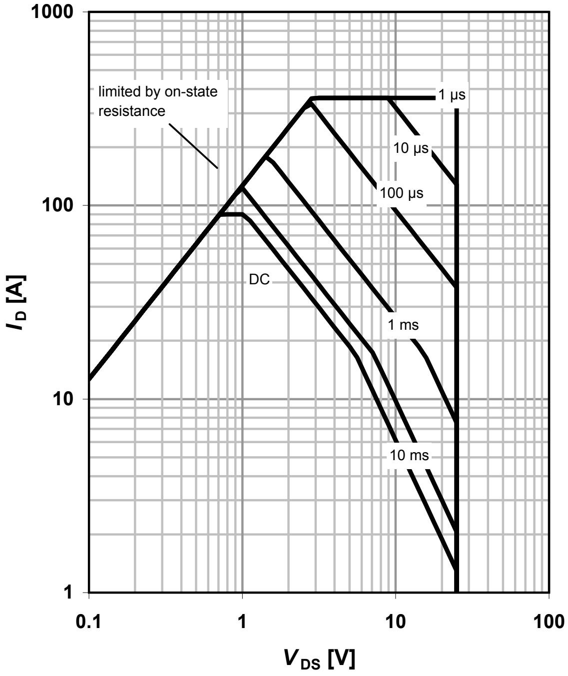
I_D=f(T_C); V_{GS}≥10 V



3 Safe operating area

I_D=f(V_{DS}); T_C=25 °C; D=0

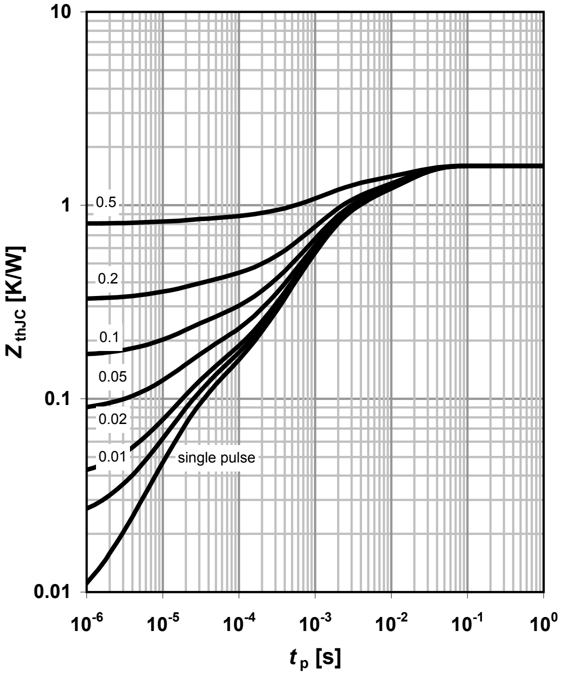
parameter: t_p



4 Max. transient thermal impedance

Z_{thJC}=f(t_p)

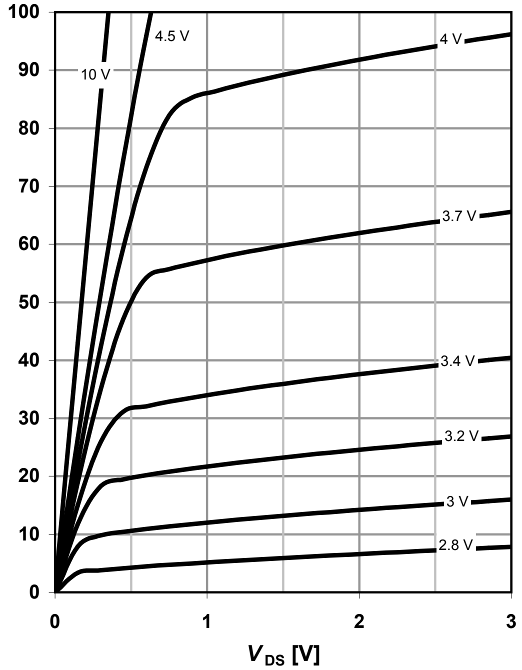
parameter: D=t_p/T



5 Typ. output characteristics

I_D=f(V_{DS}); T_j=25 °C

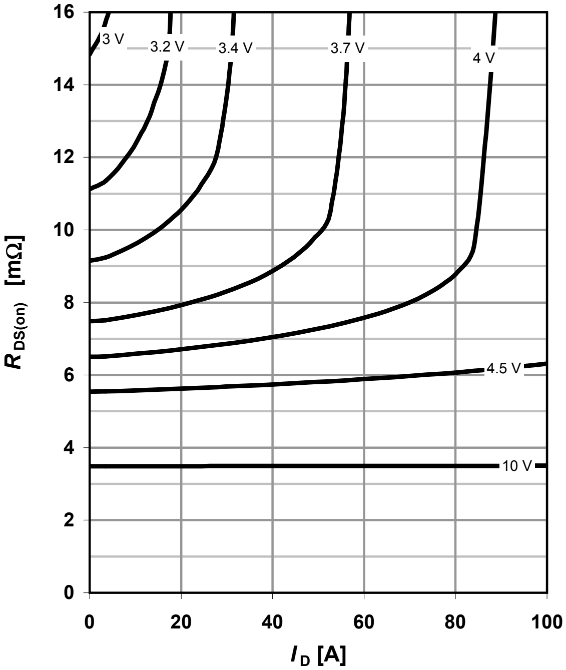
parameter: V_{GS}



6 Typ. drain-source on resistance

$R_{DS(on)}$=f(I_D); T_j=25 °C

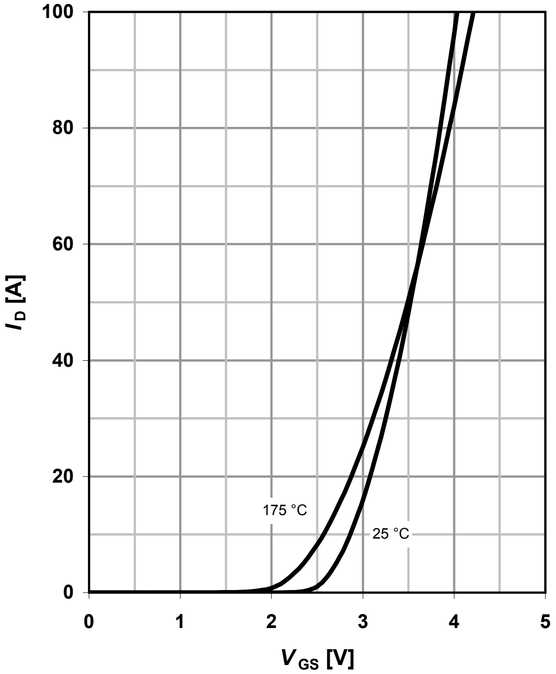
parameter: V_{GS}



7 Typ. transfer characteristics

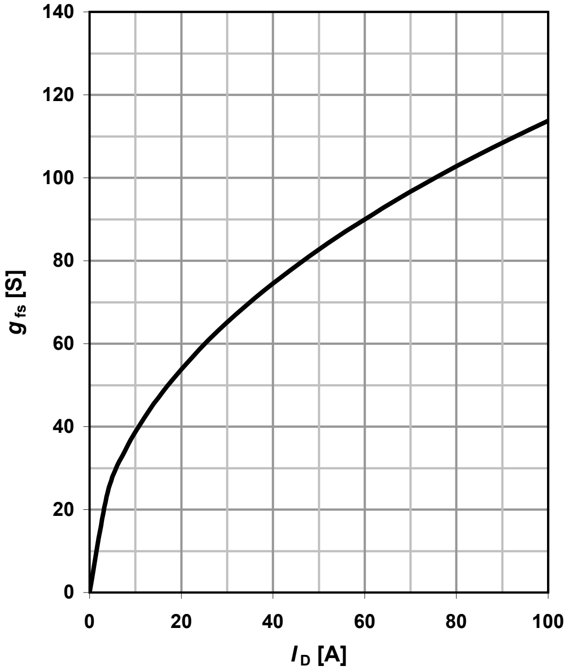
I_D=f(V_{GS}); $|V_{DS}|>2|I_D|R_{DS(on)max}$

parameter: T_j



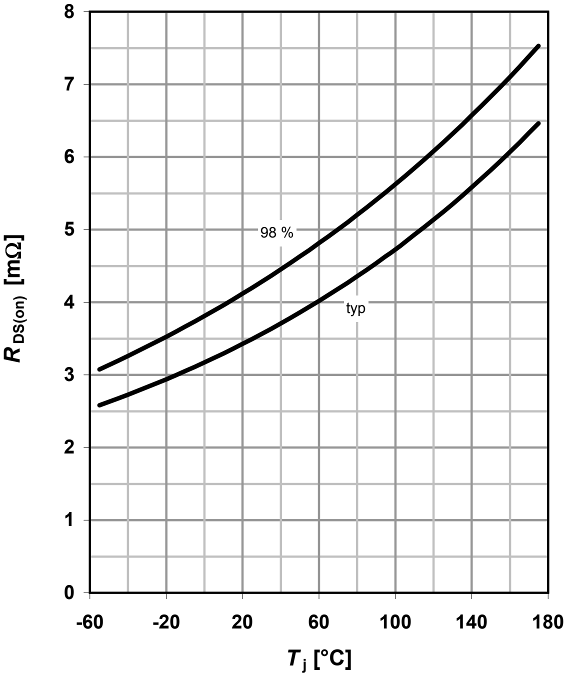
8 Typ. forward transconductance

g_{fs}=f(I_D); T_j=25 °C



9 Drain-source on-state resistance

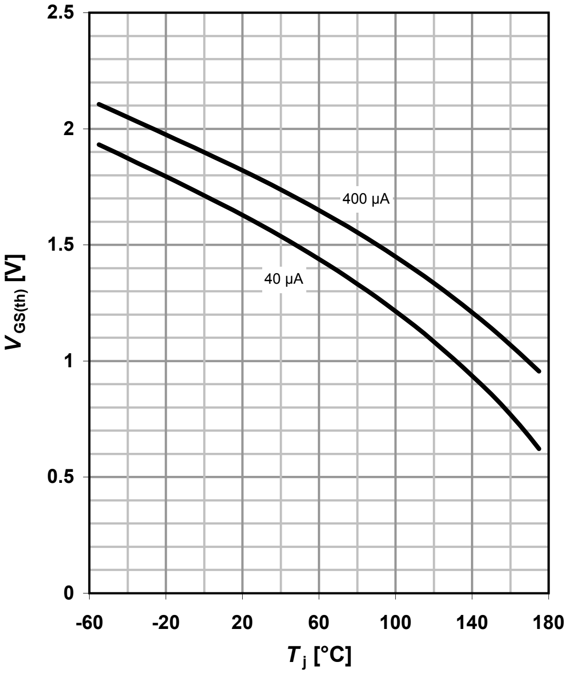
$R_{DS(on)}$=f(T_j); I_D=60 A; V_{GS}=10 V



10 Typ. gate threshold voltage

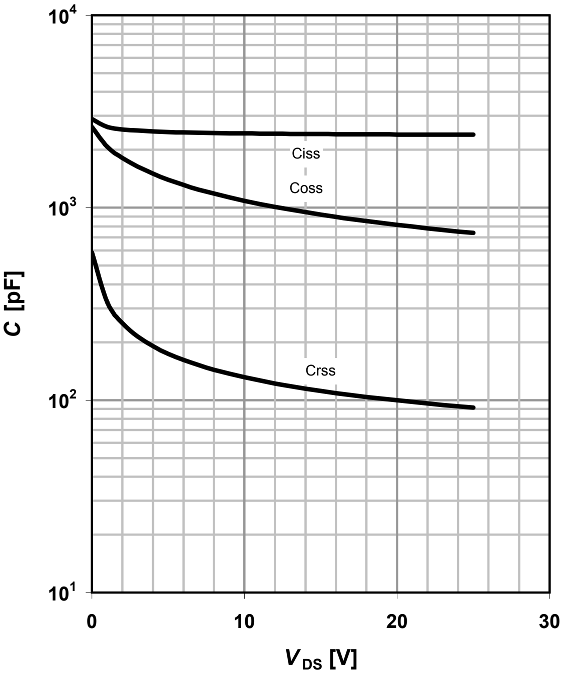
$V_{GS(th)}$=f(T_j); V_{GS}=V_{DS}

parameter: I_D



11 Typ. capacitances

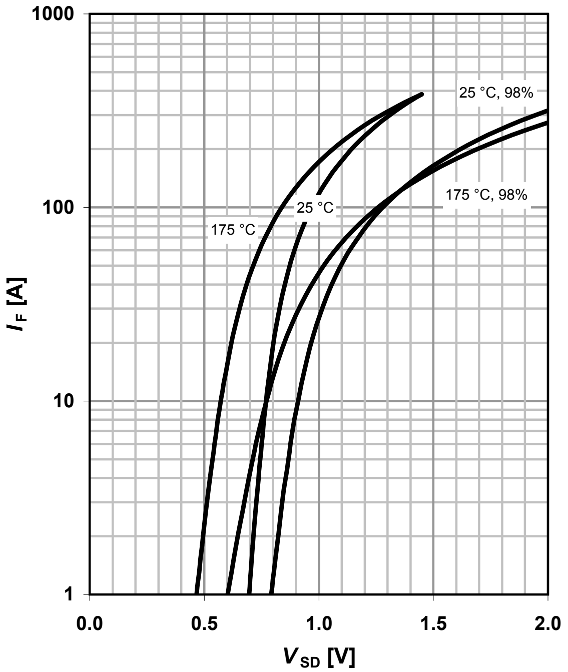
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz



12 Forward characteristics of reverse diode

I_F=f(V_{SD})

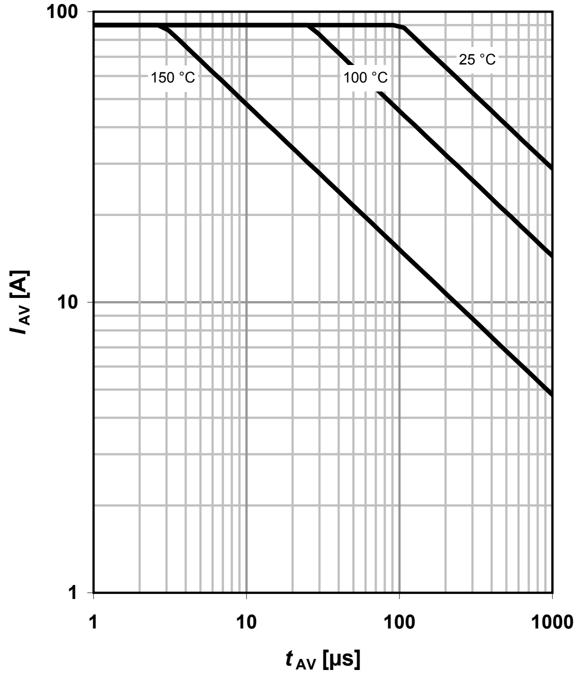
parameter: T_j



13 Avalanche characteristics

I_{AS}=f(t_{AV}); R_{GS}=25 Ω

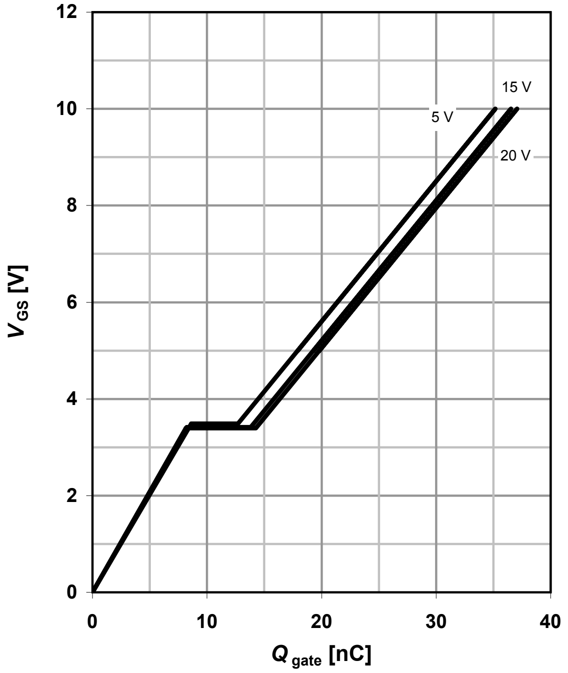
parameter: $T_{j(start)}$



14 Typ. gate charge

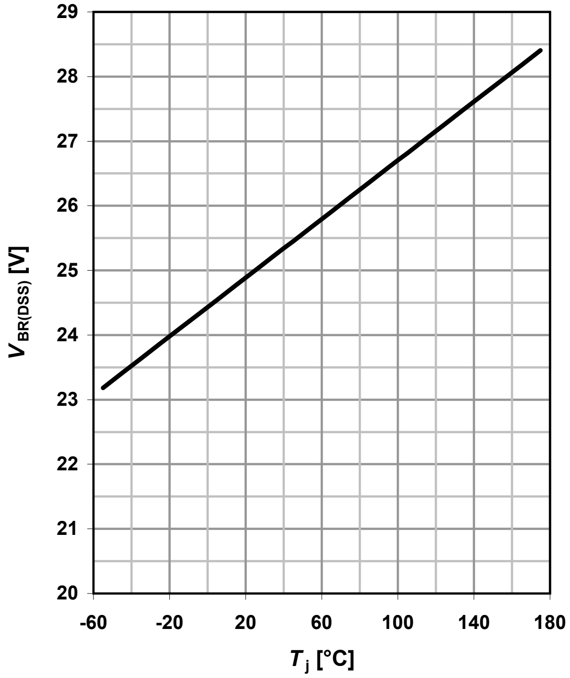
V_{GS}=f(Q_{gate}); I_D=45 A pulsed

parameter: V_{DD}

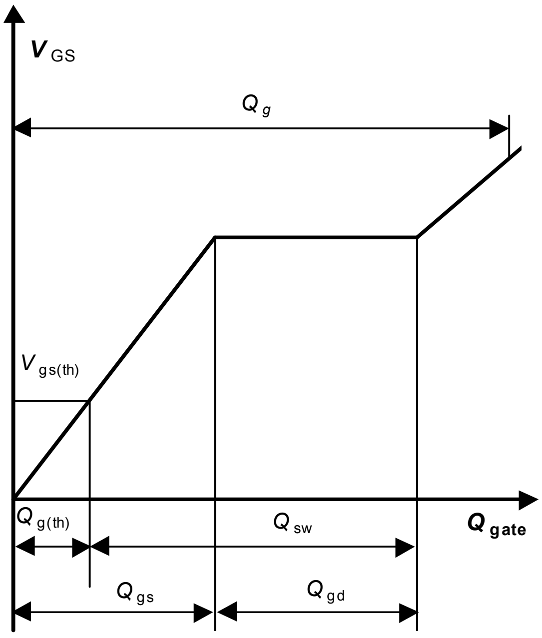


15 Drain-source breakdown voltage

$V_{BR(DSS)}$=f(T_j); I_D=1 mA

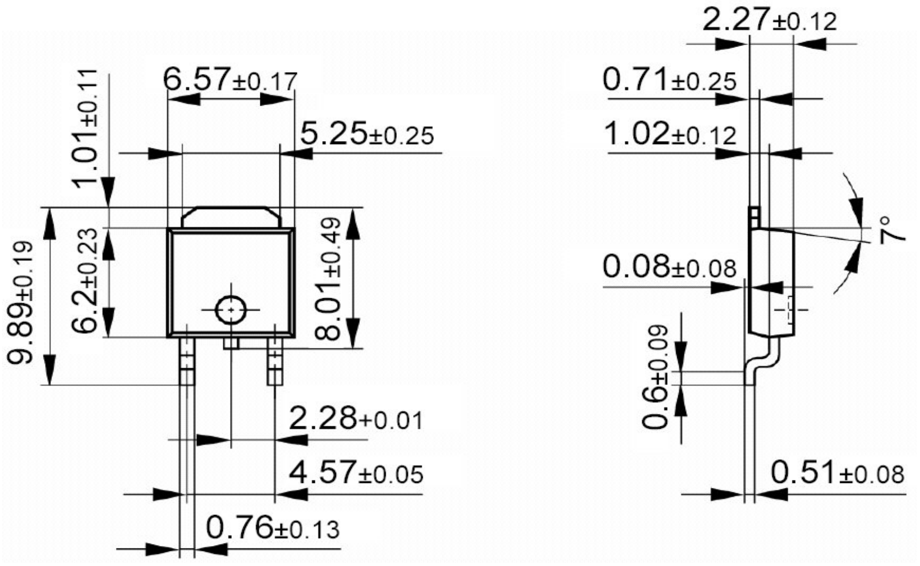


16 Gate charge waveforms

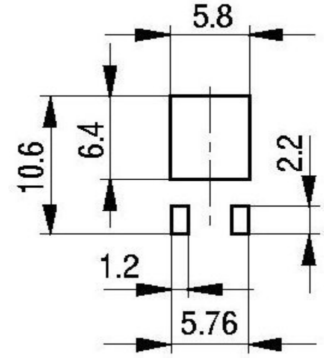


Package Outline

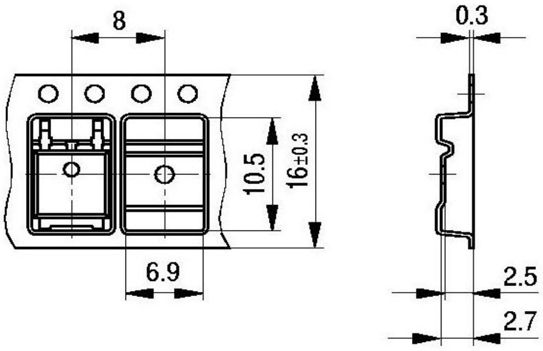
P-TO252-3-11: Outline



Footprint:



Packaging:



Dimensions in mm