International
IOR Rectifier

ADVANCE DATA

Data Sheet No.PD60217

IR2011(S)

HIGH AND LOW SIDE DRIVER

Features

- Floating channel designed for bootstrap operation
  Fully operational up to +200V
  Tolerant to negative transient voltage, dV/dt immune
- Gate drive supply range from 10V to 20V
- Independent low and high side channels
- Input logicHIN/LIN active high
- Undervoltage lockout for both channels
- 3.3V and 5V input logic compatible
- CMOS Schmitt-triggered inputs with pull-down
- Matched propagation delay for both channels

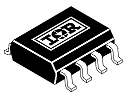
Product Summary

V_{OFFSET}	200V max.
I_O+/-	1.0A /1.0A typ.
V_{OUT}	10 - 20V
$t_{on/off}$	80 & 60 ns typ.
Delay Matching	20 ns max.

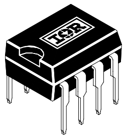
Applications

- Audio Class D amplifiers
- High power DC-DC SMPS converters
- Other high frequency applications

Packages



8-Lead SOIC

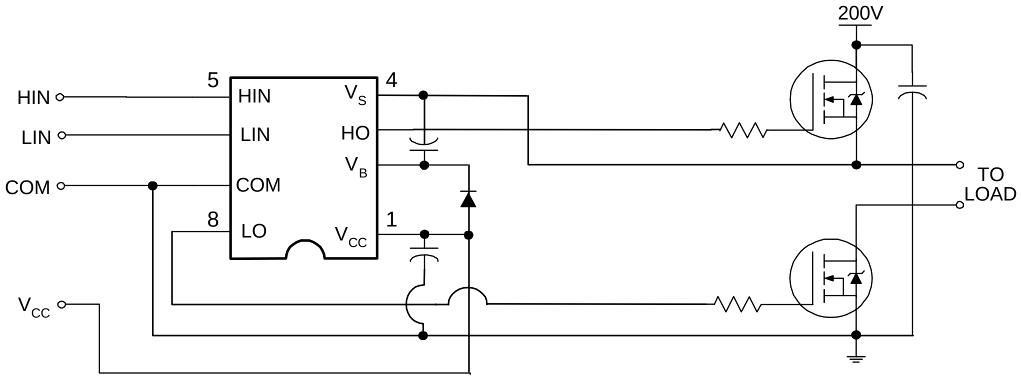


8-Lead PDIP

Description

The IR2011 is a high power, high speed power MOSFET driver with independent high and low side referenced output channels, ideal for Audio Class D and DC-DC converter applications. Logic inputs are compatible with standard CMOS or LSTTL output, down to 3.0V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channel can be used to drive an N-channel power MOSFET in the high side configuration which operates up to 200 volts. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction.

Typical Connection



(Refer to Lead Assignments for correct configuration). This/These diagram(s) show electrical connections only. Please refer to our Application Notes and DesignTips for proper circuit board layout.

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition		Min.	Max.	Units
V_B	High side floating supply voltage		-0.3	250	V
V_S	High side floating supply offset voltage		V_B - 25	V_B + 0.3	
V_{HO}	High side floating output voltage		V_S - 0.3	V_B + 0.3	
V_{CC}	Low side fixed supply voltage		-0.3	25	
V_{LO}	Low side output voltage		-0.3	V_{CC} +0.3	
V_{IN}	Logic input voltage (HIN & LIN)		COM -0.3	V_{CC} +0.3	
dV_S/dt	Allowable offset supply voltage transient (figure 2)		—	50	V/ns
P_D	Package power dissipation @ $T_A \leq +25°C$	(8-lead DIP)	—	1.0	W
		(8-lead SOIC)	—	0.625	
R_{THJA}	Thermal resistance, junction to ambient	(8-lead DIP)	—	125	°C/W
		(8-lead SOIC)	—	200	
T_J	Junction temperature		—	150	°C
T_S	Storage temperature		-55	150	
T_L	Lead temperature (soldering, 10 seconds)		—	300	

Recommended Operating Conditions

For proper operation the device should be used within the recommended conditions. The V_S and COM offset ratings are tested with all supplies biased at 15V differential.

Symbol	Definition	Min.	Max.	Units
V_B	High side floating supply absolute voltage	V_S + 10	V_S + 20	V
V_S	High side floating supply offset voltage	Note 1	200	
V_{HO}	High side floating output voltage	V_S	V_B	
V_{CC}	Low side fixed supply voltage	10	20	
V_{LO}	Low side output voltage	0	VCC	
V_{IN}	Logic input voltage (HIN & LIN)	COM	5.5	
T_A	Ambient temperature	-40	125	

Note 1: Logic operational for V_S of -4 to +200V. Logic state held for V_S of -4V to $-V_{BS}$.

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V, C_L = 1000 pF, T_A = 25°C unless otherwise specified. Figure 1 shows the timing definitions.

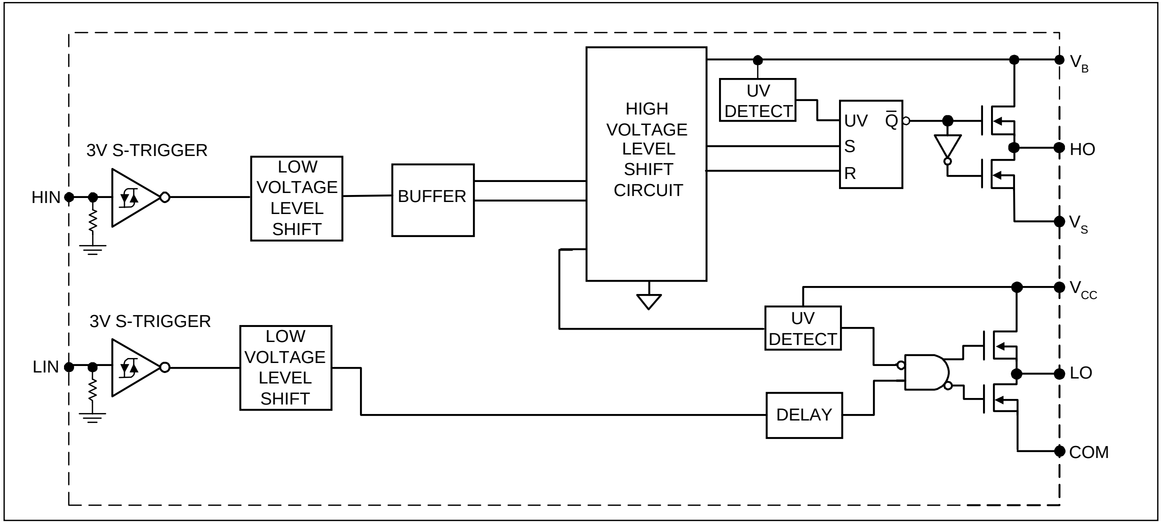
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-on propagation delay	—	80	—	ns	V_S = 0V
t_{off}	Turn-off propagation delay	—	60	—		V_S = 200V
t_r	Turn-on rise time	—	15	25		
t_f	Turn-off fall time	—	10	20		
DM1	Turn-on delay matching $\mid t_{on}$ (H) - t_{on} (L) $\mid$	10	20	30		
DM2	Turn-off delay matching $\mid t_{off}$ (H) - t_{off} (L) $\mid$	10	20	30		

Static Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V, and T_A = 25°C unless otherwise specified. The V_{IN}, V_{TH} and I_{IN} parameters are referenced to COM and are applicable to all logic input leads: HIN and LIN. The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic "1" input voltage	2.2	—	—	V	V_{CC} = 10V - 20V
V_{IL}	Logic "0" input voltage	—	—	1.2		
V_{OH}	High level output voltage, V_{BIAS} - V_O	—	—	1.0		I_O = 0A
V_{OL}	Low level output voltage, V_O	—	—	0.1		I_O = 0A
I_{LK}	Offset supply leakage current	—	—	50	µA	V_B=V_S = 200V
I_{QBS}	Quiescent V_{BS} supply current	—	70	210		V_{IN} = 0V or 3.3V
I_{QCC}	Quiescent V_{CC} supply current	—	100	230		V_{IN} = 0V or 3.3V
I_{IN+}	Logic "1" input bias current	—	20	40		V_{IN} = 3.3V
I_{IN-}	Logic "0" input bias current	—	—	1.0		V_{IN} = 0V
V_{BSUV+}	V_{BS} supply undervoltage positive going threshold	7.5	8.6	9.7	V	
V_{BSUV-}	V_{BS} supply undervoltage negative going threshold	7.0	8.2	9.4		
V_{CCUV+}	V_{CC} supply undervoltage positive going threshold	7.5	8.6	9.7		
V_{CCUV-}	V_{CC} supply undervoltage negative going threshold	7.0	8.2	9.4		
I_{O+}	Output high short circuit pulsed current	—	1.0	—	A	V_O = 0V, PW ≤ 10 µs
I_{O-}	Output low short circuit pulsed current	—	1.0	—		V_O = 15V, PW ≤ 10 µs

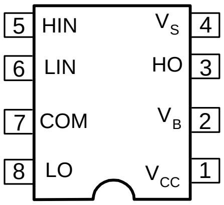
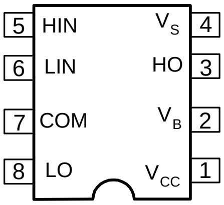
Functional Block Diagram



Lead Definitions

Symbol	Description
HIN	Logic input for high side gate driver output (HO), in phase
LIN	Logic input for low side gate driver output (LO), in phase
V_B	High side floating supply
HO	High side gate drive output
V_S	High side floating supply return
V_{CC}	Low side supply
LO	Low side gate drive output
COM	Low side return

Lead Assignments

 8-Lead PDIP	 8-Lead SOIC
IR2011	**IR2011S**
Part Number	

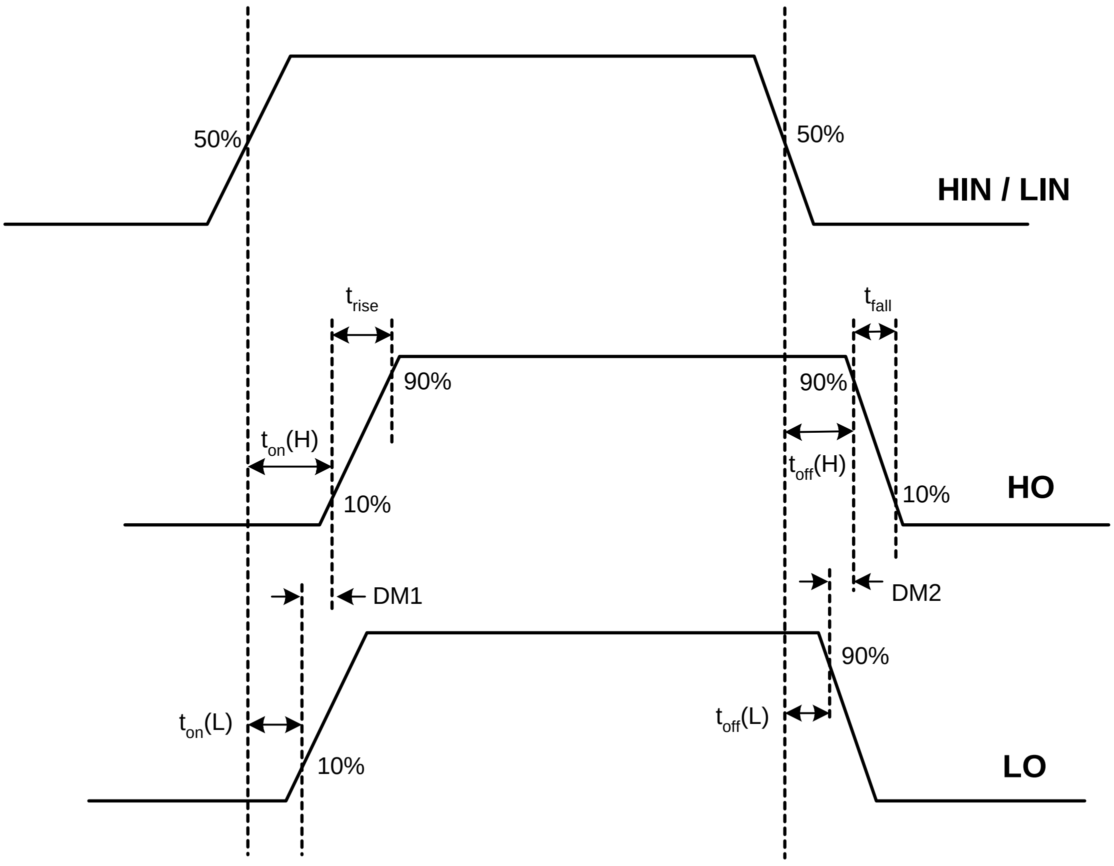
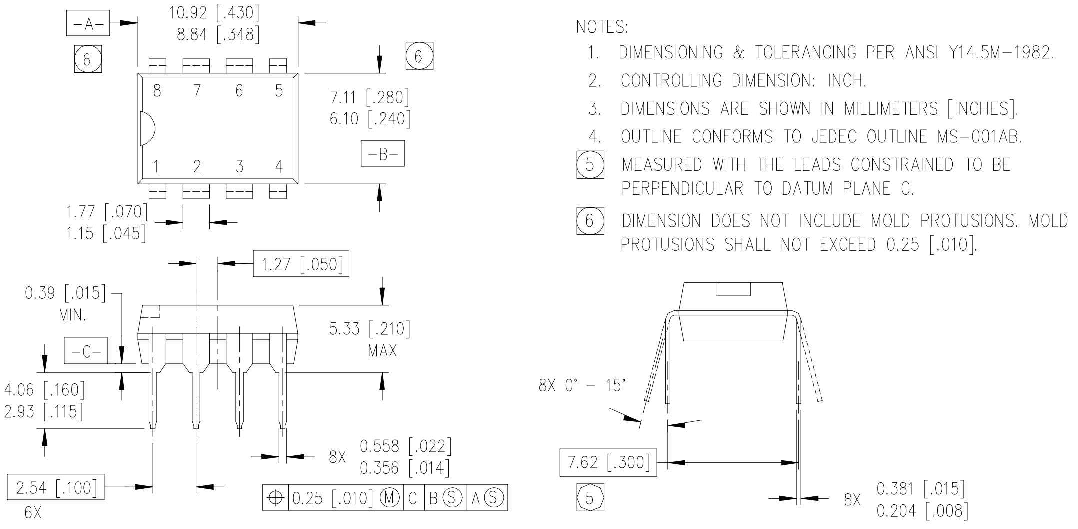


Figure 1. Timing Diagram

Case outlines



NOTES:

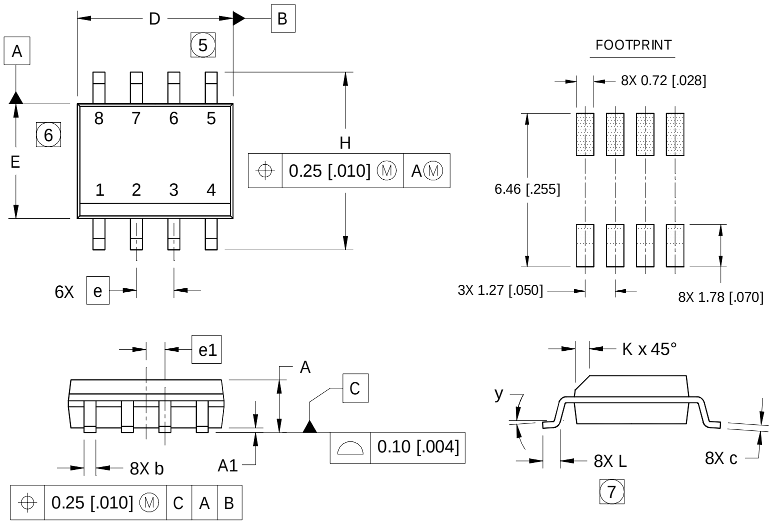
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-001AB.

⑤ MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.

⑥ DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].

8-Lead PDIP

01-6014
01-3003 01 (MS-001AB)



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e 1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°

NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.

⑤ DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 [.006].

⑥ DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.010].

⑦ DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

8-Lead SOIC

01-6027
01-0021 11 (MS-012AA)

Data and specifications subject to change without notice. 5/2/2003