

# IR3Y38M

## CCD Signal Process & Digital Interface IC

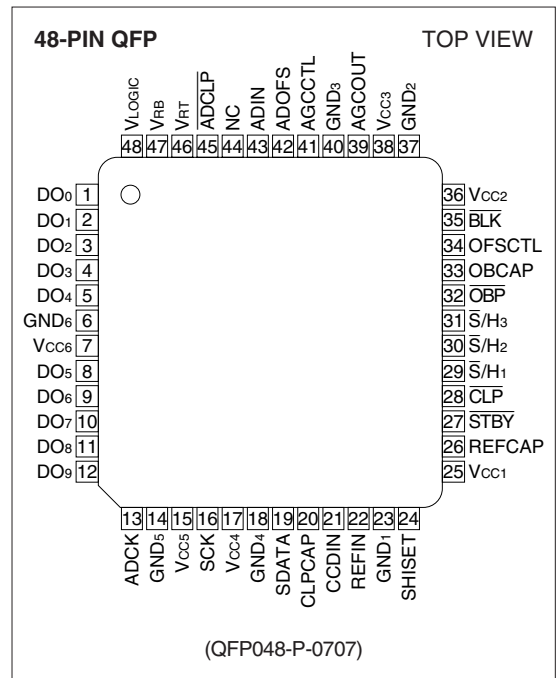
### DESCRIPTION

The IR3Y38M is a bipolar single-chip signal processing IC for CCD area sensors which includes correlated double sampling circuit (CDS), clamp circuit, automatic gain control amplifier (AGC), reference voltage generator, black level detection circuit, 10-bit analog-to-digital converter (ADC), and serial interface for internal circuits.

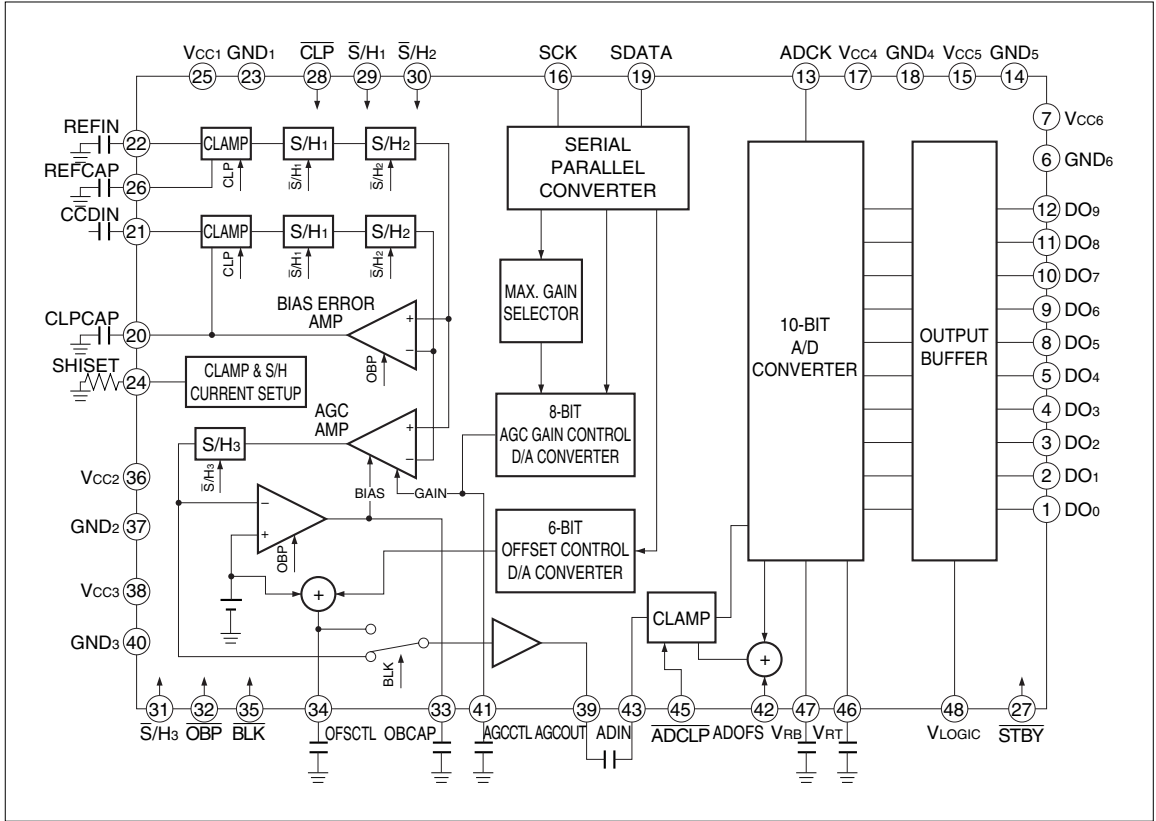
### FEATURES

- Low power consumption : 315 mW (TYP.)
- Wide AGC range : 12 to 43.5 dB
- High speed sample-and-hold circuits : pulse width 12 ns (MIN.)
- Built-in standby mode for power saving applications
- Built-in serial interface to control the AGC gain, maximum gain and offset adjustment
- 10-bit ADC operating up to 18 MHz
- Digital interface for operating 3.3 V logic ICs
- Single +5 V power supply
- Package : 48-pin QFP (QFP048-P-0707) 0.5 mm pin-pitch

### PIN CONNECTIONS


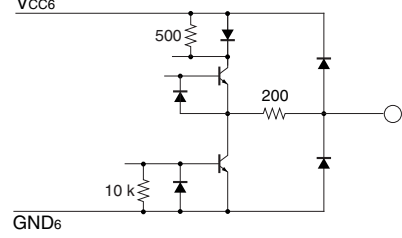
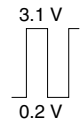
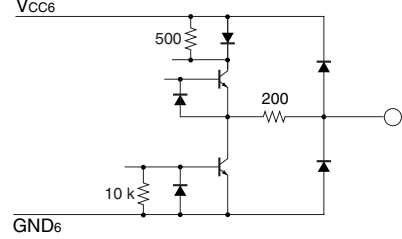
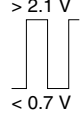
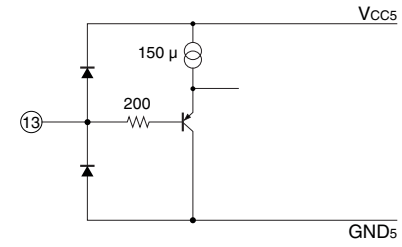

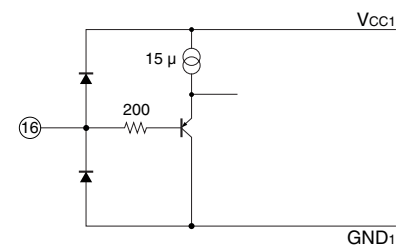


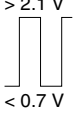
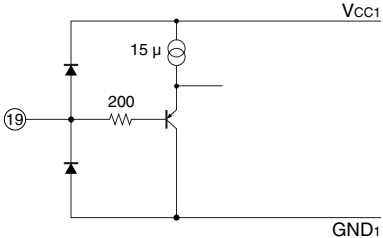
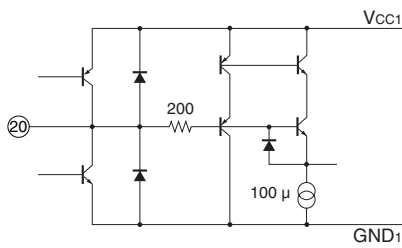
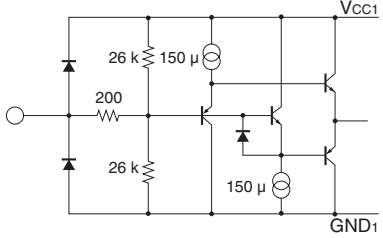
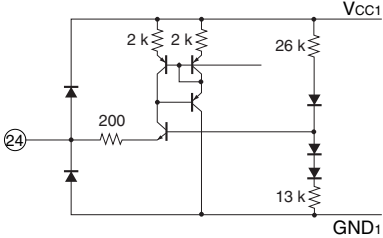
**BLOCK DIAGRAM**



## PIN DESCRIPTION

(The voltage is measured on condition that  $V_{CC1}$  to  $V_{CC6} = +5.0\text{ V}$ ,  $V_{LOGIC} = +3.3\text{ V}$ .)

PIN NO.	PIN NAME	VOLTAGE	EQUIVALENT CIRCUIT	DESCRIPTION
1	DO <sub>0</sub>			Digital data output pins of the A/D converter. DO <sub>0</sub> is LSB. The data format is a straight binary code.  $V_{OL} : 0.2\text{ V (TYP.)}$ $V_{OH} : V_{LOGIC} - 0.2\text{ V (TYP.)}$
2	DO <sub>1</sub>			
3	DO <sub>2</sub>			
4	DO <sub>3</sub>			
5	DO <sub>4</sub>			
6	GND <sub>6</sub>	0.0 V		GND pin of the output buffer of the A/D converter.
7	VCC <sub>6</sub>	5.0 V		Power supply pin of the output buffer of the A/D converter.
8	DO <sub>5</sub>			Digital data output pins of the A/D converter. DO <sub>9</sub> is MSB. The data format is a straight binary code.  $V_{OL} : 0.2\text{ V (TYP.)}$ $V_{OH} : V_{LOGIC} - 0.2\text{ V (TYP.)}$
9	DO <sub>6</sub>			
10	DO <sub>7</sub>			
11	DO <sub>8</sub>			
12	DO <sub>9</sub>			
13	ADCK			Clock input pin of the A/D converter. The A/D conversion is executed at the rising edge of the ADCK, and the data is output at the falling edge of the ADCK. Duty : 50% $f_{max} : 18\text{ MHz (MIN.)}$
14	GND <sub>5</sub>	0.0 V		Digital GND pin of the A/D converter.
15	VCC <sub>5</sub>	5.0 V		Digital power supply pin of the A/D converter.
16	SCK			Clock input pin of the serial interface. Refer to " <b>TRUTH TABLE</b> " of pin 19.

PIN NO.	PIN NAME	VOLTAGE	EQUIVALENT CIRCUIT	DESCRIPTION												
17	V <sub>CC4</sub>	5.0 V		Analog power supply pin of the A/D converter.												
18	GND <sub>4</sub>	0.0 V		Analog GND pin of the A/D converter.												
19	SDATA	 > 2.1 V < 0.7 V		Data input pin of the serial interface. <b>TRUTH TABLE</b> <table border="1" data-bbox="912 396 1227 538"> <thead> <tr> <th>SDATA</th> <th>SCK</th> <th>Action</th> </tr> </thead> <tbody> <tr> <td>DATA</td> <td>↑</td> <td>SHIFT</td> </tr> <tr> <td>0</td> <td>↓</td> <td>—</td> </tr> <tr> <td>1</td> <td>↓</td> <td>STORE</td> </tr> </tbody> </table>	SDATA	SCK	Action	DATA	↑	SHIFT	0	↓	—	1	↓	STORE
SDATA	SCK	Action														
DATA	↑	SHIFT														
0	↓	—														
1	↓	STORE														
20	CLPCAP	3.2 V		Bias decoupling pin of the CDS signal clamp circuit. This pin is connected to the GND <sub>1</sub> via a capacitor.												
21	CCDIN	2.5 V		Signal input pin of the CDS. Input CCD signal to this pin via a capacitor.												
22	REFIN	2.5 V		Reference input pin of the CDS. This pin is connected to the GND <sub>1</sub> via a capacitor.												
23	GND <sub>1</sub>	0.0 V		GND pin of the CDS/AGC. Pay careful attention to board layout of the GND <sub>1</sub> because the CDS/AGC are noise-sensitive circuitry.												
24	SHISET	1.7 V		Operation current setting pin of the CDS and $\bar{S}/H_3$ circuits. This pin is connected to the GND <sub>1</sub> via a resistor. The slew rates of the $\bar{S}/H_3$ are in inverse proportion to the value of the resistor.												

PIN NO.	PIN NAME	VOLTAGE	EQUIVALENT CIRCUIT	DESCRIPTION
25	VCC1	5.0 V		Power supply pin of the CDS/AGC.
26	REFCAP	3.2 V		Bias decoupling pin of the CDS reference clamp circuit. This pin is connected to the GND <sub>1</sub> via a capacitor.
27	STBY	5.0 V (open) > 2.1 V < 0.7 V		Standby function control pin. All actions stop and the power consumption is decreased when low. The threshold voltage has 0.4 V hysteresis. Connect to the Vcc if not used.
28	CLP			Pulse input pin of the CDS feed-through level clamp. Signal is clamped when low.
29	S/H1			Pulse input pin of the S/H1. Signal is sampled when low.
30	S/H2			Pulse input pin of the S/H2. Signal is sampled when low.
31	S/H3			Pulse input pin of the S/H3. Signal is sampled when low.
32	OBP			Pulse input pin of the OPB clamp and bias error amplifier. Signal is clamped when low.
33	OBCAP			3.7 V

PIN NO.	PIN NAME	VOLTAGE	EQUIVALENT CIRCUIT	DESCRIPTION
34	OFSCCTL	2.15 to 2.30 V		Decoupling capacitor pin of the blanking offset control D/A converter. Connect to the GND1 via a capacitor.
35	BLK			Blanking pulse input pin. The output of the AGCOUT pin is blanked when low. The blanking level can be controlled by the serial interface.
36	VCC2	5.0 V		Power supply pin of the $\bar{S}/H_3$ and OPB clamp circuits.
37	GND2	0.0 V		GND pin of the $\bar{S}/H_3$ and OPB clamp circuits.
38	VCC3	5.0 V		Power supply pin of the output buffer circuit connected to the AGCOUT pin.
39	AGCOUT	0.9 V ( $\overline{OBP} = L$ )		Signal output pin of the AGC. Connect to the ADIN pin via a capacitor.
40	GND3	0.0 V		GND pin of the output buffer circuit connected to the AGCOUT pin.
41	AGCCTL	2.5 to 3.8 V		Decoupling capacitor pin of the AGC gain control D/A converter. Connect to the GND1 via a capacitor.

PIN NO.	PIN NAME	VOLTAGE	EQUIVALENT CIRCUIT	DESCRIPTION
42	ADOFS	3.3 V (open)  Input range 1.6 to 5.0 V		Voltage adjustment pin of the ADC black level clamp. This pin is biased at 3.3 V from the inside of the IC. Connect to the GND4 via a capacitor if not used.
43	ADIN	1.4 V (ADCLP = L)		Signal input pin of the ADC. Connect to the AGCOUT pin via a capacitor. This capacitor is also used as the clamp capacitor of the ADC blank level clamp.
44	NC			No connection. It is recommended to connect to GND for better heat radiation and avoiding noise.
45	ADCLP			Pulse input pin of the ADC black level clamp. Signal is clamped when low. When the ADOFS is opened, the clamped level is set to make the ADC output 61 (decimal).
46	VRT	3.90 V		Upper reference decoupling pin of the ADC. Connect to the GND4 via a capacitor.
47	VRB	1.95 V		Lower reference decoupling pin of the ADC. Connect to the GND4 via a capacitor.

PIN NO.	PIN NAME	VOLTAGE	EQUIVALENT CIRCUIT	DESCRIPTION
48	VLOGIC	3.3 V		ADC output voltage setting pin. The high level voltage of the DO <sub>0</sub> to DO <sub>9</sub> pins is set to V <sub>LOGIC</sub> – 0.2 V. It is recommended to connect to the power supply of the following logic ICs.

## FUNCTIONAL DESCRIPTION

### CDS Circuit

The clamp circuit clamps the feed-through level of the CCD signal with the  $\overline{\text{CLP}}$  pulse. Then the  $\overline{\text{S}}/\text{H}_1$  circuit samples the signal period of the one with the  $\overline{\text{S}}/\text{H}_1$  pulse and holds on. Thus the video signal is obtained. But this signal has a level drop caused by the reset pulse of the CCD signal, and for removing it, the  $\overline{\text{S}}/\text{H}_2$  circuit samples this signal again with the  $\overline{\text{S}}/\text{H}_2$  pulse.

For reducing the effect of the sampling pulse or other noise sources, the CDS circuit is formed with a differential structure.

### Bias Error Amplifier Circuit

For stabilizing the bias level of the CDS circuit and reducing the offset of the AGC circuit, the bias error amplifier acts with the  $\overline{\text{OBP}}$  pulse during the OPB period.

### AGC Amplifier Circuit

The AGC amplifier amplifies the video signal obtained by the CDS circuit. The gain of the AGC is controlled by the value of the AGCGAIN serial register. And the maximum gain of the AGC is controlled by the value of the GAINSEL serial register.

### OPB Clamp Circuit

For clamping the level of the amplified signal to the black level, the OPB clamp circuit acts with the  $\overline{\text{OBP}}$  pulse during the OPB period.

### Blanking Circuit

The output signal is fixed to the blanking level with the  $\overline{\text{BLK}}$  pulse. The blanking level is the sum of the black level and the offset value decided by the value of the OFFSET serial register.

### A/D Converter Circuit

The  $\overline{\text{S}}/\text{H}_3$  circuit samples the amplified signal with the  $\overline{\text{S}}/\text{H}_3$  pulse and the A/D converter converts the sampled signal to 10-bit straight binary digital data. The clamp circuit placed in front of the A/D converter clamps the signal level beside the lower limit of the convertible input range with the  $\overline{\text{ADCLP}}$  pulse. The clamped level is controllable by the voltage of the ADOFS pin.

The A/D conversion is executed at the rising edge of the ADCK clock, and the data is output at the falling edge.

The high level voltage of the outputs is controlled by the voltage of the VLOGIC pin.

### Standby Function

By making the  $\overline{\text{STBY}}$  pin low, all actions of this IC stop and power consumption is decreased.

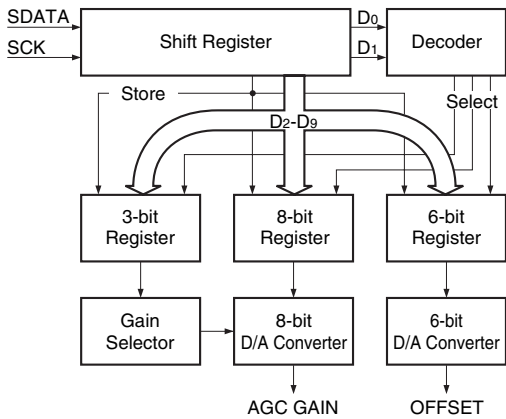
The outputs of the A/D converter (DO<sub>0</sub> to DO<sub>9</sub>) turn to high impedance when on standby.

### Serial Interface Circuit

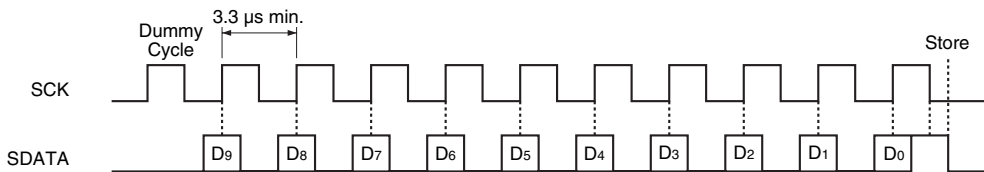
The IR3Y38M has a serial interface to control the gain of the AGC amplifier and the offset of the blanking level. This interface is constituted by a shift register for serial-parallel conversion, data registers and D/A converters.

The data input to SDATA is fetched and shifted at

the rising edge of the SCK. While transmitting data, the SDATA must be low when the SCK falls. When the SDATA is high and the SCK falls, the data on the shift register is stored at the selected data register at the following falling edge of the SDATA. The stored data register is selected by the data of the D0 and D1 bits.

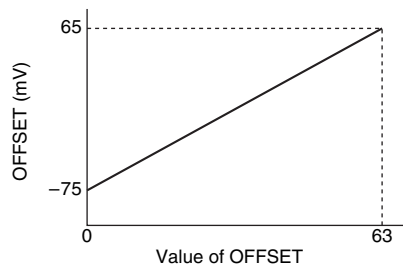
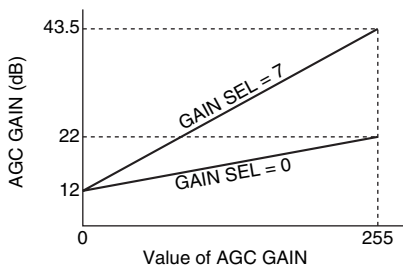


GAIN SEL	MAXIMUM GAIN (dB)
0	22
1	25
2	28
3	31.5
4	34.5
5	38
6	41
7	43.5

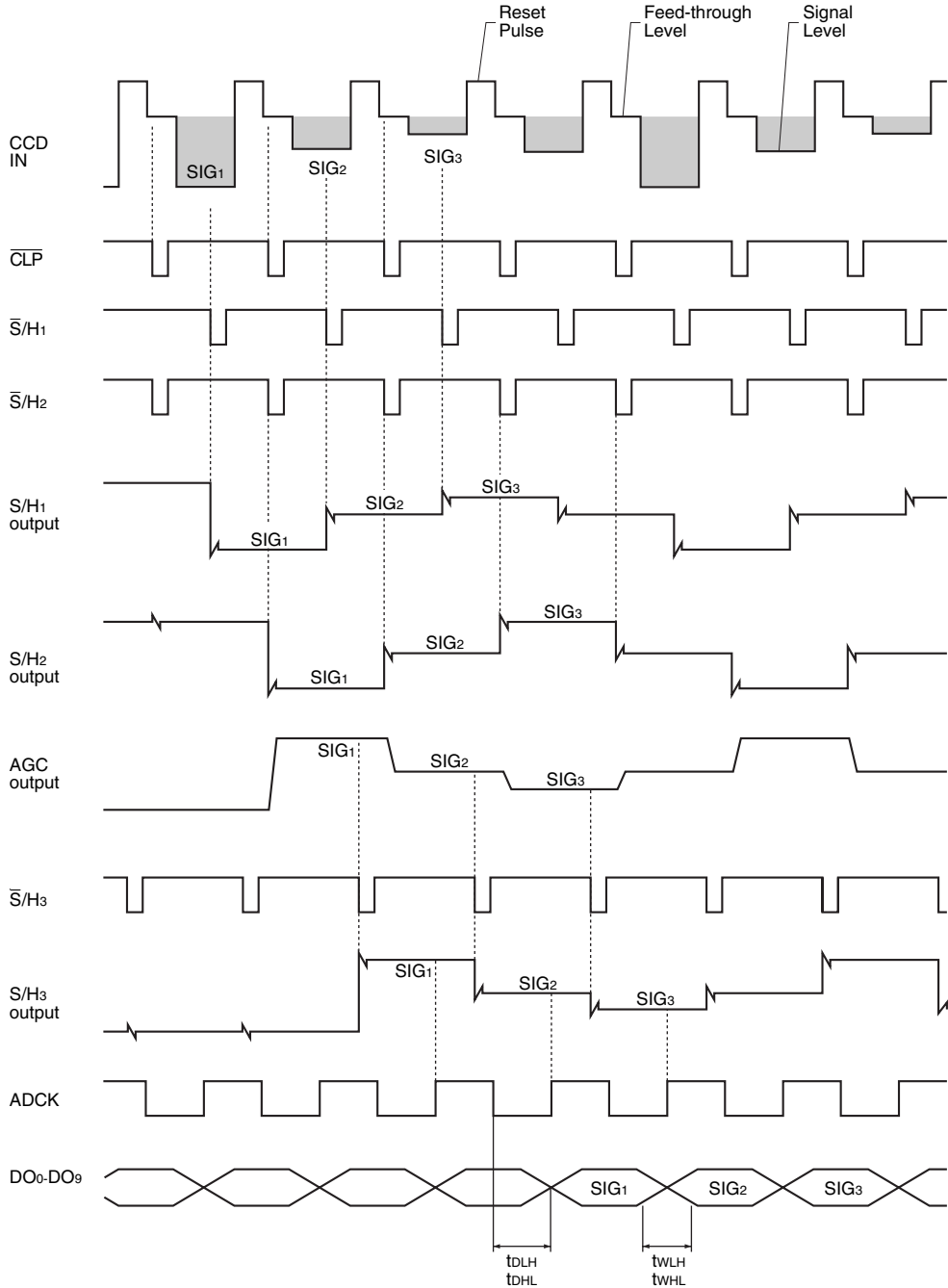


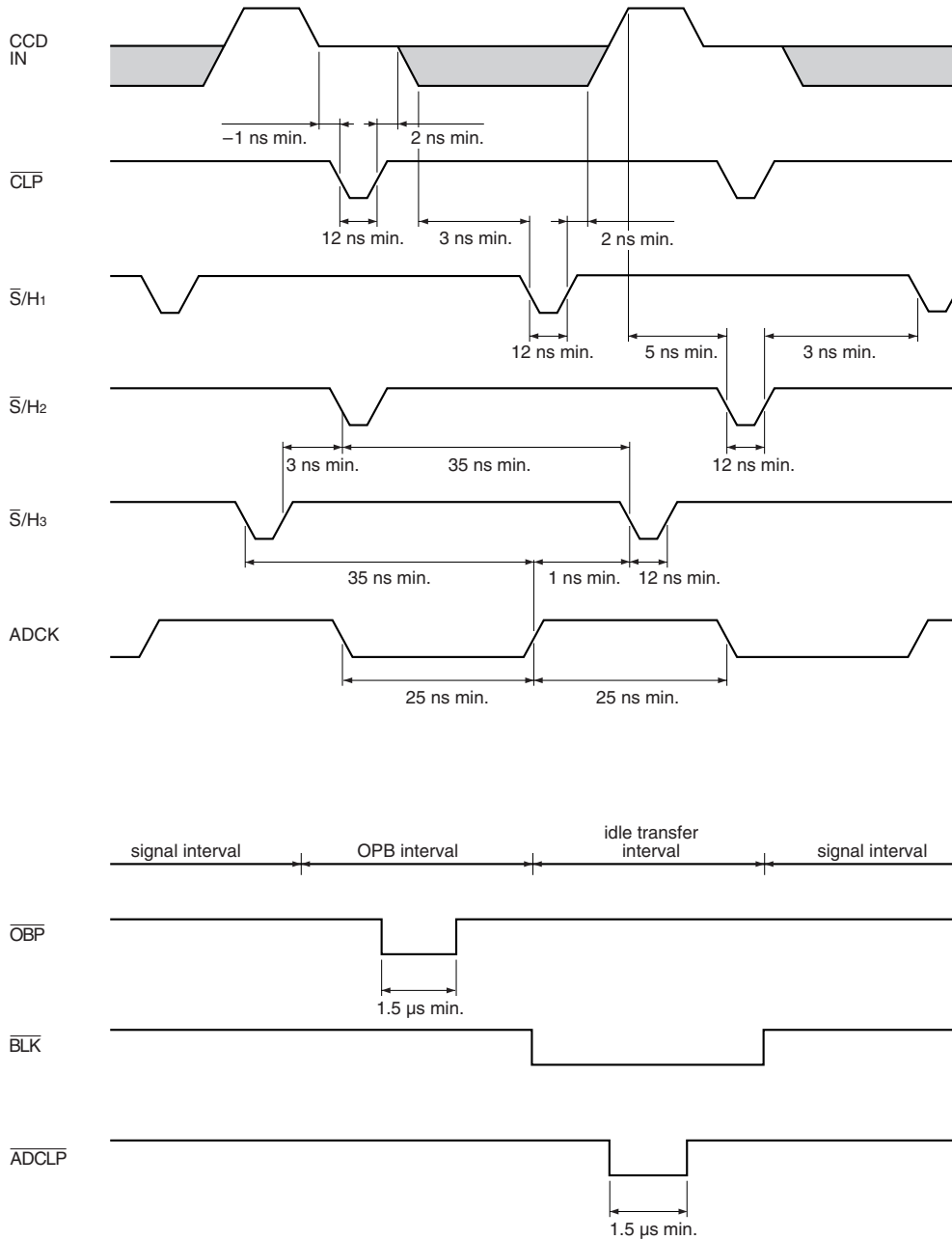
DATA REGISTER	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
GAIN SEL	/	/	/	/	/	d0	d1	d2	0	0
AGC GAIN	d0	d1	d2	d3	d4	d5	d6	d7	0	1
OFFSET	/	/	d0	d1	d2	d3	d4	d5	1	0
(Don't care)	/	/	/	/	/	/	/	/	1	1

LSB MSB



TIMING CHART





## PRECAUTIONS

Each VCC1 to VCC6 pin corresponds to the each GND1 to GND6 pin. Connect a ceramic capacitor as near the IC as possible between each corresponding Vcc pin and GND pin.

The GND1 pin is the ground of the CDS/ADC circuit handling a weak signal. Pay careful attention to the board layout of the GND1 pattern in order to avoid the potential fluctuation of the GND1 caused by the current of the other GND pins. Especially pay attention to the current of the GND6 pin's flowing spiky current.

All the GND pins must be at the same potential and not open. And keep the potential difference of each Vcc pin within 0.3 V.

The high level voltage of the outputs of the A/D

converter is controllable by the voltage of the VLOGIC pin, but take care that the high level voltage does not fall below about 1.5 V, in spite of making the VLOGIC pin 0 V. This may cause the latch up of the following logic ICs if the power supply of this IC rises up faster than the power supply of the following logic. To avoid this problem, it is recommended to make the STBY pin low until the voltage of the logic power supply becomes stable. Take care too that the high level voltage does not rise above about  $V_{CC} - 1.0$  V, in spite of making the VLOGIC pin the Vcc potential.

Restore the value of the serial register when setting up the power supply or making the STBY pin high because the value will have been removed in that case.

## ABSOLUTE MAXIMUM RATINGS

(Unless otherwise specified,  $T_A = +25$  °C)

PARAMETER	SYMBOL	CONDITIONS	RATING	UNIT
Supply voltage	VCC1-VCC6		7	V
Input voltage	V <sub>IN</sub>		-0.3 to V <sub>CC</sub> + 0.3	V
Power consumption	P <sub>D</sub>	$T_A \leq +25$ °C	570	mW
P <sub>D</sub> derating ratio		$T_A > +25$ °C	4.5	mW/°C
Operating temperature	T <sub>OPR</sub>		-30 to +70	°C
Storage temperature	T <sub>STG</sub>		-55 to +150	°C

## RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	APPLICABLE PINS	RATING	UNIT
Supply voltage	VCC1-VCC6		4.75 to 5.25	V
Standard CCD input signal level	V <sub>CCD</sub>	CCDIN	200	mVp-p
Input "Low" voltage	V <sub>IL</sub>	ADCK, SCK, SDATA, STBY, CLP, S/H1, S/H2,	0 to 0.7	V
Input "High" voltage	V <sub>IH</sub>	S/H3, OBP, BLK, ADCLP	2.1 to V <sub>CC</sub>	V
S/H pulse width	t <sub>WS/H</sub>	CLP, S/H1, S/H2, S/H3	≥ 12	ns
Clamp pulse width	t <sub>WC</sub>	OBP, ADCLP	≥ 1.5	μs
A/D converter clock frequency	f <sub>ADCK</sub>	ADCK	≤ 18	MHz
Serial interface clock frequency	f <sub>SCK</sub>	SCK	≤ 300	kHz

## ELECTRICAL CHARACTERISTICS

## DC Characteristics

(Unless otherwise specified,  $T_A = +25\text{ }^\circ\text{C}$ ,  $V_{CC1} = V_{CC2} = V_{CC3} = V_{CC4} = V_{CC5} = V_{CC6} = 5.0\text{ V}$ ,  $V_{LOGIC} = 3.3\text{ V}$ ,  $ADCK = 0\text{ V}$ ,  $SCK = 0\text{ V}$ ,  $SDATA = 0\text{ V}$ ,  $\overline{STBY} = 3.3\text{ V}$ ,  $\overline{CLP} = 0\text{ V}$ ,  $\overline{S}/H_1 = 0\text{ V}$ ,  $\overline{S}/H_2 = 0\text{ V}$ ,  $\overline{S}/H_3 = 0\text{ V}$ ,  $\overline{BLK} = 3.3\text{ V}$ ,  $\overline{OBP} = 0\text{ V}$ ,  $SW42 = \text{OFF}$ ,  $SW43 = (\text{a})$ ,  $\overline{ADCLP} = 3.3\text{ V}$ )

The current direction flowing into the pin is positive direction.

## • General

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply current (1)	I <sub>CC1</sub>	Measure pin 25 ( $V_{CC1}$ )	–	27	34	mA
Supply current (2)	I <sub>CC2</sub>	Measure pin 36 ( $V_{CC2}$ ).	–	2.3	2.8	mA
Supply current (3)	I <sub>CC3</sub>	Measure pin 38 ( $V_{CC3}$ ).	–	0.7	1.0	mA
Supply current (4)	I <sub>CC4</sub>	Measure pin 17 ( $V_{CC4}$ ).	–	13	20	mA
Supply current (5)	I <sub>CC5</sub>	Measure pin 15 ( $V_{CC5}$ ).	–	16	21	mA
Supply current (6)	I <sub>CC6</sub>	Measure pin 7 ( $V_{CC6}$ ).	–	5.0	6.5	mA
Total supply current	I <sub>CC</sub>	Total of I <sub>CC1</sub> to I <sub>CC6</sub>	–	63	77	mA
Standby supply current	I <sub>STBY</sub>	$\overline{STBY} = 0\text{ V}$ , Total of I <sub>CC1</sub> to I <sub>CC6</sub> .	–	4.5	6.5	mA
Input "Low" current (1)	I <sub>IL1</sub>	Apply to pin 28 ( $\overline{CLP}$ ), pin 29 ( $\overline{S}/H_1$ ), pin 30 ( $\overline{S}/H_2$ ), pin 31 ( $\overline{S}/H_3$ ), and pin 32 ( $\overline{OBP}$ ). $V_{IL} = 0\text{ V}$	–3.5	–2.0	–	$\mu\text{A}$
Input "High" current (1)	I <sub>IH1</sub>	Apply to pin 28 ( $\overline{CLP}$ ), pin 29 ( $\overline{S}/H_1$ ), pin 30 ( $\overline{S}/H_2$ ), pin 31 ( $\overline{S}/H_3$ ), and pin 32 ( $\overline{OBP}$ ). $V_{IH} = 3.3\text{ V}$	–	0	0.1	$\mu\text{A}$
Input "Low" current (2)	I <sub>IL2</sub>	Apply to pin 16 (SCK) and pin 19 (SDATA). $V_{IL} = 0\text{ V}$	–0.3	–0.2	–	$\mu\text{A}$
Input "High" current (2)	I <sub>IH2</sub>	Apply to pin 16 (SCK) and pin 19 (SDATA). $V_{IH} = 3.3\text{ V}$	–	0	0.1	$\mu\text{A}$
Input "Low" current (3)	I <sub>IL3</sub>	Apply to pin 35 ( $\overline{BLK}$ ) and pin 45 ( $\overline{ADCLP}$ ). $V_{IL} = 0\text{ V}$	–0.5	–0.3	0	$\mu\text{A}$
Input "High" current (3)	I <sub>IH3</sub>	Apply to pin 35 ( $\overline{BLK}$ ) and pin 45 ( $\overline{ADCLP}$ ). $V_{IH} = 3.3\text{ V}$	–	0	0.1	$\mu\text{A}$
Input "Low" current (4)	I <sub>IL4</sub>	Apply to pin 13 (ADCK). $V_{IL} = 0\text{ V}$	–3.5	–2.0	–	$\mu\text{A}$
Input "High" current (4)	I <sub>IH4</sub>	Apply to pin 13 (ADCK). $V_{IH} = 3.3\text{ V}$	–	0	0.1	$\mu\text{A}$
$\overline{STBY}$ voltage	V <sub>27</sub>	Open pin 27 ( $\overline{STBY}$ ).	4.5	5.0	–	V
$\overline{STBY}$ impedance	Z <sub>27</sub>		70	110	140	k $\Omega$

## • CDS &amp; AGC Circuits

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CLPCAP voltage	V <sub>20</sub>		2.9	3.2	3.6	V
CCDIN voltage	V <sub>21</sub>		2.3	2.5	2.8	V
REFIN voltage	V <sub>22</sub>		2.3	2.5	2.8	V
SHISET voltage	V <sub>24</sub>		1.5	1.7	1.9	V
REFCAP voltage	V <sub>26</sub>		2.9	3.2	3.6	V
OBCAP voltage	V <sub>33</sub>		3.3	3.7	4.0	V
AGCOUT voltage	V <sub>39</sub>		0.7	0.9	1.1	V
CCDIN impedance	Z <sub>21</sub>		9	13	18	kΩ
REFIN impedance	Z <sub>22</sub>		9	13	18	kΩ
REFCAP impedance	Z <sub>26</sub>		15	23	32	kΩ
OFSCCTL impedance	Z <sub>34</sub>		6	9	12	kΩ
AGCCTL impedance	Z <sub>41</sub>		7	11	15	kΩ
CLPCAP charge current	I <sub>L20</sub>	CLPCAP = 2.8 V, OBP = 0 V Measure the current of CLPCAP.	–	–135	–110	μA
CLPCAP discharge current	I <sub>H20</sub>	CLPCAP = 3.6 V, OBP = 0 V Measure the current of CLPCAP.	110	135	–	μA
CLPCAP leakage current	I <sub>Z20</sub>	CLPCAP = 3.2 V, OBP = 3.3 V Measure the current of CLPCAP.	–0.5	0	0.5	μA
OBCAP charge current	I <sub>L33</sub>	OBCAP = 3.3 V, OBP = 0 V Measure the current of OBCAP.	–	–90	–65	μA
OBCAP discharge current	I <sub>H33</sub>	OBCAP = 4.1 V, OBP = 0 V Measure the current of OBCAP.	65	90	–	μA
OBCAP leakage current	I <sub>Z33</sub>	OBCAP = 3.7 V, OBP = 3.3 V Measure the current of OBCAP.	–0.5	0	0.5	μA

## • A/D Converter Circuit

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
ADOFS voltage	V <sub>42</sub>		3.0	3.3	3.6	V
ADIN voltage	V <sub>43</sub>	ADCLP = 0 V	1.2	1.4	1.6	V
V <sub>RT</sub> voltage	V <sub>46</sub>		3.7	3.9	4.1	V
V <sub>RB</sub> voltage	V <sub>47</sub>		1.8	1.95	2.2	V
ADOFS impedance	Z <sub>42</sub>		50	70	90	kΩ
ADIN charge current	I <sub>L43</sub>	ADIN = 1.0 V, ADCLP = 0 V Measure the current of ADIN.	–	–45	–30	μA
ADIN discharge current	I <sub>H43</sub>	ADIN = 1.8 V, ADCLP = 0 V Measure the current of ADIN.	30	45	–	μA
ADIN leakage current	I <sub>Z43</sub>	ADIN = 1.4 V, ADCLP = 3.3 V Measure the current of ADIN.	–0.3	0	0.3	μA
Output "Low" voltage	V <sub>OL</sub>	SW43 = (b), ADCIN = 0.8 V Change the level of ADCK to L→H→L, then measure the voltages of DO <sub>0</sub> to DO <sub>9</sub> pins.	–	0.2	0.4	V
Output "High" voltage	V <sub>OH</sub>	SW43 = (b), ADCIN = 3.5 V Change the level of ADCK to L→H→L, then measure the voltages of DO <sub>0</sub> to DO <sub>9</sub> pins.	2.9	3.1	–	V

## AC Characteristics

(Unless otherwise specified,  $T_A = +25\text{ }^\circ\text{C}$ ,  $V_{CC1} = V_{CC2} = V_{CC3} = V_{CC4} = V_{CC5} = V_{CC6} = 5.0\text{ V}$ ,  $V_{LOGIC} = 3.3\text{ V}$ ,  $ADCK = 0\text{ V}$ ,  $SCK = 0\text{ V}$ ,  $SDATA = 0\text{ V}$ ,  $\overline{STBY} = 3.3\text{ V}$ ,  $\overline{CLP} = 3.3\text{ V}$ ,  $\overline{S}/H_1 = 0\text{ V}$ ,  $\overline{S}/H_2 = 0\text{ V}$ ,  $\overline{S}/H_3 = 0\text{ V}$ ,  $\overline{BLK} = 3.3\text{ V}$ ,  $\overline{OBP} = 3.3\text{ V}$ ,  $SW42 = \text{OFF}$ ,  $SW43 = (a)$ ,  $\overline{ADCLP} = 3.3\text{ V}$ ,  $(\text{OFFSET}) = 32$ )

The value of the serial register is written with decimal.

### • CDS & AGC Circuits

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
AGC minimum gain	GAN	(GAIN SEL) = 0, (AGC GAIN) = 0 $\overline{CLP} = \text{SG2}$ , $\overline{OBP} = \text{SG3}$ Input the attenuated SG1 ( $f = 2\text{ MHz}$ , $V = 1.6\text{ Vp-p}$ ) to the SIN and seek the attenuation amount to make the amplitude of AGCOUT $1.6\text{ Vp-p}$ .	11	12	13	dB
AGC maximum gain (0)	GAX0	(GAIN SEL) = 0, (AGC GAIN) = 255 Measure the gain using the same procedure as for the measurement of GAN.	20.5	22	24.5	dB
AGC maximum gain (1)	GAX1	(GAIN SEL) = 1, (AGC GAIN) = 255 Measure the gain using the same procedure as for the measurement of GAN.	23	25	28	dB
AGC maximum gain (2)	GAX2	(GAIN SEL) = 2, (AGC GAIN) = 255 Measure the gain using the same procedure as for the measurement of GAN.	26	28	31	dB
AGC maximum gain (3)	GAX3	(GAIN SEL) = 3, (AGC GAIN) = 255 Measure the gain using the same procedure as for the measurement of GAN.	28.5	31.5	35	dB
AGC maximum gain (4)	GAX4	(GAIN SEL) = 4, (AGC GAIN) = 255 Measure the gain using the same procedure as for the measurement of GAN.	31	34.5	38	dB
AGC maximum gain (5)	GAX5	(GAIN SEL) = 5, (AGC GAIN) = 255 Measure the gain using the same procedure as for the measurement of GAN.	34	38	42	dB
AGC maximum gain (6)	GAX6	(GAIN SEL) = 6, (AGC GAIN) = 255 Measure the gain using the same procedure as for the measurement of GAN.	36.5	41	44.5	dB
AGC maximum gain (7)	GAX7	(GAIN SEL) = 7, (AGC GAIN) = 255 Measure the gain using the same procedure as for the measurement of GAN.	38.5	43.5	47.5	dB
AGC gain variable width	GAR	$GAR = GAX7 - GAN$	26.5	31.5	35.5	dB

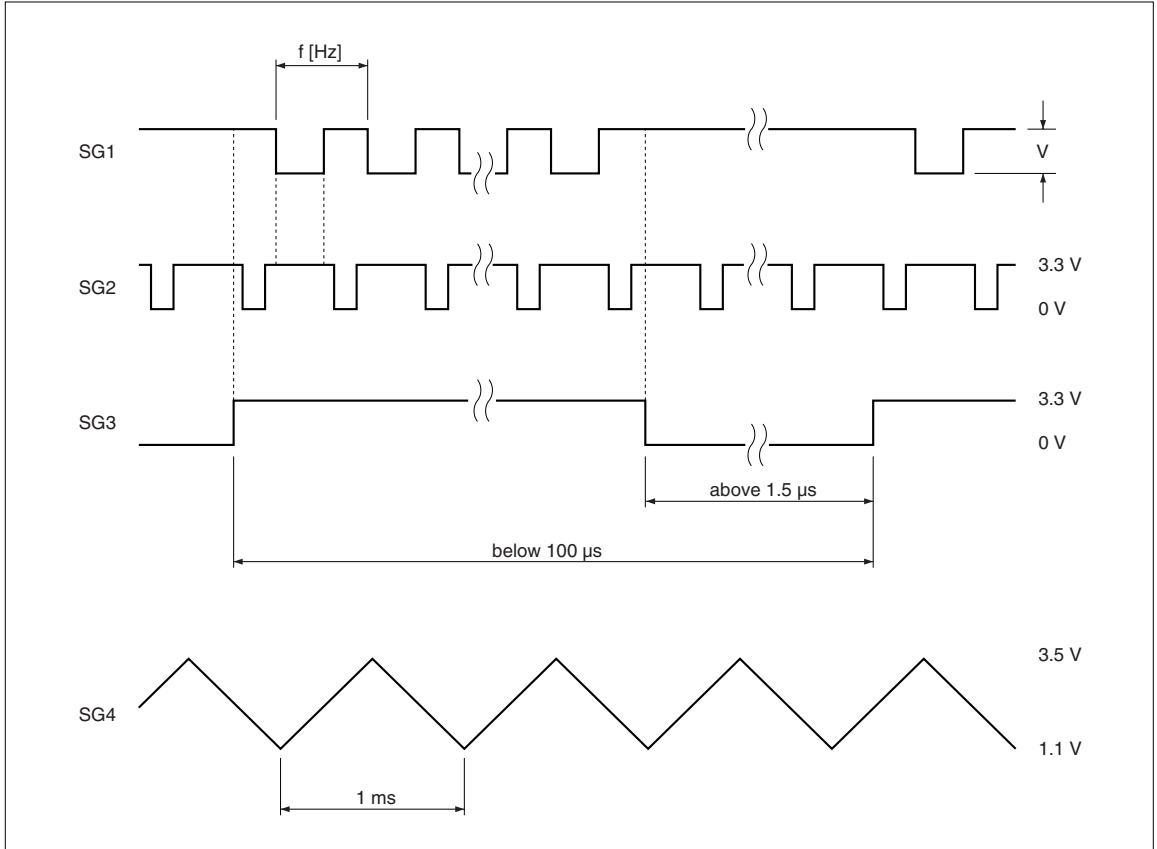
PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Bandwidth (1) (Minimum gain)	ftN	(GAIN SEL) = 0, (AGC GAIN) = 0 $\overline{CLP}$ = SG2, $\overline{OBP}$ = SG3 Input the SG1 (f = 2 MHz, V = 0.2 Vp-p) to the SIN and measure the amplitude of the AGCOUT. Increase the frequency and measure the frequency when the amplitude attenuates to -3 dB.	24	35	-	MHz
Bandwidth (2) (Maximum gain)	ftX	(GAIN SEL) = 7, (AGC GAIN) = 255 $\overline{CLP}$ = SG2, $\overline{OBP}$ = SG3 Input the SG1 (f = 2 MHz, V = 8 mVp-p) to the SIN and measure the amplitude of the AGCOUT. Increase the frequency and measure the frequency when the amplitude attenuates to -3 dB.	13	20	-	MHz
OFFSET adjustment limit (1) (OFFSET = 0)	V <sub>BON</sub>	(GAIN SEL) = 0, (AGC GAIN) = 0 SIN = GND <sub>1</sub> , (OFFSET) = 0, $\overline{CLP}$ = 0 V, $\overline{OBP}$ = 0 V Measure the voltage of the AGCOUT at BLK = 3.3 V and define it V <sub>BO11</sub> . Measure the one similarly at BLK = 0 V and define it V <sub>BO12</sub> . V <sub>BON</sub> = V <sub>BO12</sub> - V <sub>BO11</sub>	-	-75	-60	mV
OFFSET adjustment limit (2) (OFFSET = 63)	V <sub>BOX</sub>	(GAIN SEL) = 0, (AGC GAIN) = 0 SIN = GND <sub>1</sub> , (OFFSET) = 63, $\overline{CLP}$ = 0 V, $\overline{OBP}$ = 0 V Measure the V <sub>BO21</sub> and V <sub>BO22</sub> similarly to above-mentioned method. V <sub>BON</sub> = V <sub>BO22</sub> - V <sub>BO21</sub>	50	65	-	mV
Output dynamic range (1) (Minimum gain)	V <sub>DYN</sub>	(GAIN SEL) = 0, (AGC GAIN) = 0 $\overline{CLP}$ = SG2, $\overline{OBP}$ = SG3 Input the SG1 (f = 2 MHz, V = 0.9 Vp-p) to the SIN and measure the amplitude of the AGCOUT.	2.0	2.2	-	Vp-p
Output dynamic range (2) (Maximum gain)	V <sub>DYX</sub>	(GAIN SEL) = 7, (AGC GAIN) = 255 $\overline{CLP}$ = SG2, $\overline{OBP}$ = SG3 Input the SG1 (f = 2 MHz, V = 50 mVp-p) to the SIN and measure the amplitude of the AGCOUT.	2.0	2.2	-	Vp-p

### • A/D Converter Circuit

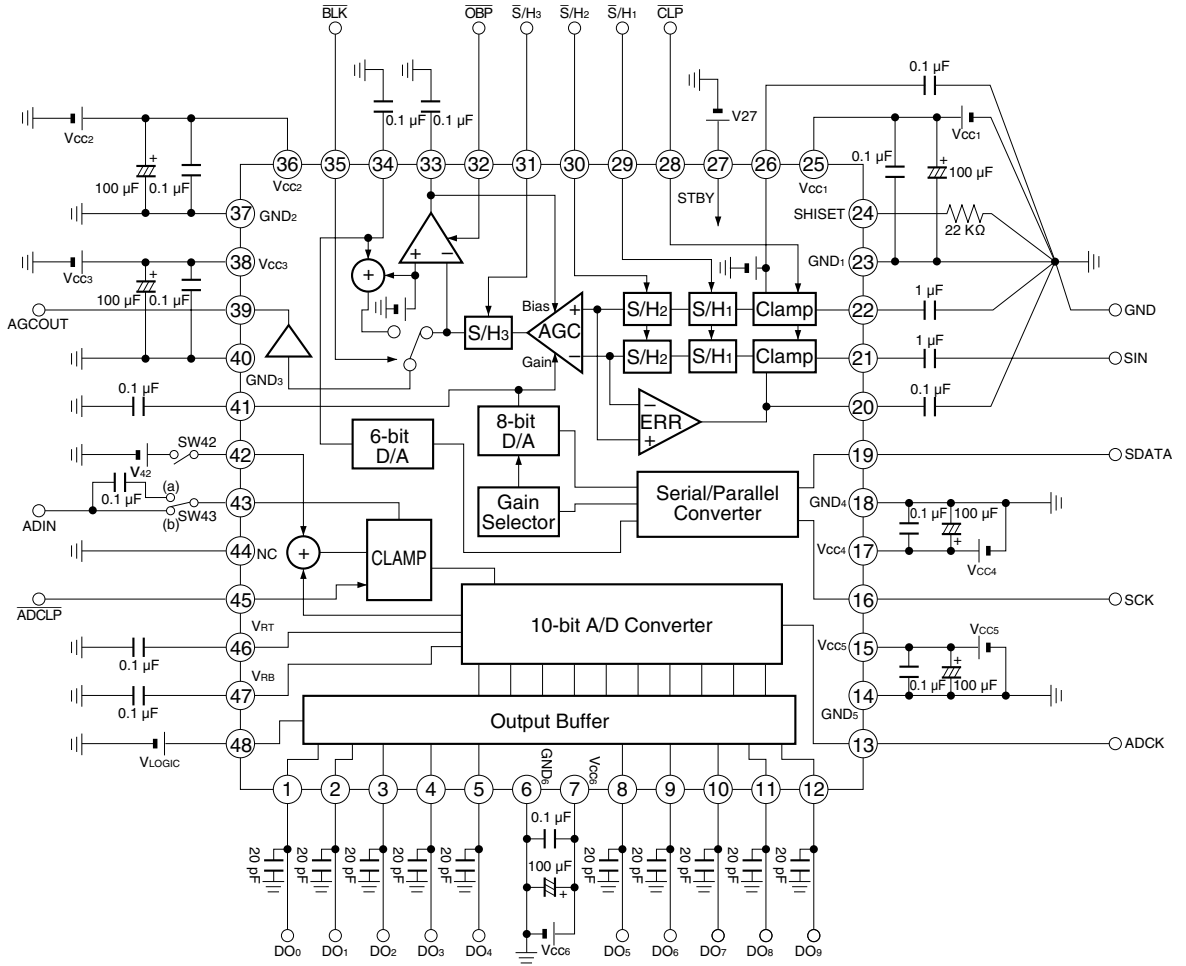
(Unless otherwise specified,  $T_A = +25\text{ }^\circ\text{C}$ ,  $V_{CC1} = V_{CC2} = V_{CC3} = V_{CC4} = V_{CC5} = V_{CC6} = 5.0\text{ V}$ ,  $V_{LOGIC} = 3.3\text{ V}$ ,  $ADCK = 18\text{ MHz}$  square wave,  $SCK = 0\text{ V}$ ,  $\overline{SDATA} = 0\text{ V}$ ,  $\overline{STBY} = 3.3\text{ V}$ ,  $\overline{CLP} = 3.3\text{ V}$ ,  $\overline{S/H1} = 0\text{ V}$ ,  $\overline{S/H2} = 0\text{ V}$ ,  $\overline{S/H3} = 0\text{ V}$ ,  $BLK = 3.3\text{ V}$ ,  $\overline{OBP} = 3.3\text{ V}$ ,  $SW42 = \text{OFF}$ ,  $SW43 = (b)$ ,  $\overline{ADCLP} = 3.3\text{ V}$ )

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Clamp value	DCLP	SW43 = (a) $\overline{ADCLP} = 0\text{ V}$ ADCIN = GND <sub>4</sub> Read the output value of DO <sub>0</sub> to DO <sub>9</sub> .	56	61	66	–
Clamp value adjustment limit (1)	DCLPN	SW42 = ON, V <sub>42</sub> = 5.0 V, $\overline{ADCLP} = 0\text{ V}$ , ADCIN = GND <sub>4</sub> Read the output value of DO <sub>0</sub> to DO <sub>9</sub> .	31	36	41	–
Clamp value adjustment limit (2)	DCLPX	SW42 = ON, V <sub>42</sub> = 1.6 V, $\overline{ADCLP} = 0\text{ V}$ , ADCIN = GND <sub>4</sub> Read the output value of DO <sub>0</sub> to DO <sub>9</sub> .	81	86	91	–
Differential linearity error	DLE	ADCIN = SG <sub>4</sub> Read the output value of DO <sub>0</sub> to DO <sub>9</sub> at about 10 <sup>6</sup> times and make it a histogram. Normalize the histogram and obtain the DLE.	–	±0.5	±0.9	LSB
Integral linearity error	ILE	Integrate the histogram and obtain the ILE.	–	±3	±7	LSB
Propagation delay (L→H)	tDLH	ADCIN = SG <sub>4</sub> , C <sub>L</sub> = 20 pF Measure the delay time from the falling edge (50%) of the ADCK to the rising edge (50%) of the DO <sub>0</sub> to DO <sub>9</sub> .	15	26	38	ns
Propagation delay (H→L)	tDHL	ADCIN = SG <sub>4</sub> , C <sub>L</sub> = 20 pF Measure the delay time from the falling edge (50%) of the ADCK to the falling edge (50%) of the DO <sub>0</sub> to DO <sub>9</sub> .	15	26	38	ns
Output rise time	twLH	ADCIN = SG <sub>4</sub> , C <sub>L</sub> = 20 pF Measure the rise time (10%→90%) of the DO <sub>0</sub> to DO <sub>9</sub> .	10	17	25	ns
Output fall time	twHL	ADCIN = SG <sub>4</sub> , C <sub>L</sub> = 20 pF Measure the fall time (90%→10%) of the DO <sub>0</sub> to DO <sub>9</sub> .	10	17	25	ns

### Measurement Waveforms



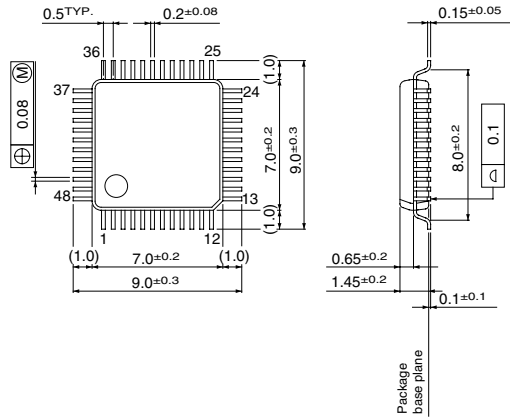
Test Circuit



## PACKAGE

(Unit : mm)

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