

## FEATURES

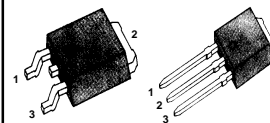
- Avalanche Rugged Technology
- Rugged Gate Oxide Technology
- Lower Input Capacitance
- Improved Gate Charge
- Extended Safe Operating Area
- 175°C Operating Temperature
- Lower Leakage Current : 10  $\mu$ A (Max.) @  $V_{DS} = 100V$
- Lower  $R_{DS(ON)}$  : 0.032  $\Omega$ (Typ.)

$$BV_{DSS} = 100 V$$

$$R_{DS(on)} = 0.04 \Omega$$

$$I_D = 40 A$$

**D<sup>2</sup>-PAK**    **I<sup>2</sup>-PAK**



1. Gate 2. Drain 3. Source

## Absolute Maximum Ratings

Symbol	Characteristic	Value	Units
$V_{DSS}$	Drain-to-Source Voltage	100	V
$I_D$	Continuous Drain Current ( $T_C=25^\circ C$ )	40	A
	Continuous Drain Current ( $T_C=100^\circ C$ )	28.3	
$I_{DM}$	Drain Current-Pulsed ①	160	A
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$E_{AS}$	Single Pulsed Avalanche Energy ②	640	mJ
$I_{AR}$	Avalanche Current ①	40	A
$E_{AR}$	Repetitive Avalanche Energy ①	16.7	mJ
dv/dt	Peak Diode Recovery dv/dt ③	6.5	V/ns
$P_D$	Total Power Dissipation ( $T_A=25^\circ C$ ) *	3.8	W
	Total Power Dissipation ( $T_C=25^\circ C$ )	167	W
	Linear Derating Factor	1.11	W/ $^\circ C$
$T_J, T_{STG}$	Operating Junction and Storage Temperature Range	- 55 to +175	$^\circ C$
$T_L$	Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5-seconds	300	

## Thermal Resistance

Symbol	Characteristic	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	--	0.9	$^\circ C/W$
$R_{\theta JA}$	Junction-to-Ambient *	--	40	
$R_{\theta JA}$	Junction-to-Ambient	--	62.5	

\* When mounted on the minimum pad size recommended (PCB Mount).

### Electrical Characteristics ( $T_C=25^\circ\text{C}$ unless otherwise specified)

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
$BV_{DSS}$	Drain-Source Breakdown Voltage	100	--	--	V	$V_{GS}=0V, I_D=250\mu\text{A}$
$\Delta BV/\Delta T_J$	Breakdown Voltage Temp. Coeff.	--	0.11	--	V/ $^\circ\text{C}$	$I_D=250\mu\text{A}$ <b>See Fig 7</b>
$V_{GS(th)}$	Gate Threshold Voltage	2.0	--	4.0	V	$V_{DS}=5V, I_D=250\mu\text{A}$
$I_{GSS}$	Gate-Source Leakage, Forward	--	--	100	nA	$V_{GS}=20V$
	Gate-Source Leakage, Reverse	--	--	-100		$V_{GS}=-20V$
$I_{DSS}$	Drain-to-Source Leakage Current	--	--	10	$\mu\text{A}$	$V_{DS}=100V$
		--	--	100		$V_{DS}=80V, T_C=150^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-State Resistance	--	--	0.04	$\Omega$	$V_{GS}=10V, I_D=20A$ ④
$g_{fs}$	Forward Transconductance	--	27.44	--	$\Omega$	$V_{DS}=40V, I_D=20A$ ④
$C_{iss}$	Input Capacitance	--	1750	2270	pF	$V_{GS}=0V, V_{DS}=25V, f=1\text{MHz}$ <b>See Fig 5</b>
$C_{oss}$	Output Capacitance	--	420	485		
$C_{rss}$	Reverse Transfer Capacitance	--	185	215		
$t_{d(on)}$	Turn-On Delay Time	--	17	50	ns	$V_{DD}=50V, I_D=40A,$ $R_G=6.2\Omega$ <b>See Fig 13</b> ④⑤
$t_r$	Rise Time	--	20	50		
$t_{d(off)}$	Turn-Off Delay Time	--	80	160		
$t_f$	Fall Time	--	45	100		
$Q_g$	Total Gate Charge	--	75	97	nC	$V_{DS}=80V, V_{GS}=10V,$ $I_D=40A$ <b>See Fig 6 &amp; Fig 12</b> ④⑤
$Q_{gs}$	Gate-Source Charge	--	13.2	--		
$Q_{gd}$	Gate-Drain("Miller") Charge	--	34.8	--		

### Source-Drain Diode Ratings and Characteristics

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
$I_S$	Continuous Source Current	--	--	40	A	Integral reverse pn-diode in the MOSFET
$I_{SM}$	Pulsed-Source Current ①	--	--	160		
$V_{SD}$	Diode Forward Voltage ④	--	--	1.6	V	$T_J=25^\circ\text{C}, I_S=40A, V_{GS}=0V$
$t_{rr}$	Reverse Recovery Time	--	135	--	ns	$T_J=25^\circ\text{C}, I_F=40A$
$Q_{rr}$	Reverse Recovery Charge	--	0.65	--	$\mu\text{C}$	$di_F/dt=100A/\mu\text{s}$ ④

#### Notes ;

- ① Repetitive Rating : Pulse Width Limited by Maximum Junction Temperature
- ②  $L=0.6\text{mH}, I_{AS}=40A, V_{DD}=25V, R_G=27\Omega$ , Starting  $T_J=25^\circ\text{C}$
- ③  $I_{SD} \leq 40A, di/dt \leq 470A/\mu\text{s}, V_{DD} \leq BV_{DSS}$ , Starting  $T_J=25^\circ\text{C}$
- ④ Pulse Test : Pulse Width = 250  $\mu\text{s}$ , Duty Cycle  $\leq 2\%$
- ⑤ Essentially Independent of Operating Temperature

Fig 1. Output Characteristics

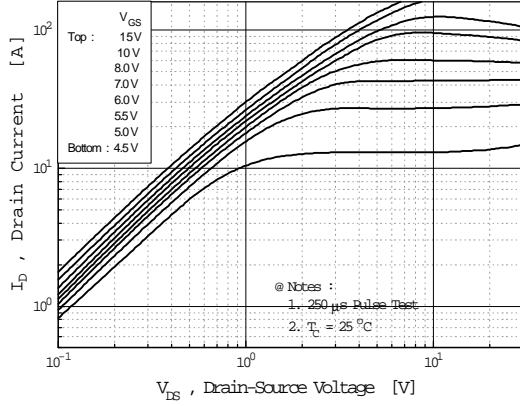


Fig 2. Transfer Characteristics

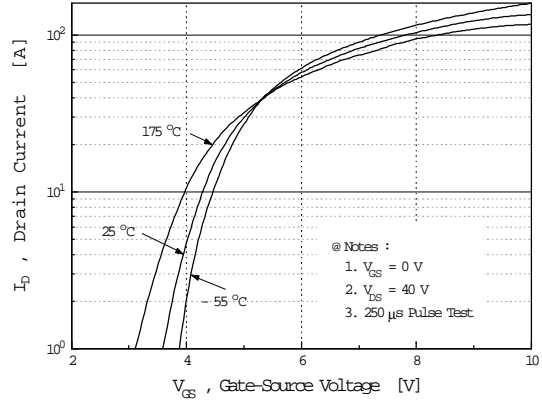


Fig 3. On-Resistance vs. Drain Current

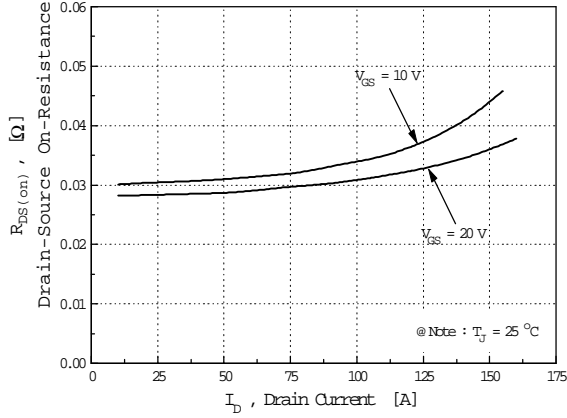


Fig 4. Source-Drain Diode Forward Voltage

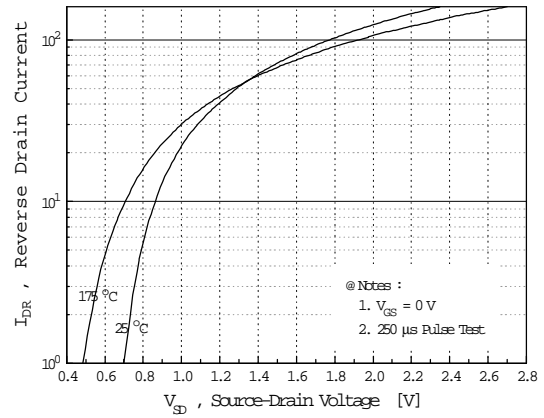


Fig 5. Capacitance vs. Drain-Source Voltage

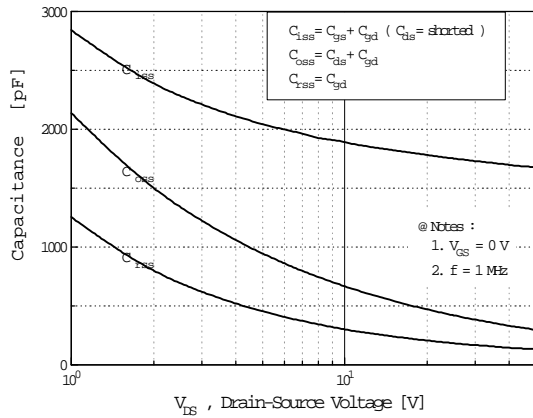
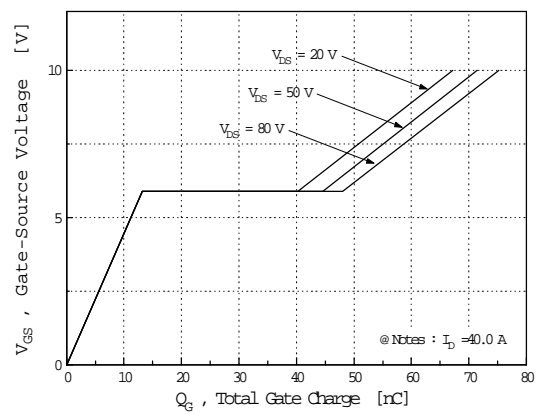


Fig 6. Gate Charge vs. Gate-Source Voltage



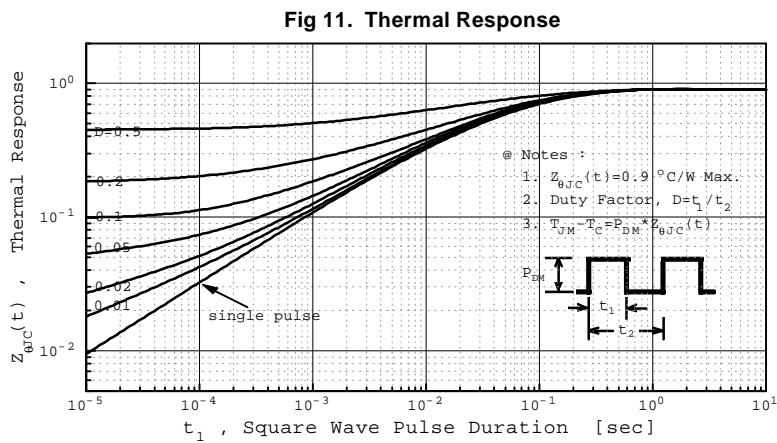
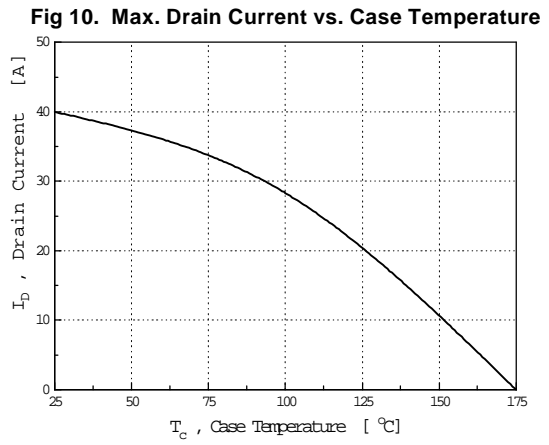
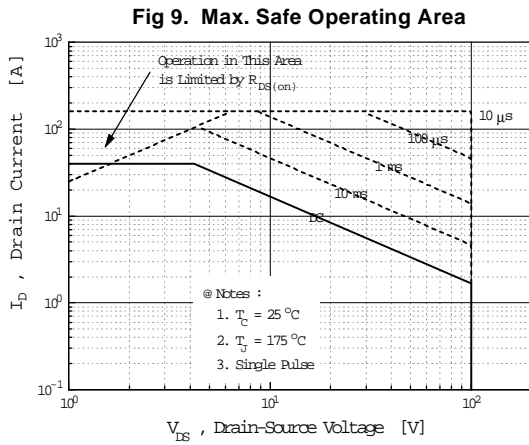
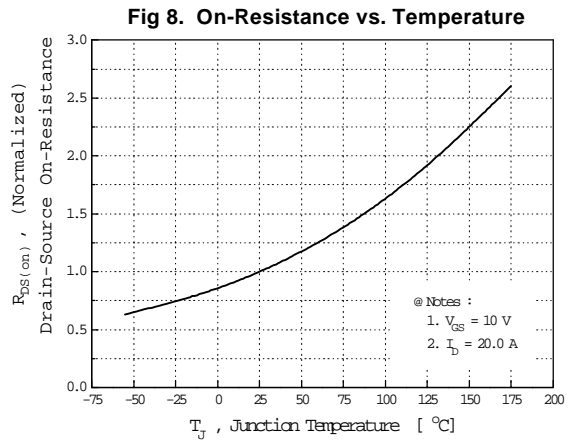
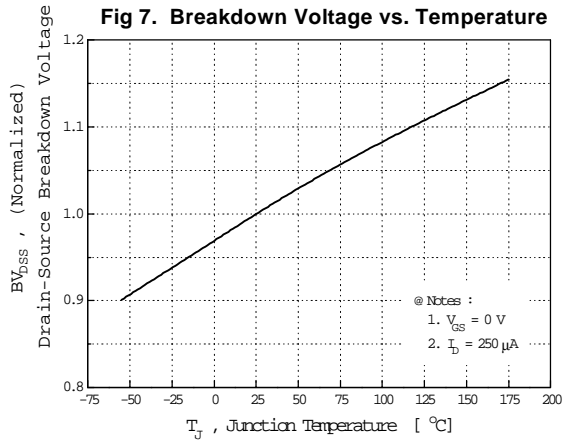


Fig 12. Gate Charge Test Circuit & Waveform

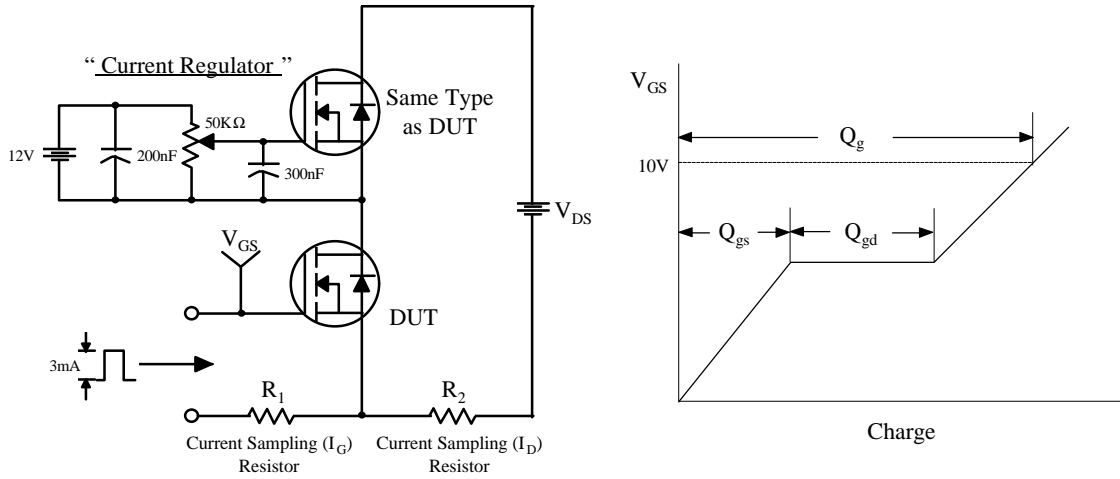


Fig 13. Resistive Switching Test Circuit & Waveforms

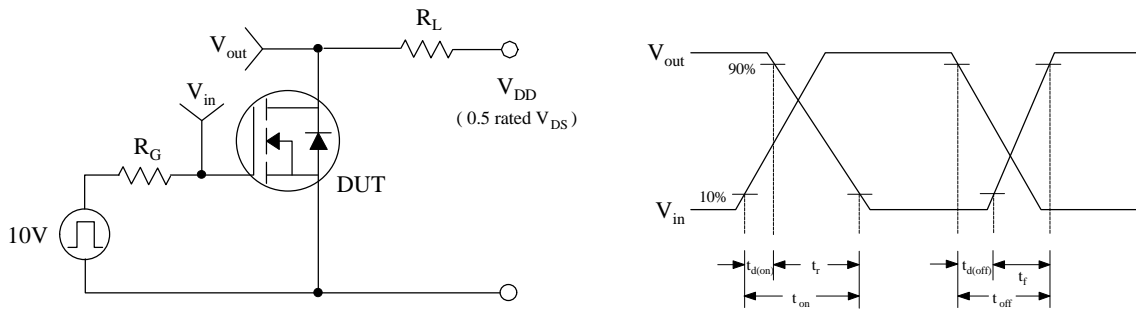


Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms

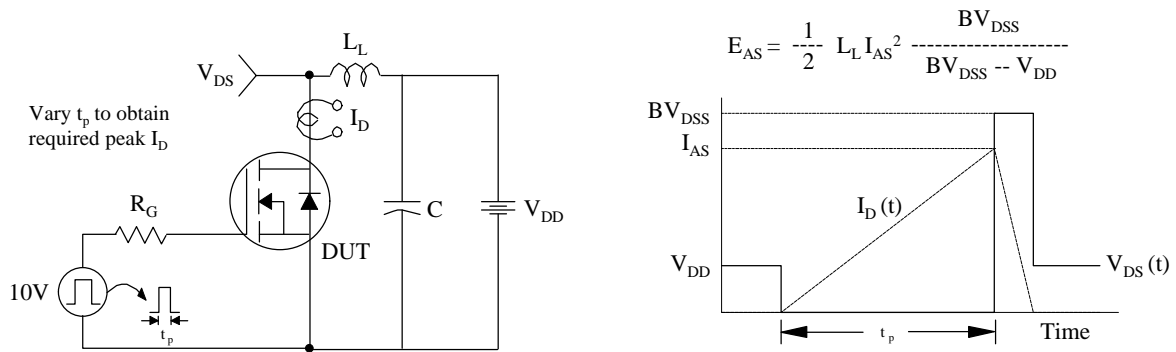
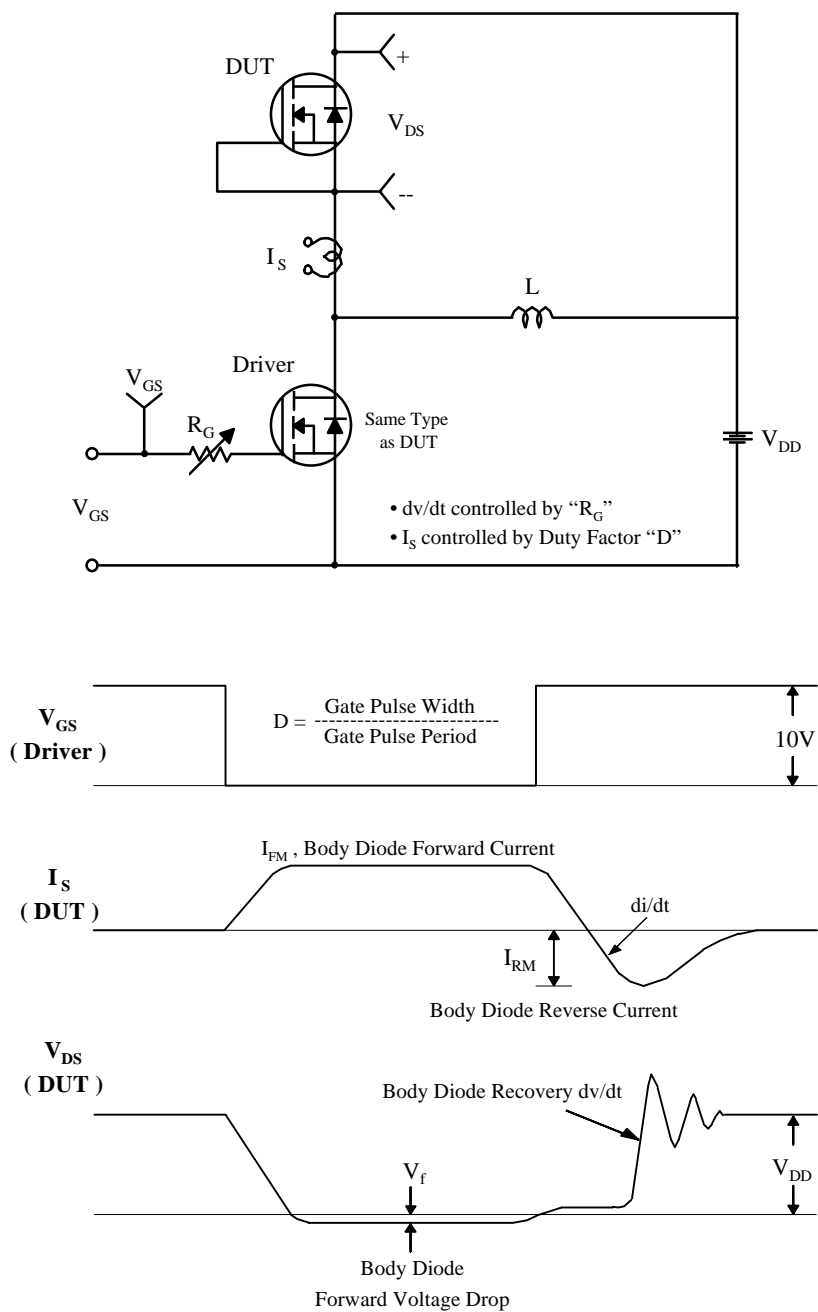


Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms



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