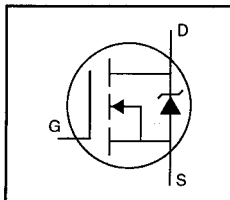


HEXFET® Power MOSFET

- Ultra Low Gate Charge
- Reduced Gate Drive Requirement
- Enhanced 30V V_{GS} Rating
- Isolated Package
- High Voltage Isolation= 2.5KV RMS ⑤
- Sink to Lead Creepage Dist.= 4.8mm
- Repetitive Avalanche Rated



$$V_{DSS} = 400V$$

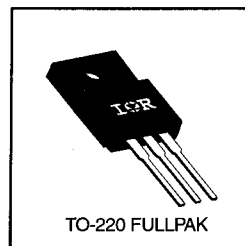
$$R_{DS(on)} = 0.55\Omega$$

$$I_D = 5.7A$$

Description

This new series of Low Charge HEXFETs achieve significantly lower gate charge over conventional MOSFETs. Utilizing advanced HEXFET technology, the device improvements allow for reduced gate drive requirements, faster switching speeds and increased total system savings. These device improvements combined with the proven ruggedness and reliability that are characteristic of HEXFETs offer the designer a new standard in power transistors for switching applications.

The TO-220 Fullpak eliminates the need for additional insulating hardware. The moulding compound used provides a high isolation capability and low thermal resistance between the tab and external heatsink.



Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10 V$	5.7	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10 V$	3.6	
I_{DM}	Pulsed Drain Current ①	23	
$P_D @ T_C = 25^\circ C$	Power Dissipation	40	W
	Linear Derating Factor	0.32	W/°C
V_{GS}	Gate-to-Source Voltage	± 30	V
E_{AS}	Single Pulse Avalanche Energy ②	310	mJ
I_{AR}	Avalanche Current ①	5.7	A
E_{AR}	Repetitive Avalanche Energy ①	4.0	mJ
dv/dt	Peak Diode Recovery dv/dt ③	4.0	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting Torque, 6-32 or M3 screw	10 lbf·in (1.1 N·m)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	3.1	°C/W
$R_{\theta JA}$	Junction-to-Ambient	—	—	65	

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	400	—	—	V	V _{GS} =0V, I _D =250μA
ΔV _{(BR)DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	0.76	—	V/°C	Reference to 25°C, I _D =1mA
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	—	0.55	Ω	V _{GS} =10V, I _D =3.4A ④
V _{GS(th)}	Gate Threshold Voltage	2.0	—	4.0	V	V _{DS} =V _{GS} , I _D =250μA
g _{fs}	Forward Transconductance	3.0	—	—	S	V _{DS} =50V, I _D =6.0A ④
I _{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	V _{DS} =400V, V _{GS} =0V
		—	—	250		V _{DS} =320V, V _{GS} =0V, T _J =125°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V _{GS} =20V
	Gate-to-Source Reverse Leakage	—	—	-100		V _{GS} =-20V
Q _g	Total Gate Charge	—	—	39	nC	I _D =10A
Q _{gs}	Gate-to-Source Charge	—	—	10		V _{DS} =320V
Q _{gd}	Gate-to-Drain ("Miller") Charge	—	—	19		V _{GS} =10V See Fig. 6 and 13 ④
t _{d(on)}	Turn-On Delay Time	—	11	—	ns	V _{DD} =200V
t _r	Rise Time	—	31	—		I _D =10A
t _{d(off)}	Turn-Off Delay Time	—	25	—		R _G =9.1Ω
t _f	Fall Time	—	20	—		R _D =20Ω See Figure 10 ④
L _D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6 mm (0.25in.) from package and center of die contact
L _S	Internal Source Inductance	—	7.5	—		
C _{iss}	Input Capacitance	—	1100	—	pF	V _{GS} =0V
C _{oss}	Output Capacitance	—	190	—		V _{DS} =25V
C _{rss}	Reverse Transfer Capacitance	—	18	—		f=1.0MHz See Figure 5
C	Drain to Sink Capacitance	—	12	—		f=1.0MHz

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I _S	Continuous Source Current (Body Diode)	—	—	5.7	A	MOSFET symbol showing the integral reverse p-n junction diode.
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	23		
V _{SD}	Diode Forward Voltage	—	—	2.0	V	T _J =25°C, I _S =5.7A, V _{GS} =0V ④
t _{rr}	Reverse Recovery Time	—	380	570	ns	T _J =25°C, I _F =10A
Q _{rr}	Reverse Recovery Charge	—	2.8	4.2	μC	di/dt=100A/μs ④
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature (See Figure 11)

③ I_{SD}≤10A, di/dt≤120A/μs, V_{DD}≤V_{(BR)DSS}, T_J≤150°C

⑤ t=60s, f=60Hz

② V_{DD}=50V, starting T_J=25°C, L=16mH
R_G=25Ω, I_{AS}=5.7A (See Figure 12)

④ Pulse width ≤ 300 μs; duty cycle ≤2%.

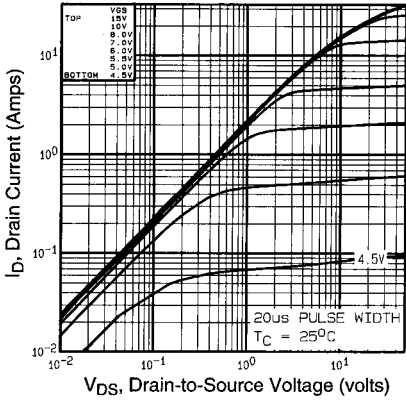


Fig 1. Typical Output Characteristics,
 $T_C=25^\circ\text{C}$

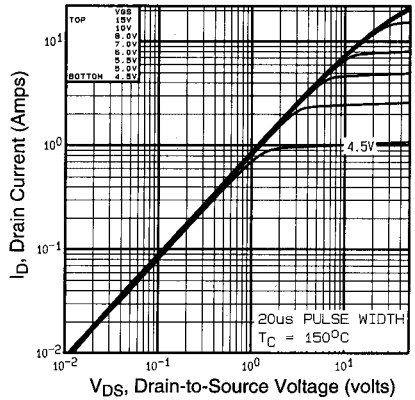


Fig 2. Typical Output Characteristics,
 $T_C=150^\circ\text{C}$

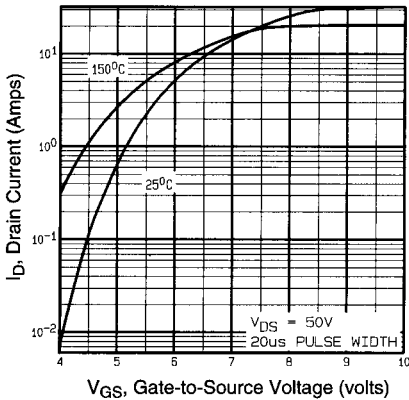


Fig 3. Typical Transfer Characteristics

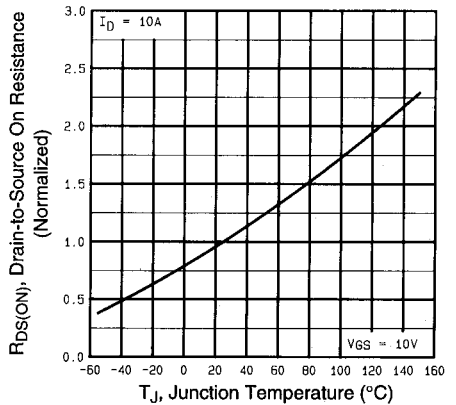


Fig 4. Normalized On-Resistance
Vs. Temperature

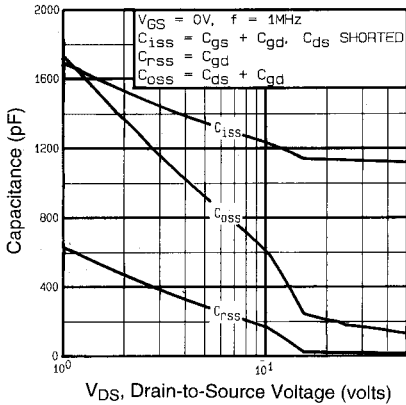


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

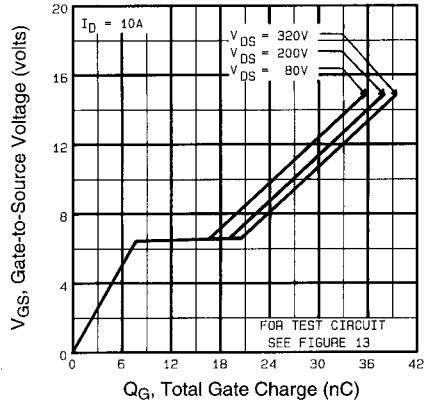


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

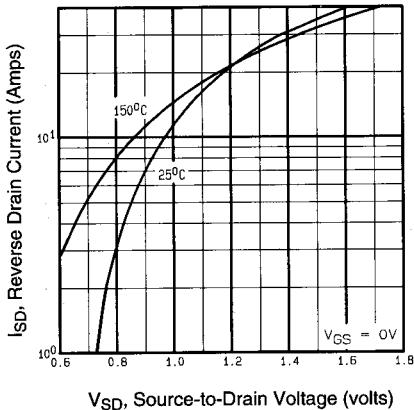


Fig 7. Typical Source-Drain Diode Forward Voltage

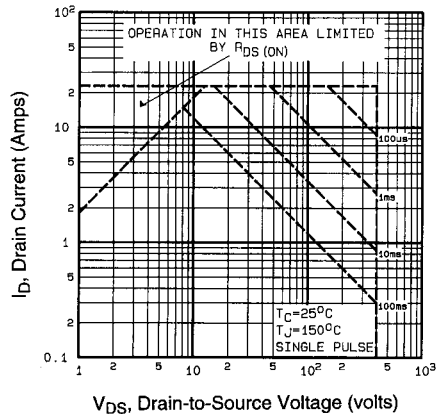


Fig 8. Maximum Safe Operating Area

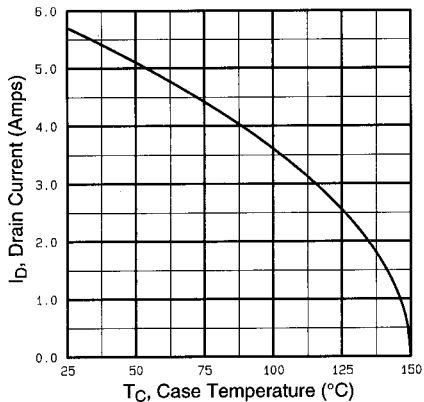


Fig 9. Maximum Drain Current Vs. Case Temperature

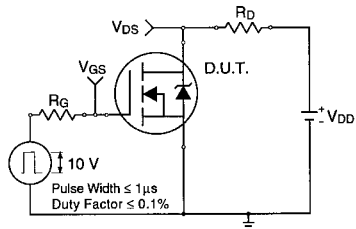


Fig 10a. Switching Time Test Circuit

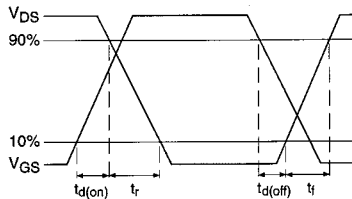


Fig 10b. Switching Time Waveforms

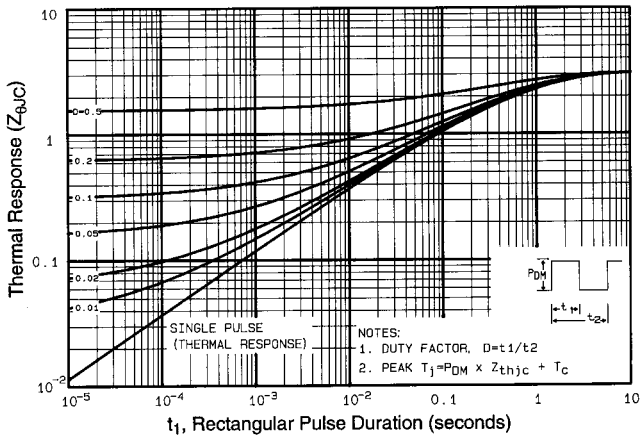


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

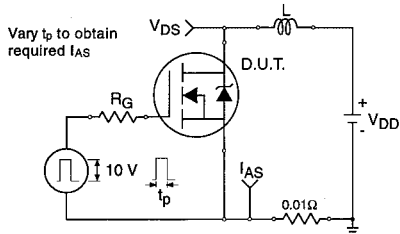


Fig 12a. Unclamped Inductive Test Circuit

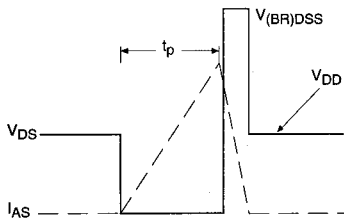


Fig 12b. Unclamped Inductive Waveforms

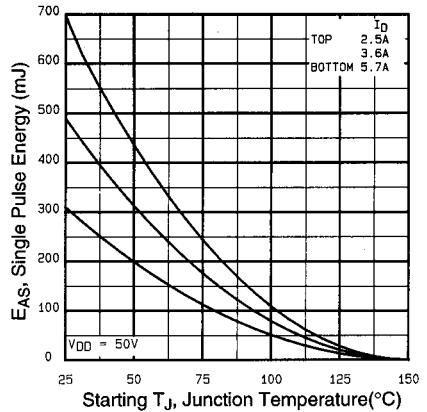


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

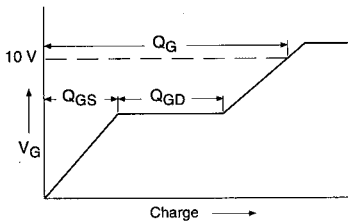


Fig 13a. Basic Gate Charge Waveform

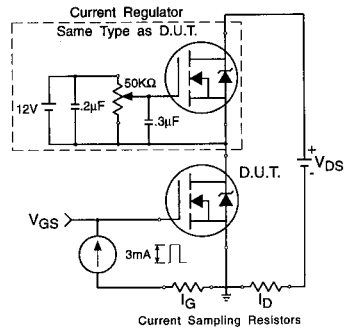
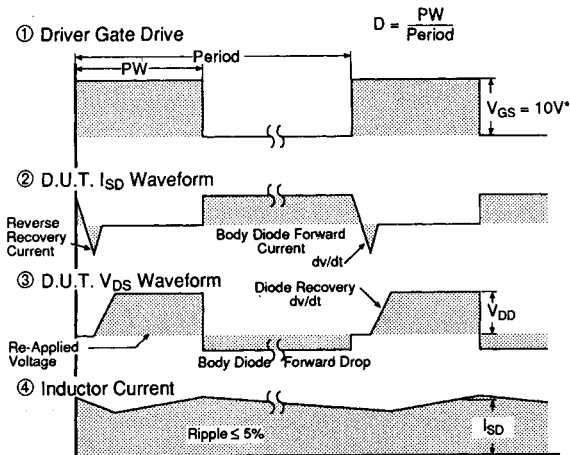
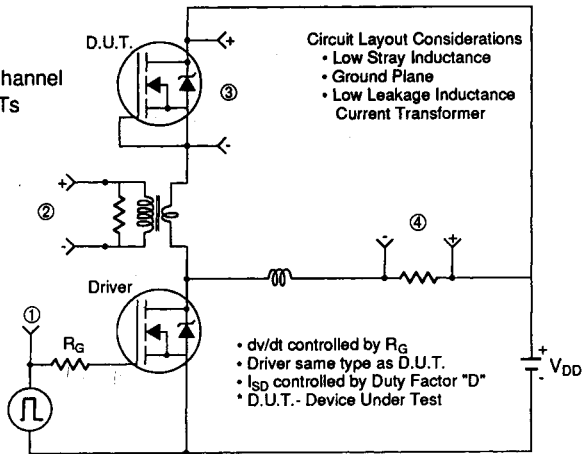


Fig 13b. Gate Charge Test Circuit

Appendix A

Peak Diode Recovery dv/dt Test Circuit

Fig 14. For N-Channel HEXFETs

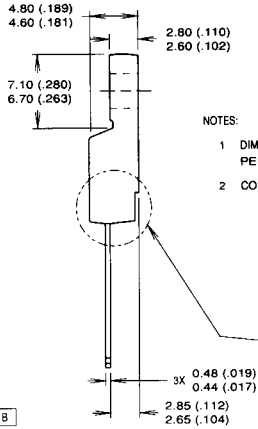
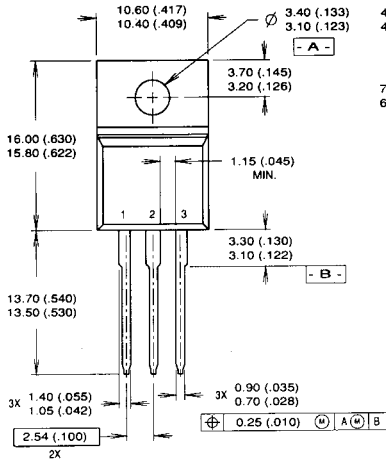


* $V_{GS} = 5V$ for Logic Level Devices

Package Outline

TO-220 FullPak Outline

Dimensions are shown in millimeters (inches)



LEAD ASSIGNMENTS

- 1 - GATE
- 2 - DRAIN
- 3 - SOURCE

NOTES:

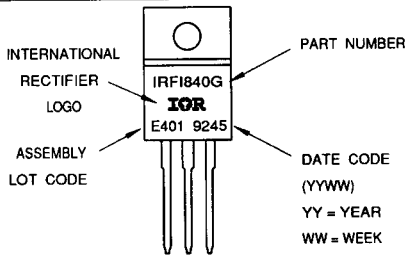
- 1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
- 2 CONTROLLING DIMENSION : INCH.

MINIMUM CREEPAGE DISTANCE BETWEEN A-B-C-D = 4.80 (.189)

Part Marking Information

TO-220 FULL-PAK

EXAMPLE: THIS IS AN IRFI840G WITH ASSEMBLY LOT CODE E401



Appendix C



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