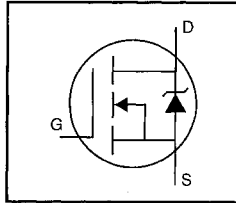


### HEXFET® Power MOSFET

- Isolated Package
- High Voltage Isolation= 2.5KV RMS ⑤
- Sink to Lead Creepage Dist.= 4.8mm
- Dynamic dv/dt Rating
- Low Thermal Resistance



$$V_{DSS} = 500V$$

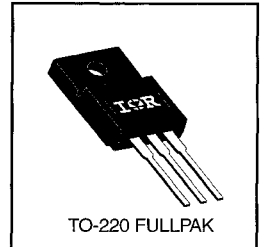
$$R_{DS(on)} = 3.0\Omega$$

$$I_D = 2.1A$$

### Description

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220 Fullpak eliminates the need for additional insulating hardware in commercial-industrial applications. The moulding compound used provides a high isolation capability and a low thermal resistance between the tab and external heatsink. This isolation is equivalent to using a 100 micron mica barrier with standard TO-220 product. The Fullpak is mounted to a heatsink using a single clip or by a single screw fixing.



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### Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D$ @ $T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{ V}$	2.1	A
$I_D$ @ $T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{ V}$	1.3	
$I_{DM}$	Pulsed Drain Current ①	8.4	
$P_D$ @ $T_C = 25^\circ\text{C}$	Power Dissipation	30	W
	Linear Derating Factor	0.24	
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$E_{AS}$	Single Pulse Avalanche Energy ②	110	mJ
$I_{AR}$	Avalanche Current ①	2.1	A
$E_{AR}$	Repetitive Avalanche Energy ①	3.0	mJ
dv/dt	Peak Diode Recovery dv/dt ③	3.5	V/ns
$T_J$	Operating Junction and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
$T_{STG}$	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting Torque, 6-32 or M3 screw	10 lbf•in (1.1 N•m)	

### Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	4.1	$^\circ\text{C/W}$
$R_{\theta JA}$	Junction-to-Ambient	—	—	65	

**Electrical Characteristics @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)**

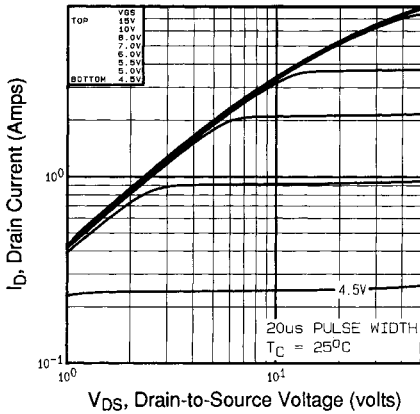
	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	500	—	—	V	$V_{GS}=0V, I_D=250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.59	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D=1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	3.0	$\Omega$	$V_{GS}=10V, I_D=1.3A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS}=V_{GS}, I_D=250\mu A$
$g_{fs}$	Forward Transconductance	1.5	—	—	S	$V_{DS}=50V, I_D=1.3A$ ④
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	25	$\mu A$	$V_{DS}=500V, V_{GS}=0V$
		—	—	250		$V_{DS}=400V, V_{GS}=0V, T_J=125^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS}=20V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS}=-20V$
$Q_g$	Total Gate Charge	—	—	24	nC	$I_D=2.1A$
$Q_{gs}$	Gate-to-Source Charge	—	—	3.3		$V_{DS}=400V$
$Q_{gd}$	Gate-to-Drain ("Miller") Charge	—	—	13		$V_{GS}=10V$ See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	—	8.0	—	ns	$V_{DD}=250V$
$t_r$	Rise Time	—	8.6	—		$I_D=2.1A$
$t_{d(off)}$	Turn-Off Delay Time	—	33	—		$R_G=18\Omega$
$t_f$	Fall Time	—	16	—		$R_D=120\Omega$ See Figure 10 ④
$L_D$	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6 mm (0.25in.) from package and center of die contact
$L_S$	Internal Source Inductance	—	7.5	—		
$C_{iss}$	Input Capacitance	—	360	—	pF	$V_{GS}=0V$
$C_{oss}$	Output Capacitance	—	92	—		$V_{DS}=25V$
$C_{rss}$	Reverse Transfer Capacitance	—	37	—		$f=1.0\text{MHz}$ See Figure 5
C	Drain to Sink Capacitance	—	12	—		$f=1.0\text{MHz}$


**Source-Drain Ratings and Characteristics**

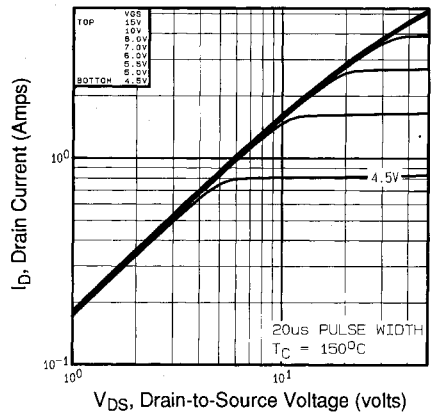
	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	2.1	A	MOSFET symbol showing the integral reverse p-n junction diode.
$I_{SM}$	Pulsed Source Current (Body Diode) ①	—	—	8.0		
$V_{SD}$	Diode Forward Voltage	—	—	1.6	V	$T_J=25^\circ\text{C}, I_S=2.1A, V_{GS}=0V$ ④
$t_{rr}$	Reverse Recovery Time	—	260	520	ns	$T_J=25^\circ\text{C}, I_F=2.1A$
$Q_{rr}$	Reverse Recovery Charge	—	0.70	1.4	$\mu\text{C}$	$di/dt=100A/\mu\text{s}$ ④
$t_{on}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S+L_D$ )				

**Notes:**

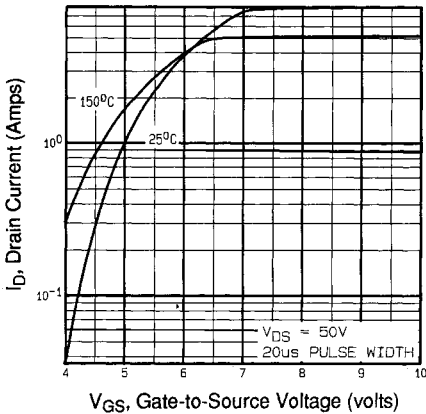
- ① Repetitive rating; pulse width limited by max. junction temperature (See Figure 11)
- ②  $V_{DD}=50V$ , starting  $T_J=25^\circ\text{C}$ ,  $L=44\text{mH}$ ,  $R_G=25\Omega$ ,  $I_{AS}=2.1A$  (See Figure 12)
- ③  $I_{SD}\leq 2.1A$ ,  $di/dt\leq 50A/\mu\text{s}$ ,  $V_{DD}\leq V_{(BR)DSS}$ ,  $T_J\leq 150^\circ\text{C}$
- ④ Pulse width  $\leq 300\mu\text{s}$ ; duty cycle  $\leq 2\%$
- ⑤  $t=60\text{s}$ ,  $f=60\text{Hz}$



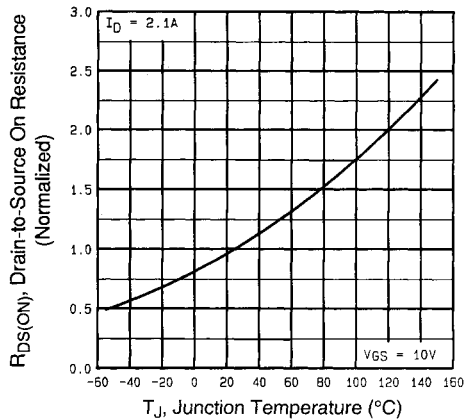
**Fig 1.** Typical Output Characteristics,  $T_C=25^\circ\text{C}$



**Fig 2.** Typical Output Characteristics,  $T_C=150^\circ\text{C}$

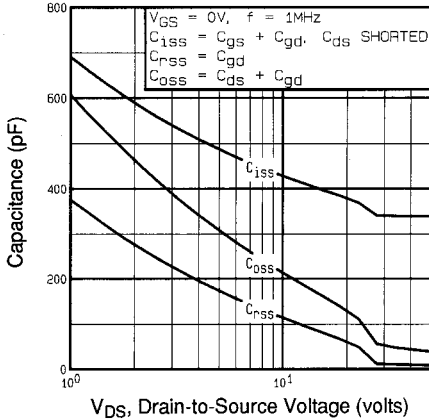


**Fig 3.** Typical Transfer Characteristics

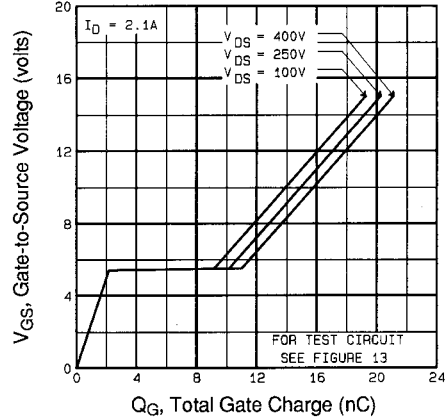


**Fig 4.** Normalized On-Resistance Vs. Temperature

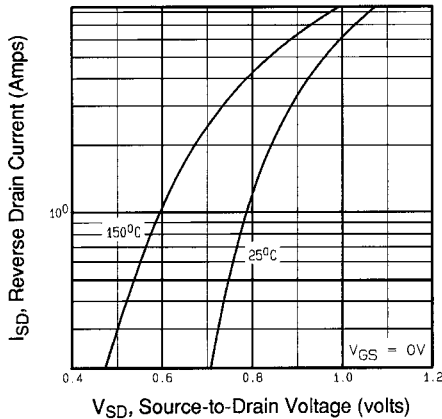
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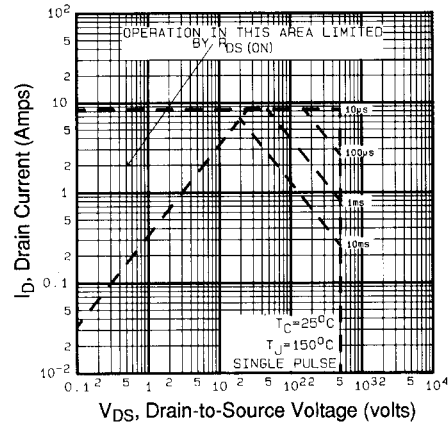
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



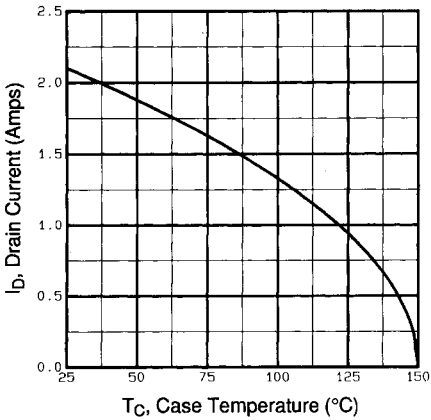
**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



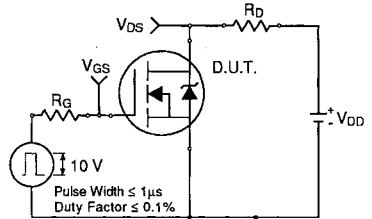
**Fig 7.** Typical Source-Drain Diode Forward Voltage



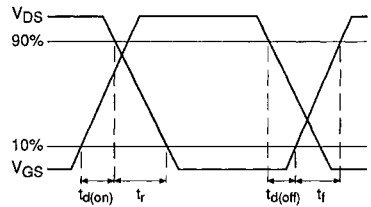
**Fig 8.** Maximum Safe Operating Area



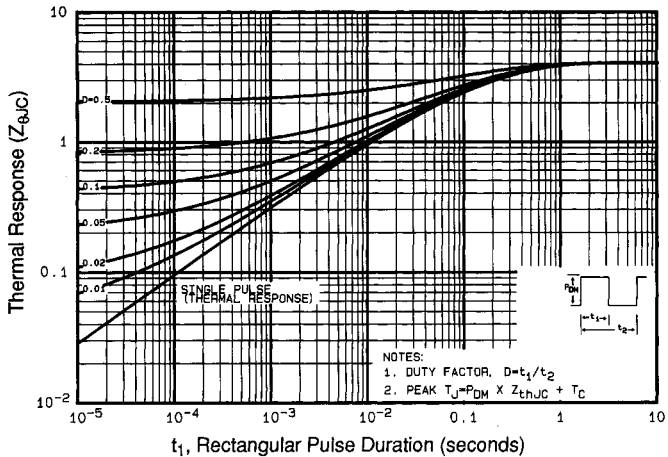
**Fig 9.** Maximum Drain Current Vs. Case Temperature



**Fig 10a.** Switching Time Test Circuit

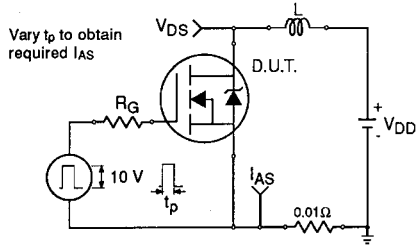


**Fig 10b.** Switching Time Waveforms

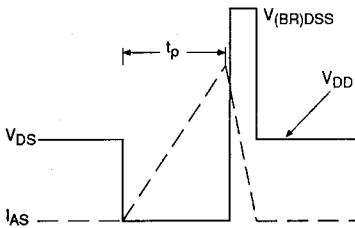


**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

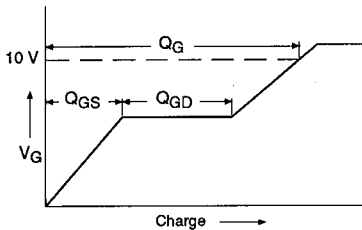
DATA SHEETS



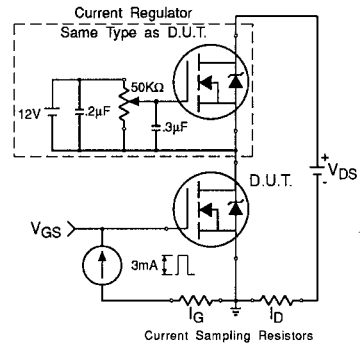
**Fig 12a.** Unclamped Inductive Test Circuit



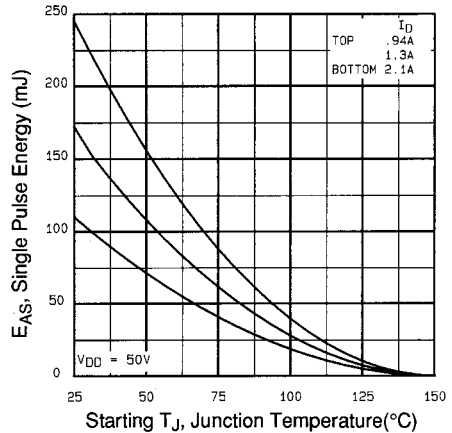
**Fig 12b.** Unclamped Inductive Waveforms



**Fig 13a.** Basic Gate Charge Waveform



**Fig 13b.** Gate Charge Test Circuit



**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current

**Appendix A:** Figure 14, Peak Diode Recovery  $dv/dt$  Test Circuit – See page 1505

**Appendix B:** Package Outline Mechanical Drawing – See page 1510

**Appendix C:** Part Marking Information – See page 1517



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