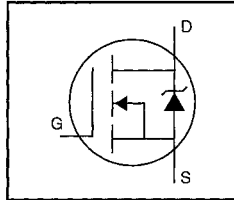


### HEXFET® Power MOSFET

- Isolated Package
- High Voltage Isolation= 2.5KV RMS @
- Sink to Lead Creepage Dist.= 4.8mm
- 175°C Operating Temperature
- Dynamic dv/dt Rating
- Low Thermal Resistance



$$V_{DSS} = 60V$$

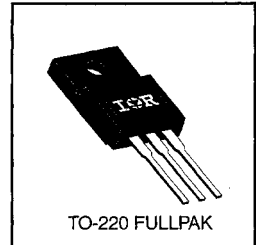
$$R_{DS(on)} = 0.20\Omega$$

$$I_D = 8.0A$$

### Description

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220 Fullpak eliminates the need for additional insulating hardware in commercial-industrial applications. The moulding compound used provides a high isolation capability and a low thermal resistance between the tab and external heatsink. This isolation is equivalent to using a 100 micron mica barrier with standard TO-220 product. The Fullpak is mounted to a heatsink using a single clip or by a single screw fixing.



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### Absolute Maximum Ratings

|                           | Parameter                                 | Max.                | Units |
|---------------------------|---|---------------------|-------|
| $I_D @ T_C = 25^\circ C$  | Continuous Drain Current, $V_{GS} @ 10 V$ | 8.0                 | A     |
| $I_D @ T_C = 100^\circ C$ | Continuous Drain Current, $V_{GS} @ 10 V$ | 5.7                 |       |
| $I_{DM}$                  | Pulsed Drain Current ①                    | 32                  |       |
| $P_D @ T_C = 25^\circ C$  | Power Dissipation                         | 27                  | W     |
|                           | Linear Derating Factor                    | 0.18                | W/°C  |
| $V_{GS}$                  | Gate-to-Source Voltage                    | ±20                 | V     |
| $E_{AS}$                  | Single Pulse Avalanche Energy ②           | 47                  | mJ    |
| dv/dt                     | Peak Diode Recovery dv/dt ③               | 4.5                 | V/ns  |
| $T_J$                     | Operating Junction and                    | -55 to +175         | °C    |
| $T_{STG}$                 | Storage Temperature Range                 |                     |       |
|                           | Soldering Temperature, for 10 seconds     |                     |       |
|                           | Mounting Torque, 6-32 or M3 screw         | 10 lbf·in (1.1 N·m) |       |

### Thermal Resistance

|                 | Parameter           | Min. | Typ. | Max. | Units |
|-----------------|---------------------|------|------|------|-------|
| $R_{\theta JC}$ | Junction-to-Case    | —    | —    | 5.5  | °C/W  |
| $R_{\theta JA}$ | Junction-to-Ambient | —    | —    | 65   |       |

## Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

|                                 | Parameter                            | Min. | Typ. | Max. | Units    | Test Conditions   |
|---------------------------------|--------------------------------------|------|------|------|----------|---|
| $V_{(BR)DSS}$                   | Drain-to-Source Breakdown Voltage    | 60   | —    | —    | V        | $V_{GS}=0V, I_D=250\mu A$   |
| $\Delta V_{(BR)DSS}/\Delta T_J$ | Breakdown Voltage Temp. Coefficient  | —    | 0.63 | —    | V/°C     | Reference to $25^\circ\text{C}$ , $I_D=1\text{mA}$                  |
| $R_{DS(on)}$                    | Static Drain-to-Source On-Resistance | —    | —    | 0.20 | $\Omega$ | $V_{GS}=10V, I_D=4.8A$ ④  |
| $V_{GS(th)}$                    | Gate Threshold Voltage               | 2.0  | —    | 4.0  | V        | $V_{DS}=V_{GS}, I_D=250\mu A$                                       |
| $g_{fs}$                        | Forward Transconductance             | 2.2  | —    | —    | S        | $V_{DS}=25V, I_D=4.8A$ ④  |
| $I_{DSS}$                       | Drain-to-Source Leakage Current      | —    | —    | 25   | $\mu A$  | $V_{DS}=60V, V_{GS}=0V$   |
|                                 |                                      | —    | —    | 250  |          | $V_{DS}=48V, V_{GS}=0V, T_J=150^\circ\text{C}$                      |
| $I_{GSS}$                       | Gate-to-Source Forward Leakage       | —    | —    | 100  | nA       | $V_{GS}=20V$  |
|                                 | Gate-to-Source Reverse Leakage       | —    | —    | -100 |          | $V_{GS}=-20V$   |
| $Q_g$                           | Total Gate Charge                    | —    | —    | 11   | nC       | $I_D=10A$   |
| $Q_{gs}$                        | Gate-to-Source Charge                | —    | —    | 3.1  |          | $V_{DS}=48V$  |
| $Q_{gd}$                        | Gate-to-Drain ("Miller") Charge      | —    | —    | 5.8  |          | $V_{GS}=10V$ See Fig. 6 and 13 ④                                    |
| $t_{d(on)}$                     | Turn-On Delay Time                   | —    | 10   | —    | ns       | $V_{DD}=30V$  |
| $t_r$                           | Rise Time                            | —    | 50   | —    |          | $I_D=10A$   |
| $t_{d(off)}$                    | Turn-Off Delay Time                  | —    | 13   | —    |          | $R_G=24\Omega$  |
| $t_f$                           | Fall Time                            | —    | 19   | —    |          | $R_D=2.7\Omega$ See Figure 10 ④                                     |
| $L_D$                           | Internal Drain Inductance            | —    | 4.5  | —    | nH       | Between lead, 6 mm (0.25in.) from package and center of die contact |
| $L_S$                           | Internal Source Inductance           | —    | 7.5  | —    |          |   |
| $C_{iss}$                       | Input Capacitance                    | —    | 300  | —    | pF       | $V_{GS}=0V$   |
| $C_{oss}$                       | Output Capacitance                   | —    | 160  | —    |          | $V_{DS}=25V$  |
| $C_{rss}$                       | Reverse Transfer Capacitance         | —    | 29   | —    |          | $f=1.0\text{MHz}$ See Figure 5                                      |
| C                               | Drain to Sink Capacitance            | —    | 12   | —    |          | $f=1.0\text{MHz}$   |

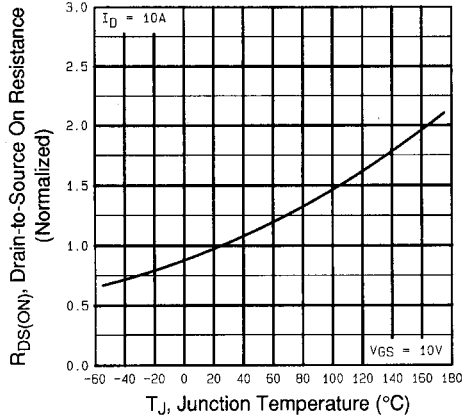
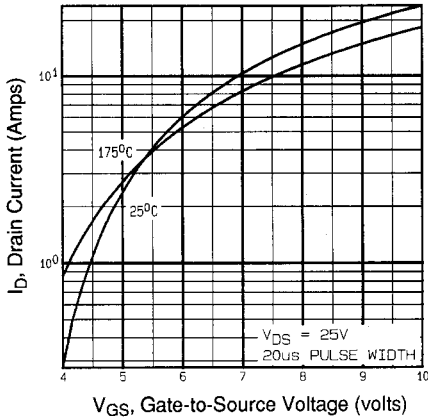
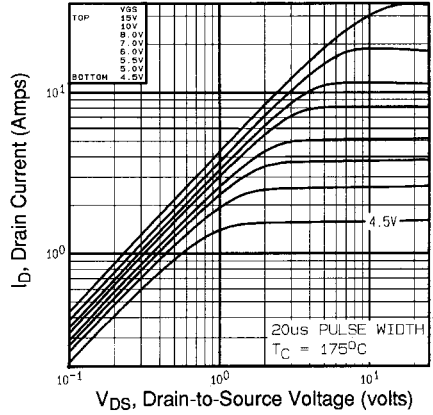
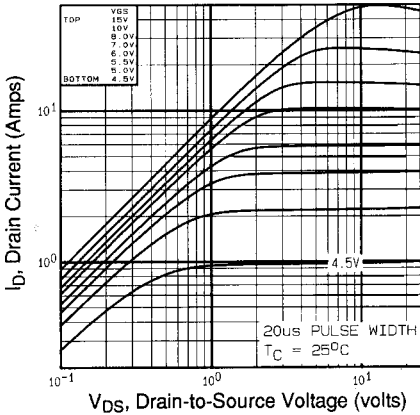


## Source-Drain Ratings and Characteristics

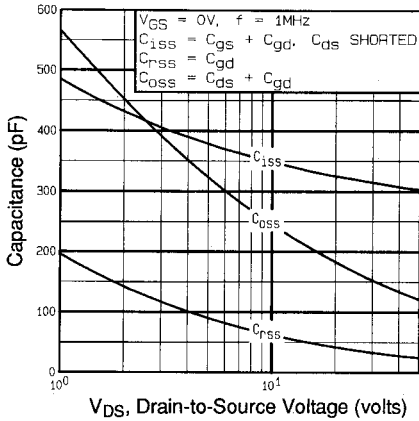
|          | Parameter                              | Min.  | Typ. | Max. | Units   | Test Conditions  |
|----------|--|---|------|------|---------|--|
| $I_S$    | Continuous Source Current (Body Diode) | —   | —    | 8.0  | A       | MOSFET symbol showing the integral reverse p-n junction diode. |
| $I_{SM}$ | Pulsed Source Current (Body Diode) ①   | —   | —    | 32   |         |  |
| $V_{SD}$ | Diode Forward Voltage                  | —   | —    | 1.6  | V       | $T_J=25^\circ\text{C}, I_S=8.0A, V_{GS}=0V$ ④                  |
| $t_{rr}$ | Reverse Recovery Time                  | —   | 70   | 140  | ns      | $T_J=25^\circ\text{C}, I_R=10A$                                |
| $Q_{rr}$ | Reverse Recovery Charge                | —   | 0.20 | 0.40 | $\mu C$ | $di/dt=100A/\mu s$ ④   |
| $t_{on}$ | Forward Turn-On Time                   | Intrinsic turn-on time is negligible (turn-on is dominated by $L_S+L_D$ ) |      |      |         |  |

### Notes:

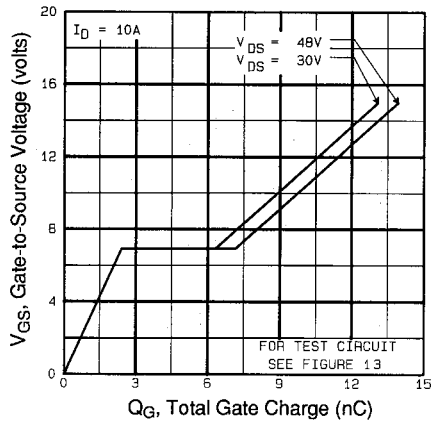
- ① Repetitive rating; pulse width limited by max. junction temperature (See Figure 11)
- ②  $V_{DD}=25V$ , starting  $T_J=25^\circ\text{C}$ ,  $L=856\mu H$ ,  $R_G=25\Omega$ ,  $I_{AS}=8.0A$  (See Figure 12)
- ③  $I_{SD}\leq 10A$ ,  $di/dt\leq 90A/\mu s$ ,  $V_{DD}\leq V_{(BR)DSS}$ ,  $T_J\leq 175^\circ\text{C}$
- ④ Pulse width  $\leq 300\mu s$ ; duty cycle  $\leq 2\%$
- ⑤  $t=60s$ ,  $f=60\text{Hz}$



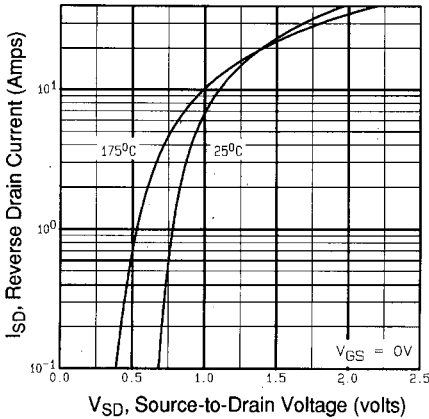
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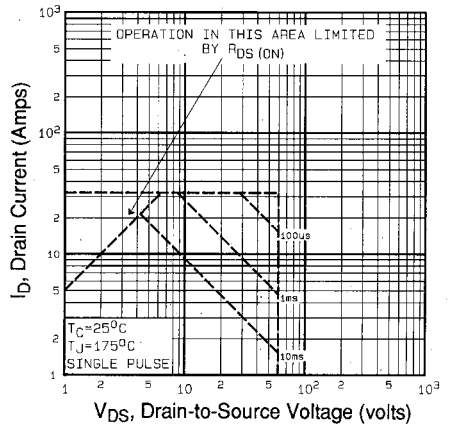
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



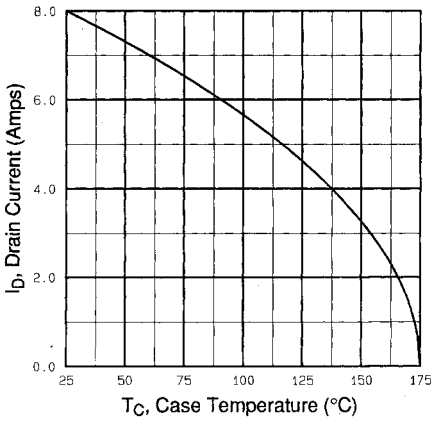
**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



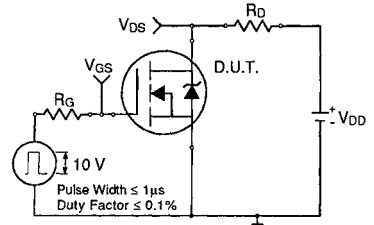
**Fig 7.** Typical Source-Drain Diode Forward Voltage



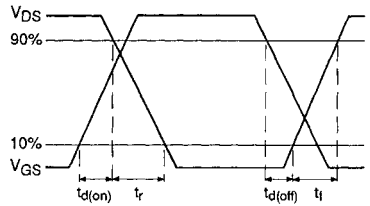
**Fig 8.** Maximum Safe Operating Area



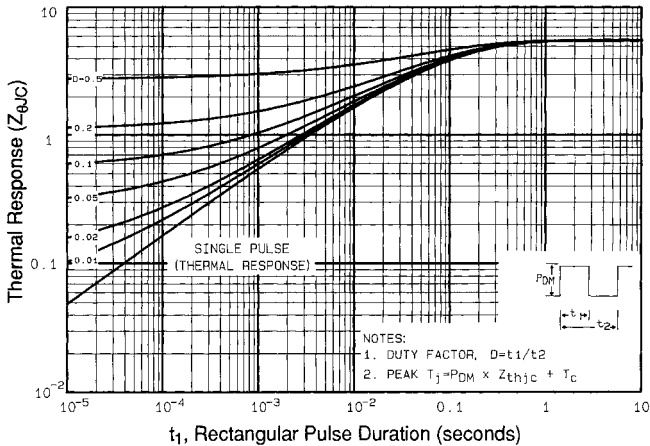
**Fig 9.** Maximum Drain Current Vs. Case Temperature



**Fig 10a.** Switching Time Test Circuit

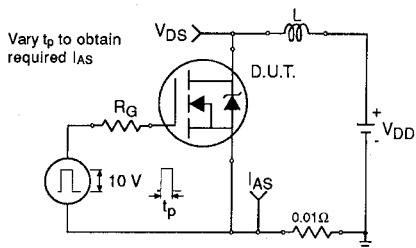


**Fig 10b.** Switching Time Waveforms

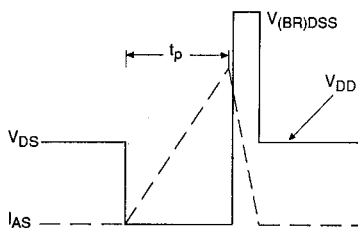


**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

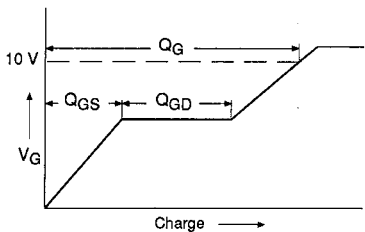
DATA SHEETS



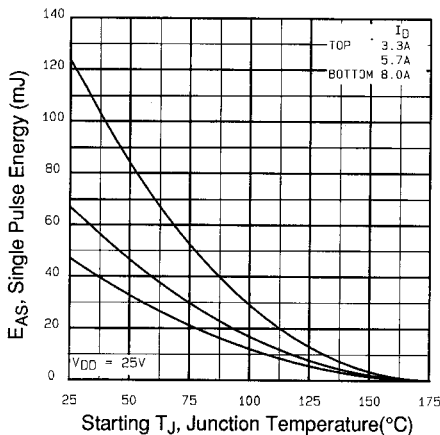
**Fig 12a.** Unclamped Inductive Test Circuit



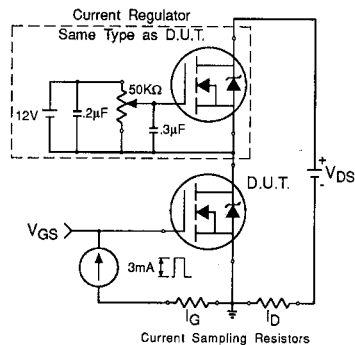
**Fig 12b.** Unclamped Inductive Waveforms



**Fig 13a.** Basic Gate Charge Waveform



**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current



**Fig 13b.** Gate Charge Test Circuit

**Appendix A:** Figure 14, Peak Diode Recovery  $dv/dt$  Test Circuit – See page 1505

**Appendix B:** Package Outline Mechanical Drawing – See page 1510

**Appendix C:** Part Marking Information – See page 1517



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