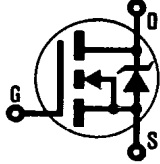




## REPETITIVE AVALANCHE AND $dv/dt$ RATED\*

LOWER ON STATE RESISTANCE, 175°C OPERATING TEMPERATURE

## HEXFET® TRANSISTORS



N-CHANNEL

**IRF510**

**IRF511**

**IRF512**

**IRF513**

### 100 Volt, 0.54 Ohm HEXFET TO-220AB Plastic Package

The HEXFET® technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of this latest "State of the Art" design achieves: very low on-state resistance combined with high transconductance; superior reverse energy and diode recovery  $dv/dt$  capability.

The HEXFET transistors also feature all of the well established advantages of MOSFETs such as voltage control, very fast switching, ease of paralleling and temperature stability of the electrical parameters.

They are well suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers and high energy pulse circuits.

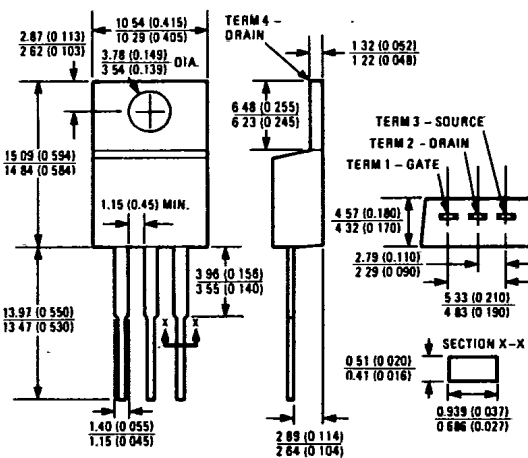
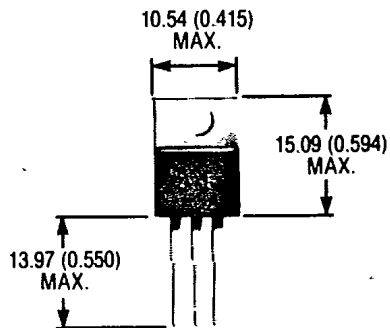
### Product Summary

Part Number	$BV_{DSS}$	$R_{DS(on)}$	$I_D$
IRF510	100V	0.54Ω	5.6A
IRF511	80V	0.54Ω	5.6A
IRF512	100V	0.74Ω	4.9A
IRF513	80V	0.74Ω	4.9A

### FEATURES:

- Repetitive Avalanche Ratings
- Dynamic  $dv/dt$  Rating
- Simple Drive Requirements
- Ease of Paralleling

### CASE STYLE AND DIMENSIONS



Case Style TO-220AB  
Dimensions in Millimeters and (Inches)

\*This data sheet applies to product with batch codes that begin with a digit, ie. 2A3B


C-183

# Absolute Maximum Ratings


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Parameter		IRF510, IRF511	IRF512, IRF513	Units
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current	5.6	4.9	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current	4.0	3.4	A
$I_{DM}$	Pulsed Drain Current <sup>①</sup>	20	18	A
$P_D @ T_C = 25^\circ\text{C}$	Max. Power Dissipation	43		W
	Linear Derating Factor	0.29		W/K <sup>②</sup>
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$		V
$E_{AS}$	Single Pulse Avalanche Energy <sup>②</sup>	19 (See Fig. 14)		mJ
$I_{AR}$	Avalanche Current <sup>①</sup> (Repetitive or Non-Repetitive)	5.6 (See $E_{AR}$ )		A
$E_{AR}$	Repetitive Avalanche Energy <sup>①</sup>	4.3 (See $I_{AR}$ )		mJ
$dv/dt$	Peak Diode Recovery $dv/dt$ <sup>③</sup>	5.5 (See Fig. 17)		V/ns
$T_J$	Operating Junction	-55 to 175		$^\circ\text{C}$
$T_{STG}$	Storage Temperature Range			$^\circ\text{C}$
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)		$^\circ\text{C}$

## Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (Unless Otherwise Specified)

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions	
$BV_{DSS}$	Drain-to-Source Breakdown Voltage	IRF510 IRF512 100	—	—	V	$V_{GS} = 0V, I_D = 250 \mu\text{A}$	
		IRF511 IRF513 80					
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance <sup>④</sup>	IRF510 IRF511 —	0.41	0.54	$\Omega$	$V_{GS} = 10V, I_D = 3.4A$	
		IRF512 IRF513 —	0.54	0.74			
$I_{D(on)}$	On-State Drain Current <sup>④</sup>	IRF510 IRF511 5.6	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ Max. $V_{GS} = 10V$	
		IRF512 IRF513 4.9					
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$
$g_{fs}$	Forward Transconductance <sup>④</sup>	ALL	1.3	2.0	—	S ( $\Omega$ )	$V_{DS} \geq 50V, I_{DS} = 3.4A$
$I_{DSS}$	Zero Gate Voltage Drain Current	ALL	—	—	250 1000	$\mu\text{A}$	$V_{DS} = \text{Max. Rating}, V_{GS} = 0V$ $V_{DS} = 0.8 \times \text{Max. Rating}$ $V_{GS} = 0V, T_J = 150^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Leakage Forward	ALL	—	—	500	nA	$V_{GS} = 20V$
$I_{GSS}$	Gate-to-Source Leakage Reverse	ALL	—	—	-500	nA	$V_{GS} = -20V$
$Q_g$	Total Gate Charge	ALL	—	5.2	7.7	nC	$V_{GS} = 10V, I_D = 5.6A$
$Q_{gs}$	Gate-to-Source Charge	ALL	—	1.5	2.3	nC	$V_{DS} = 0.8 \times \text{Max. Rating}$ See Fig. 16 (Independent of operating temperature)
$Q_{gd}$	Gate-to-Drain ("Miller") Charge	ALL	—	2.2	3.2	nC	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	7.6	11	ns	$V_{DD} = 50V, I_D = 5.6A, R_G = 24\Omega$ $R_D = 9.1\Omega$ See Fig. 15
$t_r$	Rise Time	ALL	—	24	36	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	14	21	ns	
$t_f$	Fall Time	ALL	—	14	21	ns	(Independent of operating temperature)
$L_D$	Internal Drain Inductance	ALL	—	4.5	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die. Modified MOSFET symbol showing the internal inductances. 
$L_S$	Internal Source Inductance	ALL	—	7.5	—	nH	
$C_{iss}$	Input Capacitance	ALL	—	180	—	pF	$V_{GS} = 0V, V_{DS} = 25V$ $f = 1.0 \text{ MHz}$ See Fig. 10
$C_{oss}$	Output Capacitance	ALL	—	82	—	pF	
$C_{rss}$	Reverse Transfer Capacitance	ALL	—	15	—	pF	

Source-Drain Diode Ratings and Characteristics

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
$I_S$ Continuous Source Current (Body Diode)	ALL	—	—	5.6	A	Modified MOSFET symbol showing the integral Reverse p-n junction rectifier. 
$I_{SM}$ Pulsed Source Current (Body Diode) ①	ALL	—	—	20	A	
$V_{SD}$ Diode Forward Voltage ②	ALL	—	—	2.5	V	$T_J = 25^\circ\text{C}$ , $I_S = 5.6\text{A}$ , $V_{GS} = 0\text{V}$
$t_{rr}$ Reverse Recovery Time	ALL	48	96	200	ns	$T_J = 25^\circ\text{C}$ , $I_F = 5.6\text{A}$ , $di/dt = 100\text{A}/\mu\text{s}$
$Q_{RR}$ Reverse Recovery Charge	ALL	0.17	0.38	0.83	$\mu\text{C}$	
$t_{on}$ Forward Turn-On Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$ .				

Thermal Resistance

$R_{thJC}$ Junction-to-Case	ALL	—	—	3.5	K/W ③	
$R_{thCS}$ Case-to-Sink	ALL	—	0.50	—	K/W ③	Mounting surface flat, smooth, and greased
$R_{thJA}$ Junction-to-Ambient	ALL	—	—	80	K/W ③	Typical socket mount

Typical SPICE Computer Model Parameters (For More Information See Application Note An-975)

Device	Level, SPICE MOSFET Model	W ( $\mu\text{m}$ ), Channel Width	L ( $\mu\text{m}$ ), Channel Length	Theta ( $\mu\text{V}$ ), Mobility Modulation	UO ( $\text{CM}^2/\text{V}\cdot\text{S}$ ), Surface Mobility	VTO (V), Threshold Voltage	R1 ( $\Omega$ ), Drain Resistance	R2 ( $\Omega$ ), Source Resistance	RG ( $\Omega$ ), Gate Resistance
All	3	0.142	1.2	0.28	450	3.74	0.17	0.02	3

CGSO (pf), Gate-Source Capacitance	CGD (fF), Gate-Drain Capacitance	E1 (V), Voltage Dependent Voltage Source	LD (nH), Drain Inductance	LS (nH), Source Inductance	LG (nH), Gate Inductance	IS (A), Diode Saturation Current	RS ( $\Omega$ ), Diode Bulk Resistance
840	C1	4 + 0.95 VDG	4.5	7.5	7.5	$1 \times 10^{-13}$	0.045

$C1 = 160\text{ pf} + 6.4 \times 10^{-21} (V_{GE})^{20} - 2.92 \times 10^{-22} (V_{GE})^{22}$

① Repetitive Rating; Pulse width limited by maximum junction temperature (see figure 5) Refer to current HEXFET reliability report

②  $I_{SD} \leq 5.6\text{A}$ ,  $di/dt \leq 75\text{A}/\mu\text{s}$ ,  $V_{DD} \leq BV_{DSS}$ ,  $T_J \leq 175^\circ\text{C}$  Suggested  $R_G = 24\Omega$

③  $K/W = ^\circ\text{C}/\text{W}$   
 $W/K = \text{W}/^\circ\text{C}$

④ @  $V_{DD} = 25\text{V}$ , Starting  $T_J = 25^\circ\text{C}$ ,  $L = 910\ \mu\text{H}$ ,  $R_G = 25\Omega$ , Peak  $I_L = 5.6\text{A}$ .

⑤ Pulse width  $\leq 300\ \mu\text{s}$ ; Duty Cycle  $\leq 2\%$

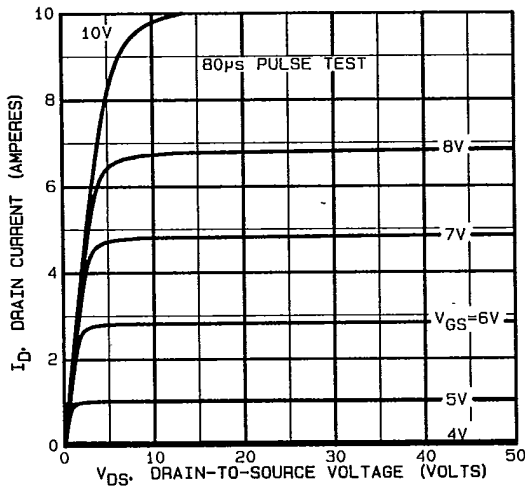


Fig. 1 — Typical Output Characteristics

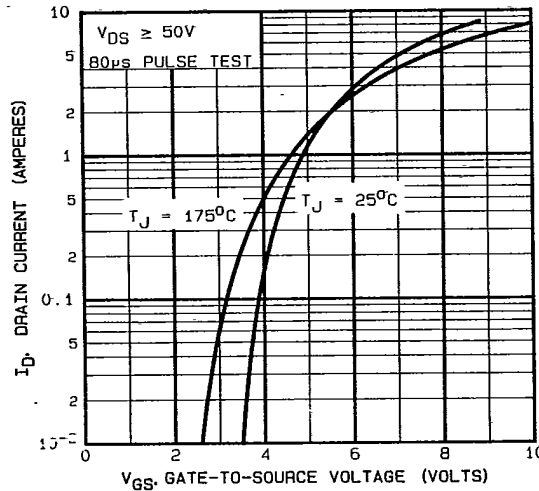


Fig. 2 — Typical Transfer Characteristics

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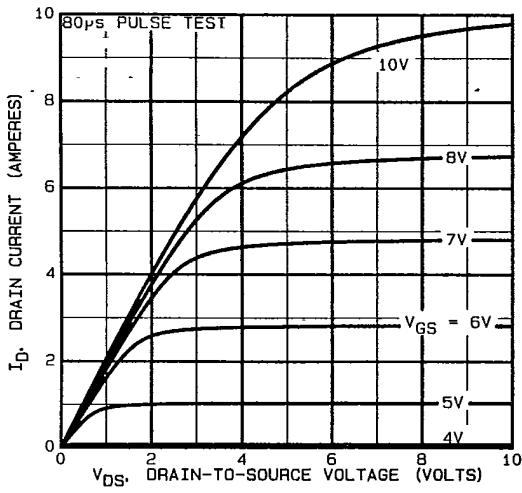


Fig. 3 - Typical Saturation Characteristics

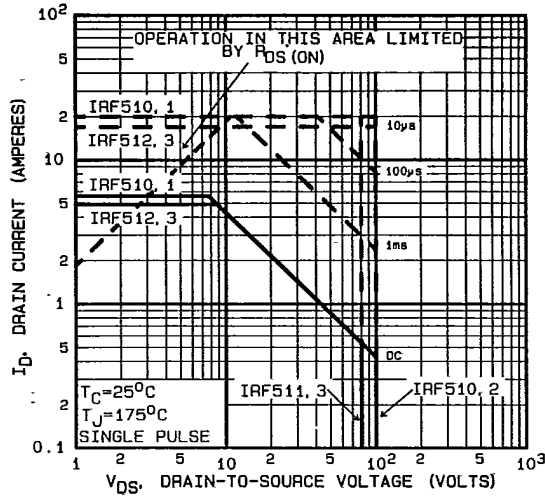


Fig. 4 - Maximum Safe Operating Area

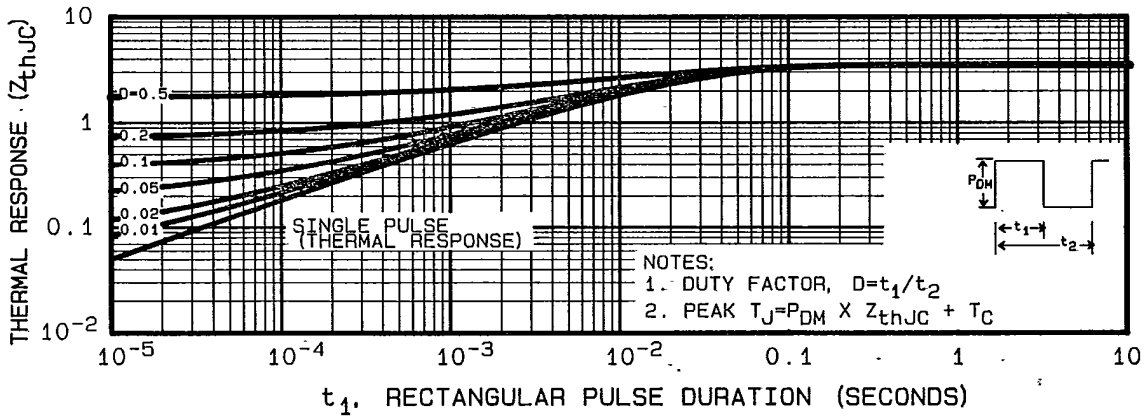


Fig. 5 - Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

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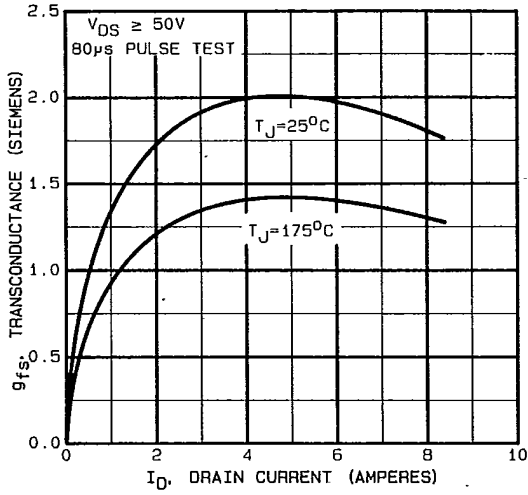


Fig. 6 — Typical Transconductance Vs. Drain Current

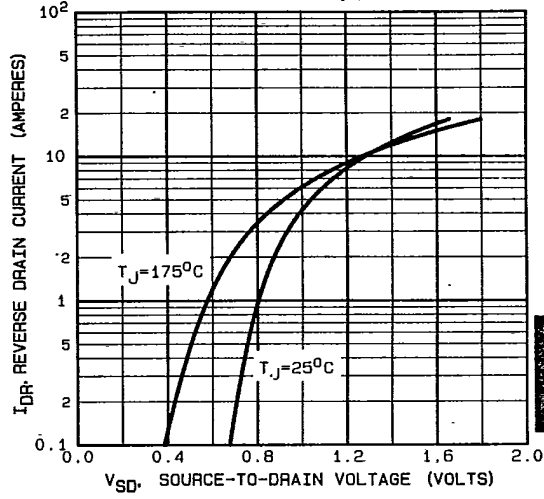


Fig. 7 — Typical Source-Drain Diode Forward Voltage

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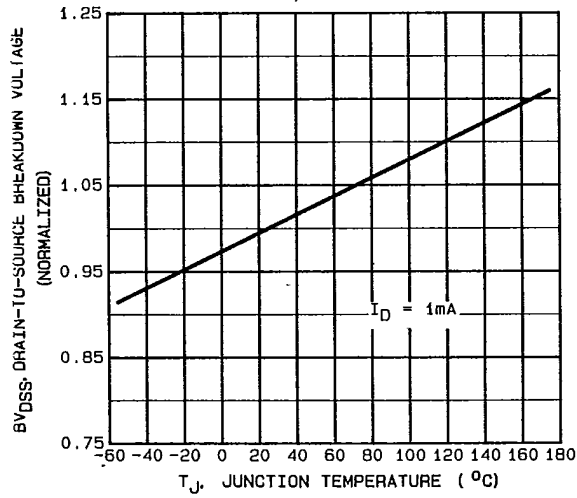


Fig. 8 — Breakdown Voltage Vs. Temperature

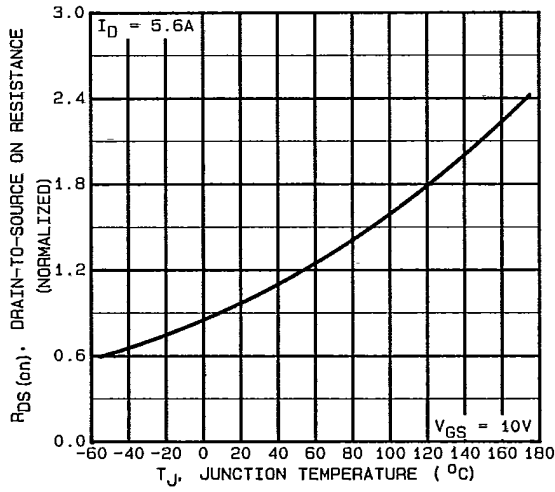


Fig. 9 — Normalized On-Resistance Vs. Temperature

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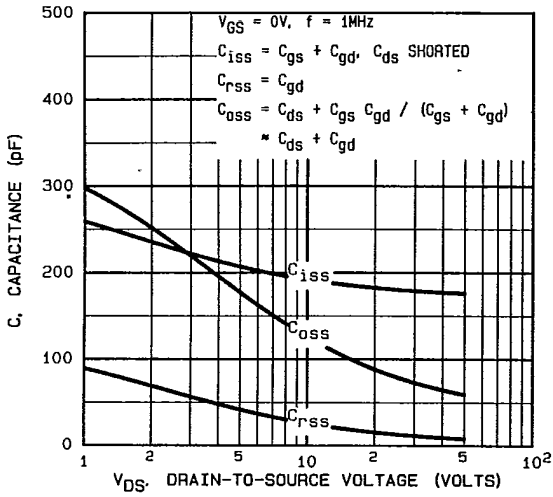


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

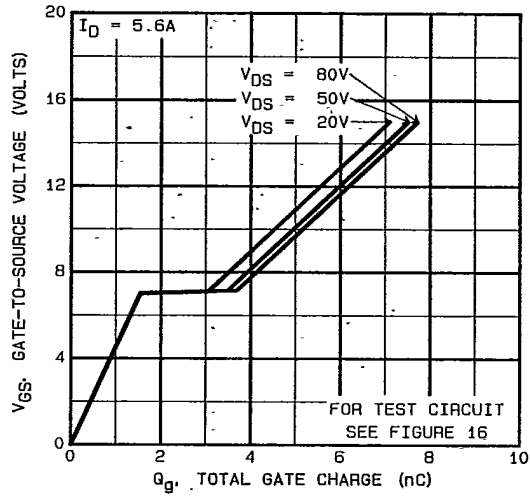


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

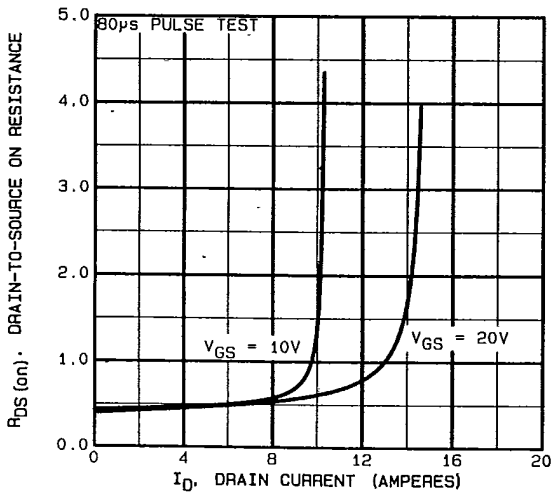


Fig. 12 — Typical On-Resistance Vs. Drain Current

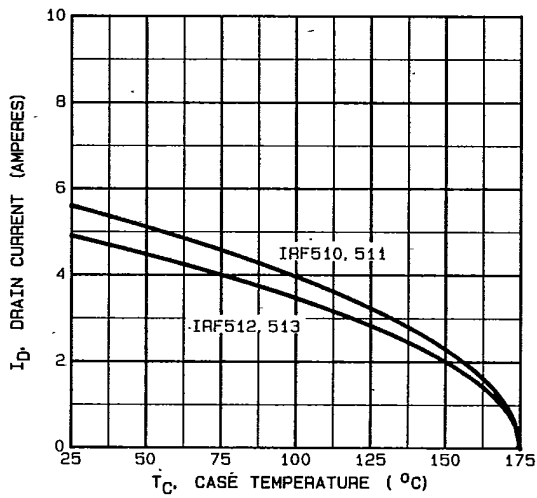


Fig. 13 — Maximum Drain Current Vs. Case Temperature

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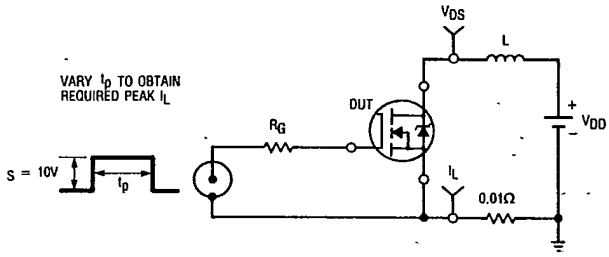


Fig. 14a — Unclamped Inductive Test Circuit

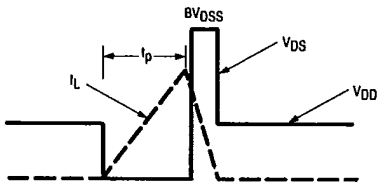


Fig. 14b — Unclamped Inductive Waveforms

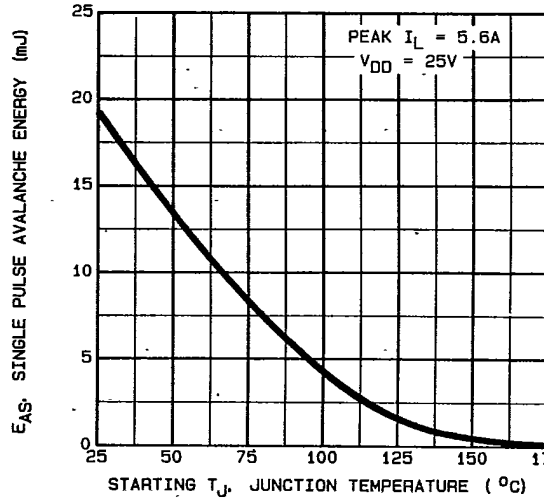


Fig. 14c — Maximum Avalanche Energy vs. Starting Junction Temperature

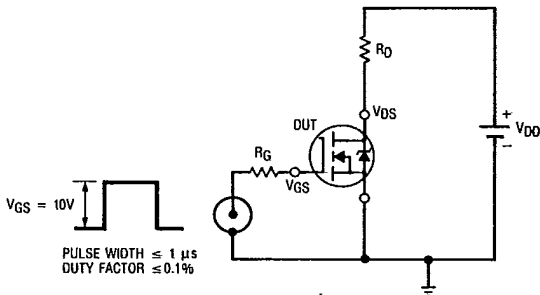


Fig. 15a — Switching Time Test Circuit

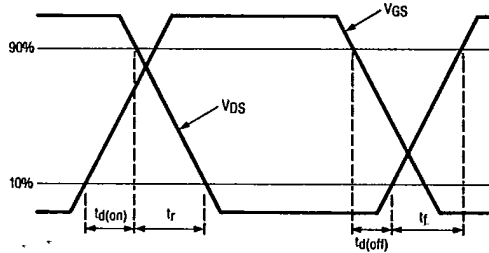


Fig. 15b — Switching Time Waveforms

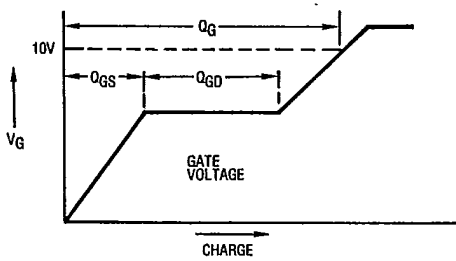


Fig. 16a — Basic Gate Charge Waveform

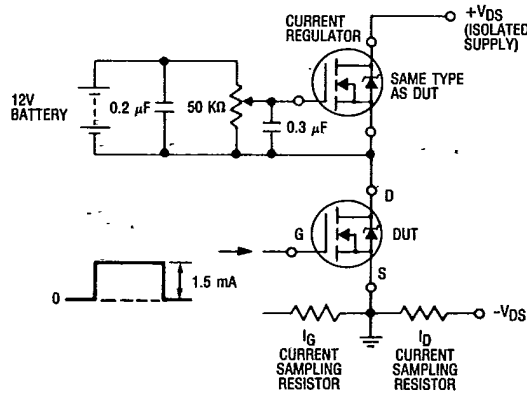


Fig. 16b — Gate Charge Test Circuit

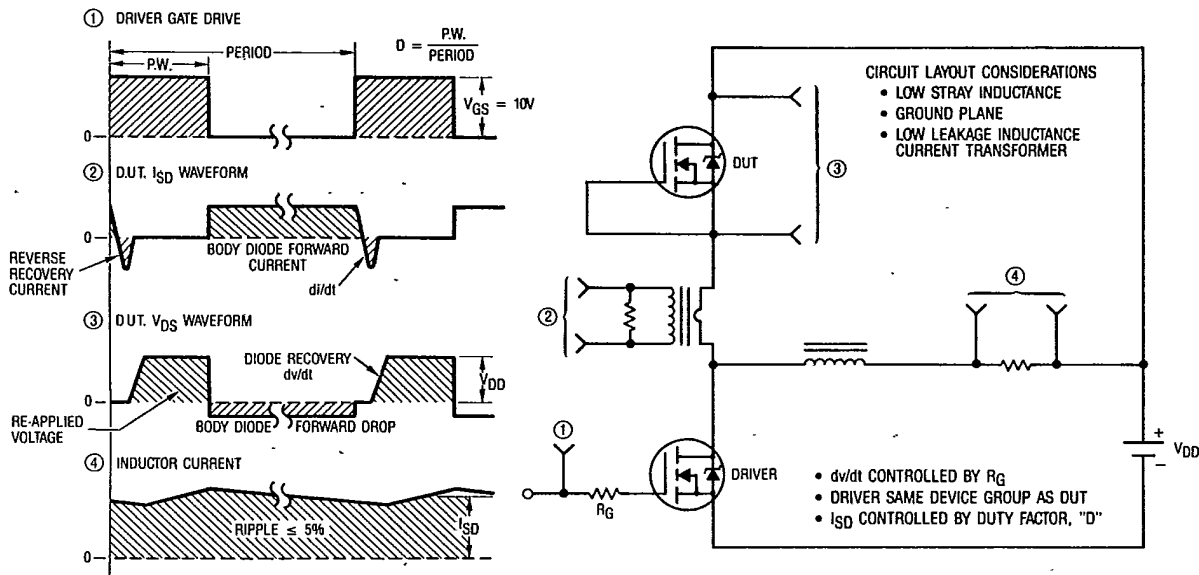
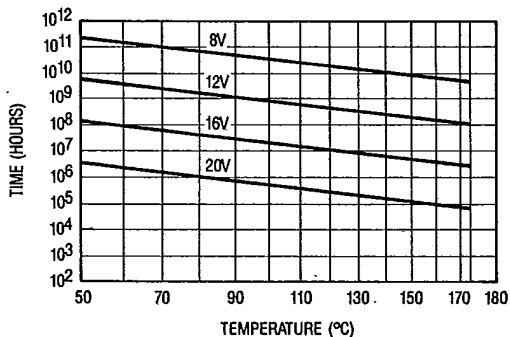
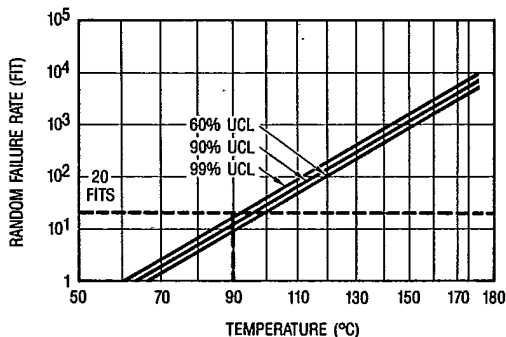


Fig. 17 — Peak Diode Recovery  $dv/dt$  Test Circuit



\*Fig. 18 — Typical Time to Accumulated 1% Gate Failure



\*Fig. 19 — Typical High Temperature Reverse Bias (HTRB) Failure Rate

\*The data shown is correct as of January 15, 1987. This information is updated on a quarterly basis; for the latest reliability data, please contact your local IR field office.