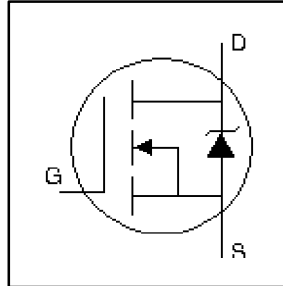


HEXFET® Power MOSFET

- Advanced Process Technology
- Ultra Low On-Resistance
- Isolated Package
- High Voltage Isolation = 2.5KVRMS^⑥
- Sink to Lead Creepage Dist. = 4.8mm
- Logic-Level Gate Drive
- $R_{DS(on)}$ Specified at $V_{GS}=5.0V$ & $10V$

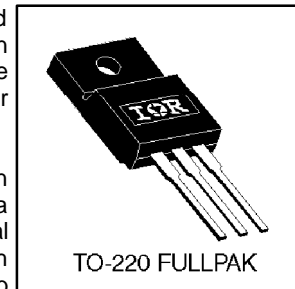


$V_{DSS} = 30V$
$R_{DS(on)} = 0.010\Omega$
$I_D = 52A$ ^⑤

Description

Fourth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve the lowest possible on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient device for use in a wide variety of applications.

The TO-220 Fullpak eliminates the need for additional insulating hardware in commercial-industrial applications. The moulding compound used provides a high isolation capability and a low thermal resistance between the tab and external heatsink. This isolation is equivalent to using a 100 micron mica barrier with standard TO-220 product. The Fullpak is mounted to a heatsink using a single clip or by a single screw fixing.




Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ $T_C = 25^\circ C$	Continuous Drain Current, V_{GS} @ 10V	52 ^⑤	A
I_D @ $T_C = 100^\circ C$	Continuous Collector Current, V_{GS} @ 10V	37	
I_{DM}	Pulsed Drain Current ^①	210	
P_D @ $T_C = 25^\circ C$	Power Dissipation	48	W
	Linear Derating Factor	0.32	W/ $^\circ C$
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy ^②	90	mJ
I_{AR}	Avalanche Current ^③	31	A
E_{AR}	Repetitive Avalanche Energy ^④	4.8	mJ
dv/dt	Peak Diode Recovery dv/dt ^③	4.5	V/ns
T_J	Operating Junction and	-55 to + 175	$^\circ C$
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 screw.	10 lbf•in (1.1N•m)	

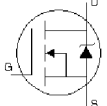
Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	3.1	$^\circ C/W$
$R_{\theta JA}$	Junction-to-Ambient	—	—	65	

Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	30	—	—	V	$V_{GS} = 0V, I_D = 250\mu A, T_J > -40^\circ\text{C}$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.039	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.010	Ω	$V_{GS} = 10V, I_D = 31A$ ④
		—	—	0.015		$V_{GS} = 5.0V, I_D = 26A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	1.0	—	2.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
g_{fs}	Forward Transconductance	44	—	—	S	$V_{DS} = 25V, I_D = 55A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	$V_{DS} = 30V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 24V, V_{GS} = 0V, T_J = 150^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 10V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -10V$
Q_g	Total Gate Charge	—	—	85	nC	$I_D = 46A, V_{DS} = 24V, V_{GS} = 5.0V$
		—	—	150		$I_D = 55A$
Q_{gs}	Gate-to-Source Charge	—	—	23	ns	$V_{DS} = 24V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	36		$V_{GS} = 10V$, See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	—	9.1	—		$V_{DD} = 15V$
t_r	Rise Time	—	110	—	ns	$I_D = 55A$
$t_{d(off)}$	Turn-Off Delay Time	—	110	—		$R_G = 5.0\Omega$
t_f	Fall Time	—	100	—		$R_D = 0.26\Omega$, See Fig. 10 ④
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	3700	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	1700	—		$V_{DS} = 25V$
C_{rss}	Reverse Transfer Capacitance	—	310	—		$f = 1.0\text{MHz}$, See Fig. 5
C	Drain to Sink Capacitance	—	12	—		$f = 1.0\text{MHz}$

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	52	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	210		
V_{SD}	Diode Forward Voltage	—	—	1.6	V	$T_J = 25^\circ\text{C}, I_S = 31A, V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	—	59	89	ns	$T_J = 25^\circ\text{C}, I_F = 55A$
Q_{rr}	Reverse Recovery Charge	—	0.11	0.17	μC	$di/dt = 100A/\mu s$ ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ② $V_{DD} = 25V$, starting $T_J = 25^\circ\text{C}$, $L = 20\mu H$, $R_G = 25\Omega$, $I_{AS} = 55A$. (See Figure 12)
- ③ $I_{SD} \leq 55A, di/dt \leq 100A/\mu s, V_{DD} \leq V_{(BR)DSS}, T_J \leq 175^\circ\text{C}$
- ④ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.
- ⑤ Calculated continuous current based on maximum allowable junction temperature; for recommended current-handling of the package refer to Design Tip # 93-4

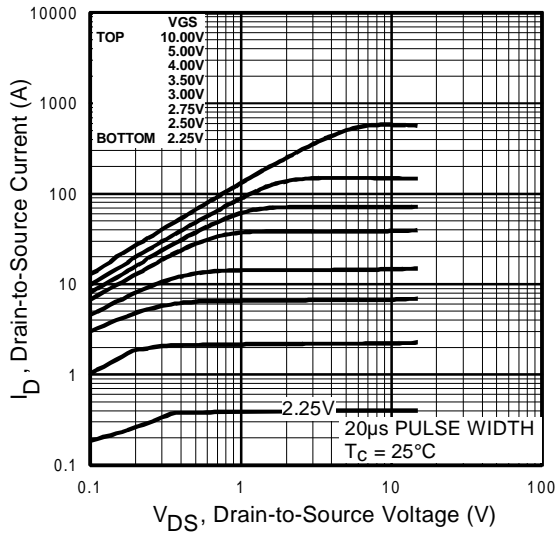


Fig 1. Typical Output Characteristics,
 $T_C = 25^\circ\text{C}$

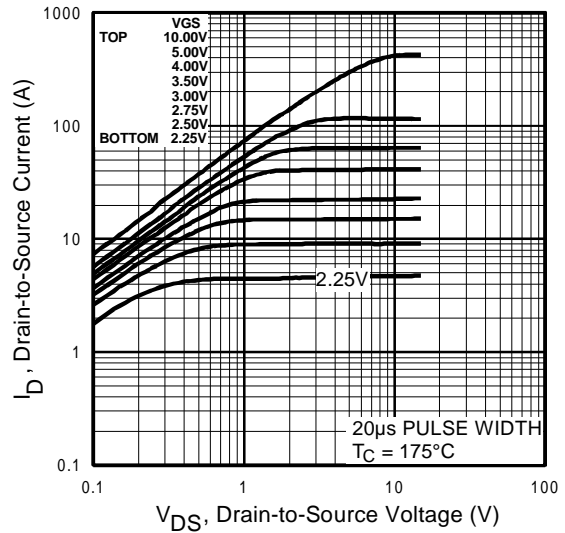


Fig 2. Typical Output Characteristics,
 $T_C = 175^\circ\text{C}$

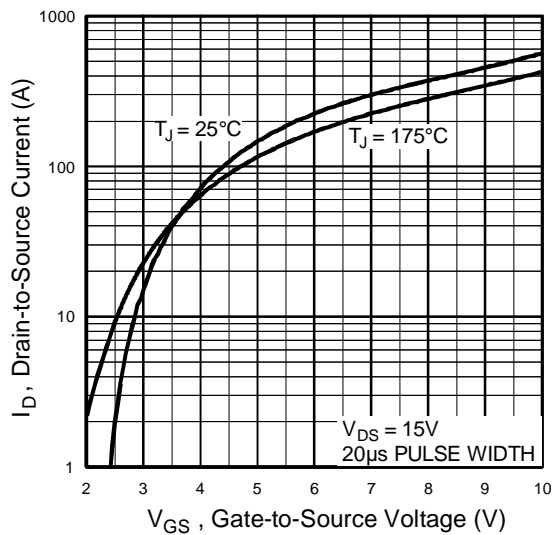


Fig 3. Typical Transfer Characteristics

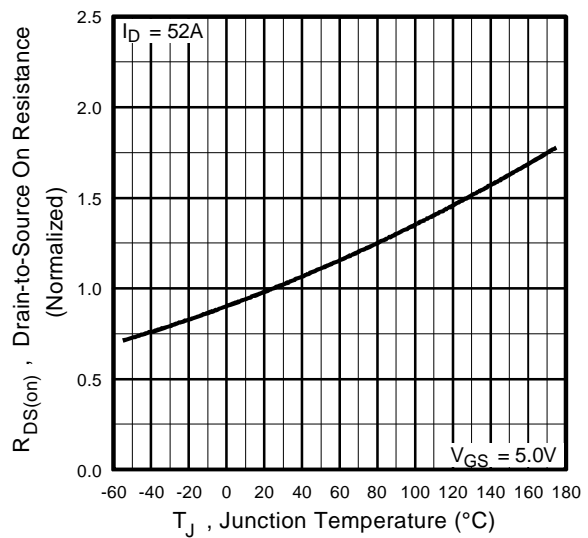


Fig 4. Normalized On-Resistance
Vs. Temperature

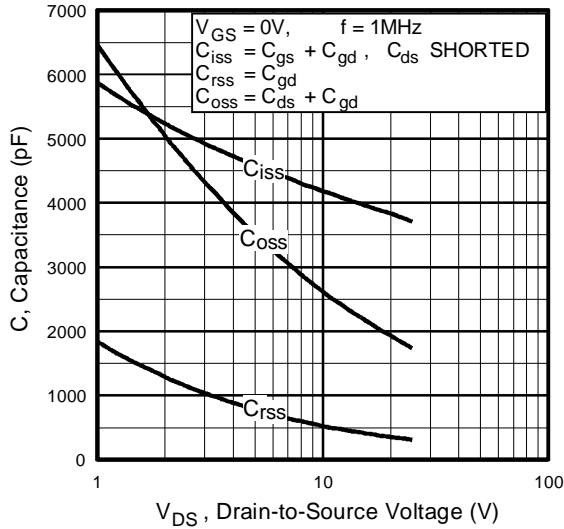


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

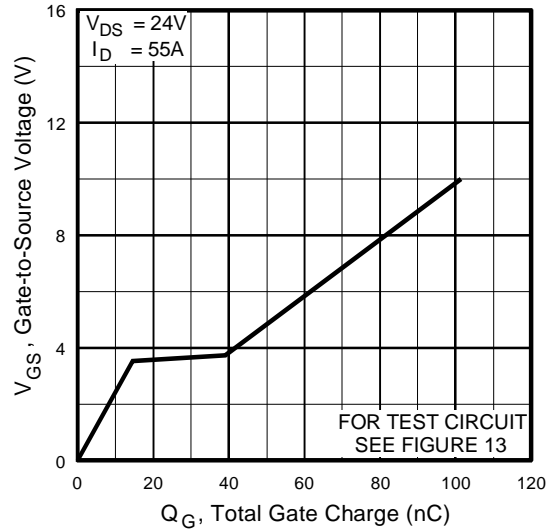


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

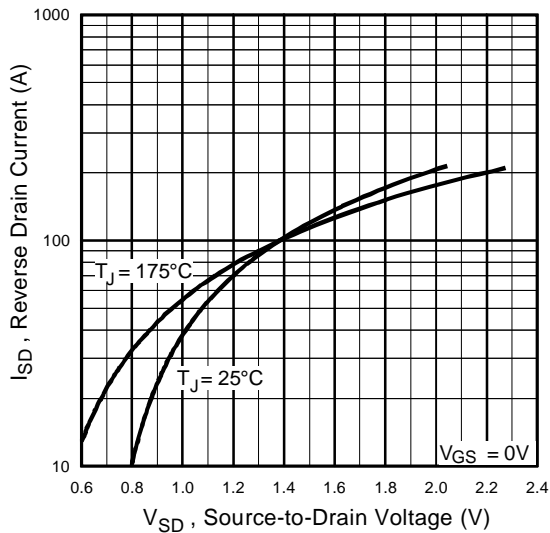


Fig 7. Typical Source-Drain Diode Forward Voltage

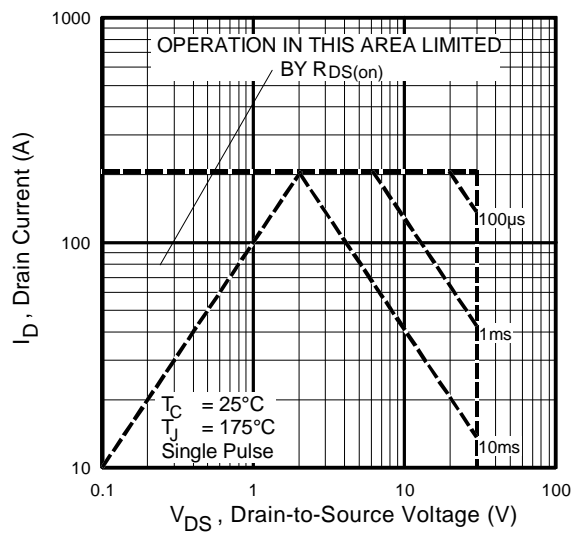


Fig 8. Maximum Safe Operating Area

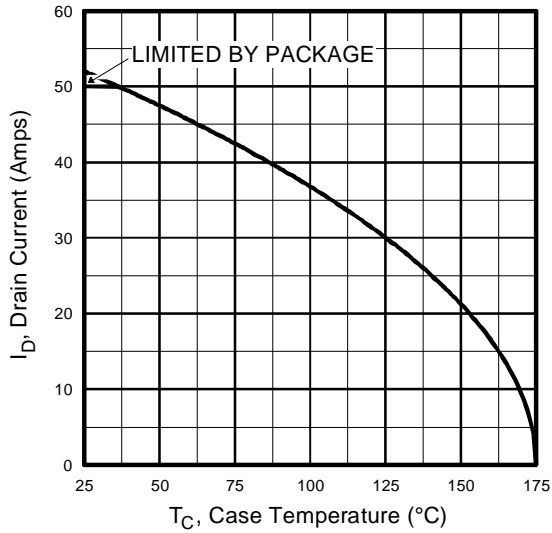


Fig 9. Maximum Drain Current Vs. Case Temperature

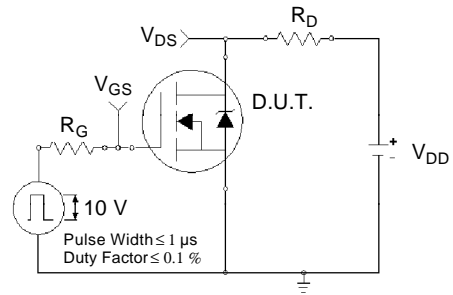


Fig 10a. Switching Time Test Circuit

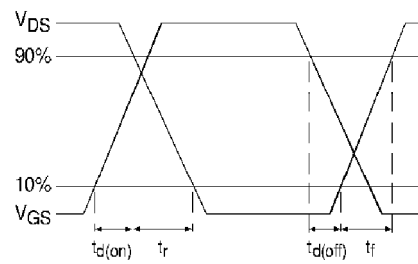


Fig 10b. Switching Time Waveforms

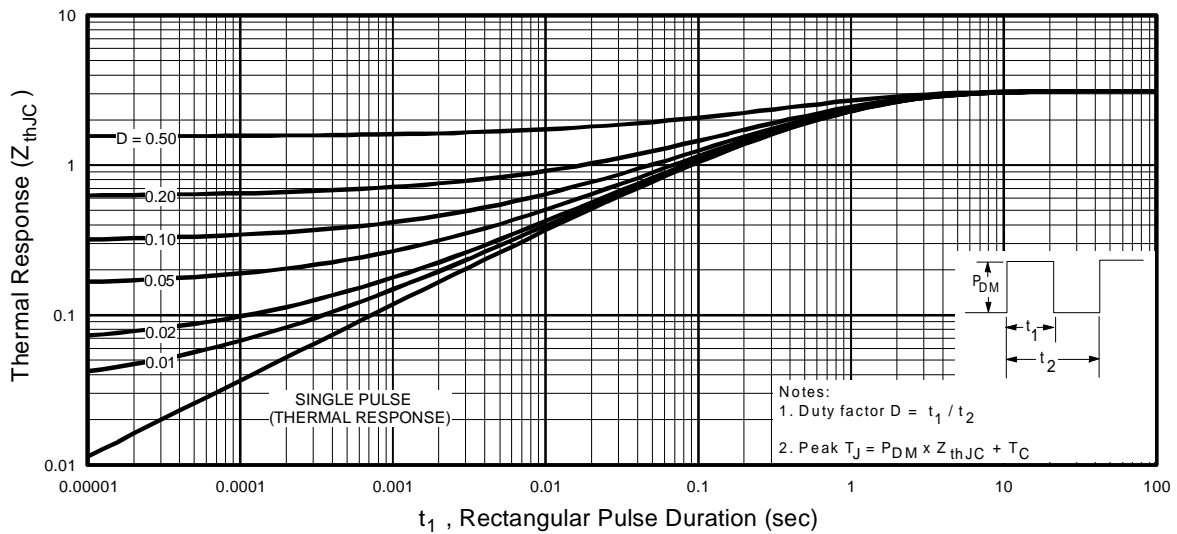


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

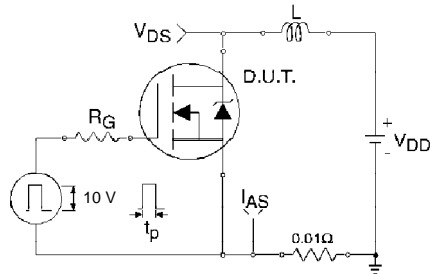


Fig 12a. Unclamped Inductive Test Circuit

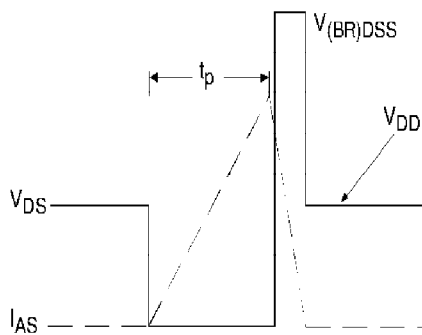


Fig 12b. Unclamped Inductive Waveforms

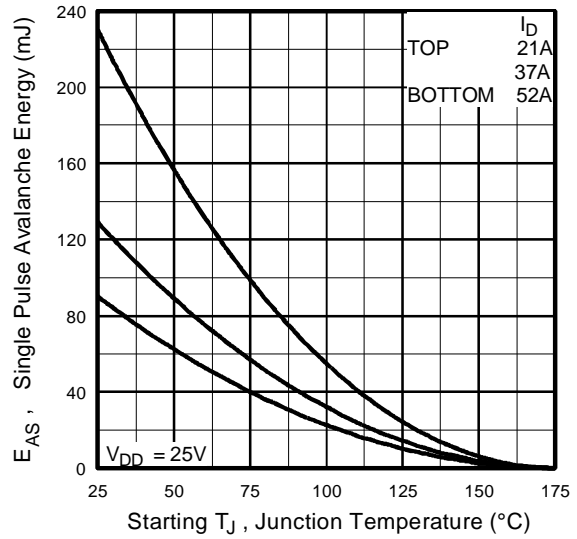


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

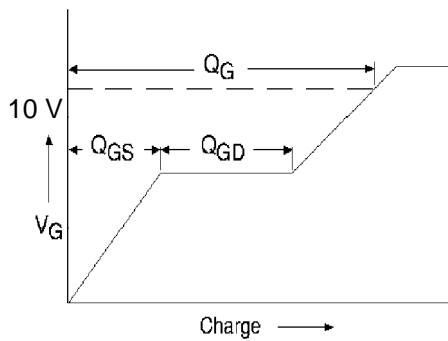


Fig 13a. Basic Gate Charge Waveform

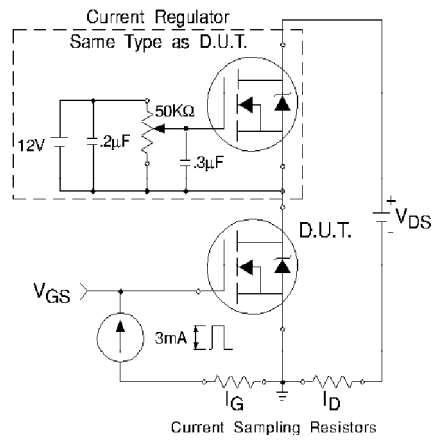
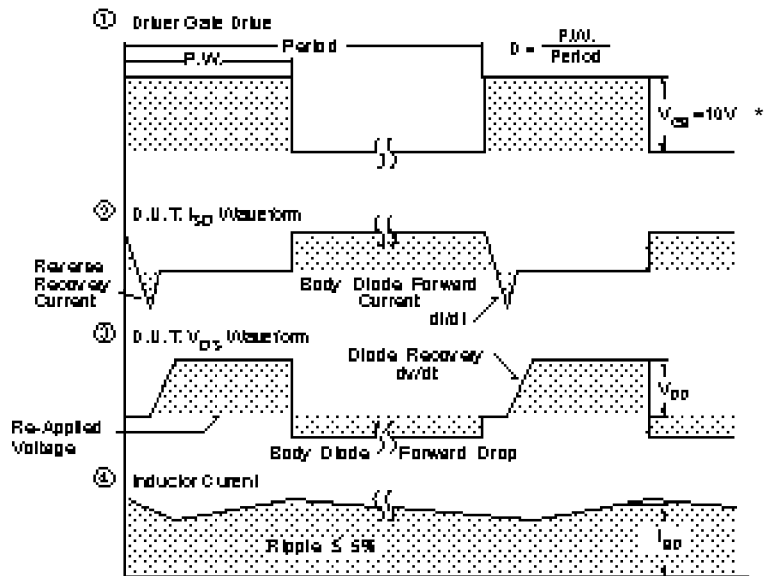
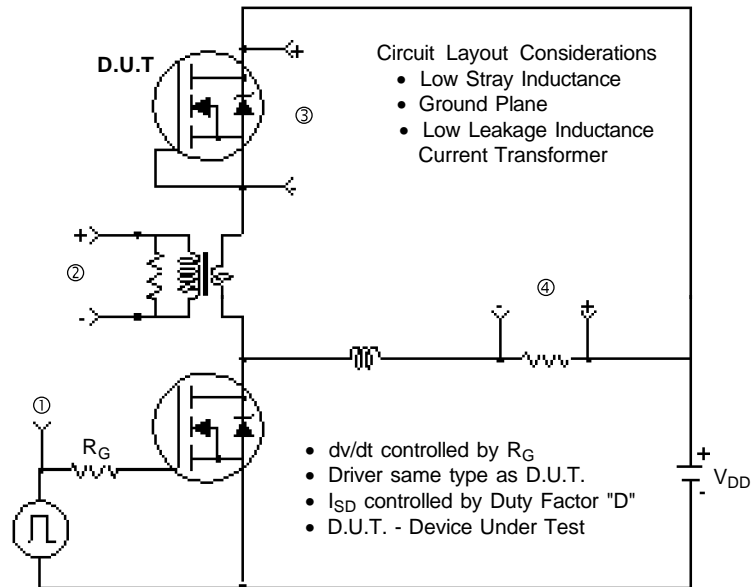


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* $V_{GS} = 5V$ for Logic Level Devices

Fig 14. For N-Channel HEXFETS

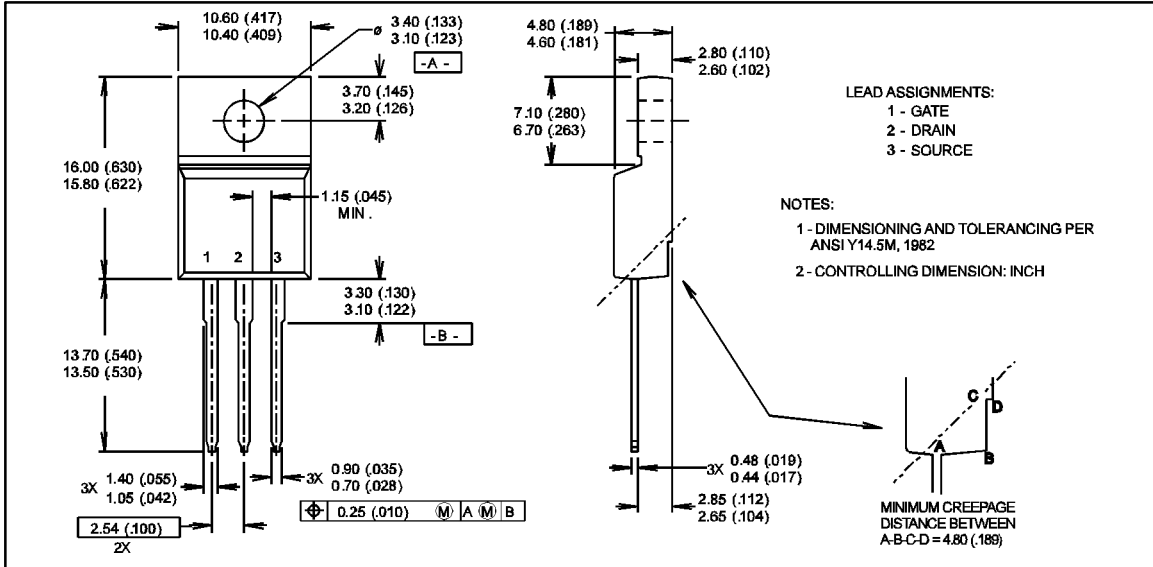
IRLI2203G



Package Outline

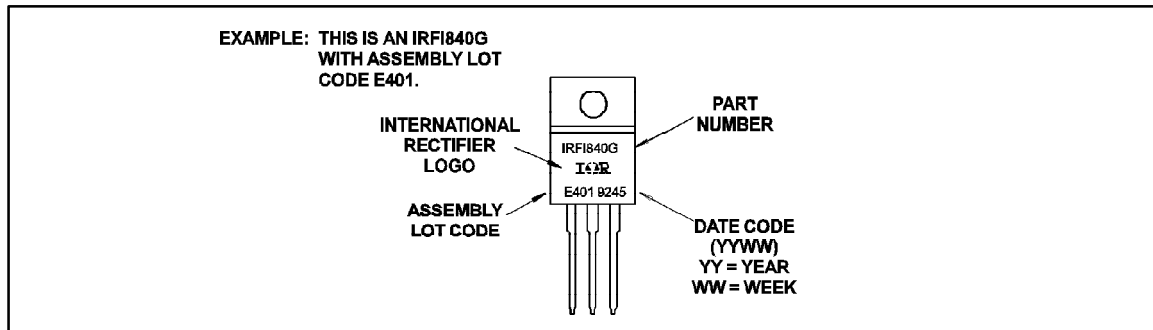
TO-220 FullPak Outline

Dimensions are shown in millimeters (inches)



Part Marking Information

TO-220 FullPak



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EUROPEAN HEADQUARTERS: Hurst Green, Oxted, Surrey RH8 9BB, UK Tel: (44) 0883 713215
IR CANADA: 7321 Victoria Park Ave., Suite 201, Markham, Ontario L3R 3L1, Tel: (905) 475 1897 **IR GERMANY:** Saalburgstrasse 157, 61350 Bad Homburg Tel: 6172 37066 **IR ITALY:** Via Liguria 49, 10071 Borgaro, Torino Tel: (39) 1145 10111 **IR FAR EAST:** K&H Bldg., 2F, 3-30-4 Nishi-Ikeburo 3-Chome, Toshima-Ki, Tokyo 171 Tel: (03)3983 0641 **IR SOUTHEAST ASIA:** 315 Outram Road, #10-02 Tan Boon Liat Building, Singapore, 0316 Tel: 65 221 8371

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